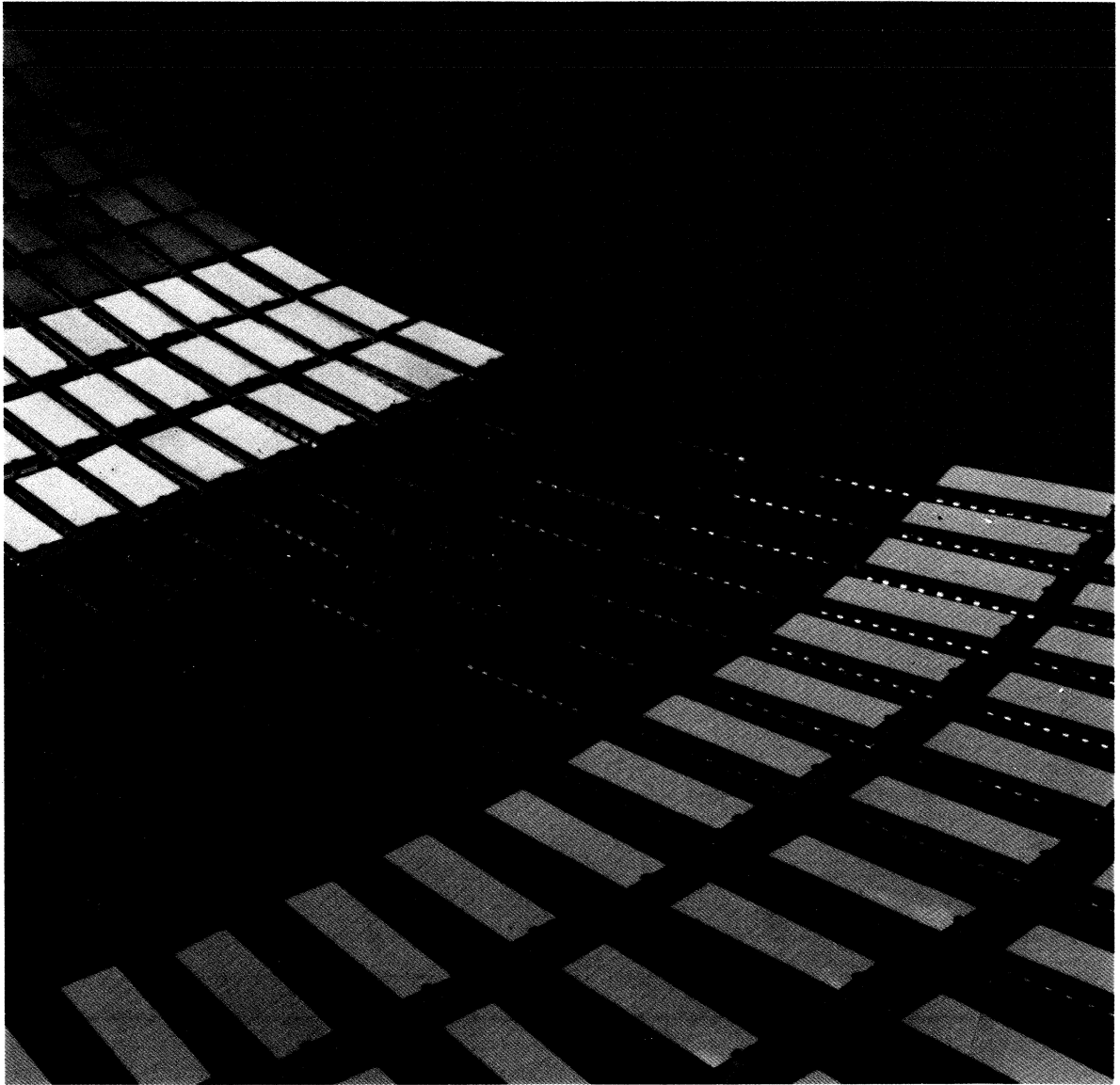
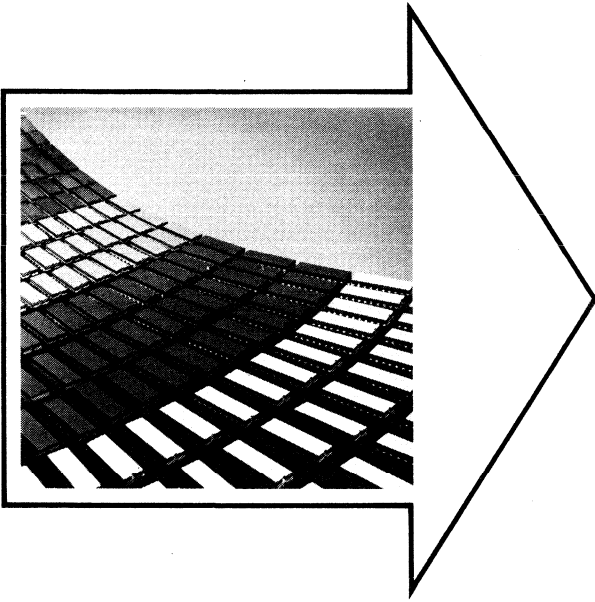


Bipolar LSI Data Book



Monolithic Memories

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Bipolar LSI Data Book

First Edition

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Introduction

This book has been prepared to give the user a concise list of all Bipolar LSI Products offered by Monolithic Memories. It is divided by products into sections on PROMs, ROMs, Character Generators, RAMs, Programmable Logic, LSI Logic, Arithmetic Elements and Interface. Each section has been designed to allow the user the most useable format for the products described. The PROM and ROM sections give data in the "generic" form allowing a quick review of the trade-off between devices. Cross references and selection guides are given where applicable. Programming and available programmers are given in detail. LSI Logic, Programmable Logic, Arithmetic Element and Interface data sheets are shown in detail for each product. New products to be introduced are shown with appropriate introduction quarter. This LSI data book was formatted with you, the user, in mind. For more information, contact the local Monolithic Memories sales representative or franchised distributor.

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Quality System

The quality system at Monolithic Memories is based on MIL-Q-9858, "Quality Program Requirements," MIL-I-45208, "Inspection System Requirements," and MIL-M-38510, Appendix A, "Product Assurance Program." MIL-M-38510 plays a significant role in structuring MMI's quality program.

MMI's facilities in Sunnyvale were certified in June of 1977 by DESC, Defense Electronics Supply Center, to manufacture and qualify to class B and class C Schottky Bipolar PROMs, ROMs and RAMs in accordance with the requirements of MIL-M-38510. This certification included a successful audit of our quality system to the stringent requirements of Appendix A of MIL-M-38510 which defines a Product Assurance Program tailored for integrated circuit manufacturers by DESC. This same quality system has also met the strict requirements of both "controlled" and "captive" line programs connected with our special Hi-Rel programs.

The quality accent at MMI is on process control as reflected in the use of many monitors and audits rather than gate inspections. This philosophy is consistent with building in quality and reliability rather than attempting to screen for it.

Process Control

MMI's advanced low-power Schottky TTL process uses such techniques as redundant masking to reduce random defects and self-aligning masking to reduce active chip area. Although more costly than the standard SSI or MSI Schottky TTL processes, these approaches yield better quality, increased reliability and lower overall cost due to higher net die per wafer. During the initial production stages of new designs and periodically thereafter, engineering characterizes the design-process compatibility by careful sample selection of lots reflecting process variable extremes.

Screening

Much of the assembly (packaging only) is performed offshore at our Penang, Malaysia facility. This facility has been qualified and is routinely monitored for conformance to MIL-STD-883 by MMI's military customers as well as by MMI's Quality Assurance Department. All standard hermetic MMI products are 100% screened to MIL-STD-883 Class C. This includes:

- Pre-cap inspection.*
- High-temperature storage at 150°C.
- Temperature cycling. -65°C to +150°C
- Constant acceleration.
- Fine and gross leak.
- Final electrical test.
- Q.A. sample acceptance testing.

*Modified for LSI.

The product assurance levels which MMI guarantees are listed in the table on this page.

Reliability Engineering maintains product surveillance through routine sampling and submission to MIL-STD-883, method 5005, qualification testing. Additional step-stress and extended (limit) testing conditions are used when warranted. In general, failure rates have been found to be two orders of magnitude better than MIL-HDBK-217 estimates.

The quality organization is defined into three departments:

- Quality control
- Quality assurance
- Reliability assurance

Quality Assurance (AQL) Levels

TEST	LEVEL I COMMERCIAL (%)	LEVEL II MILITARY (%)
Hermeticity (includes fine and gross)	0.65	0.4
Electrical		
DC at 25°C	.40	.25
Functional at 25°C	.40	.25
AC at 25°C	.65	.40
DC at Temperature Extremes	.65	.65
Functional at Temperature Extremes	.65	.65
AC at Temperature Extremes	1.5	1.5

Hi-Rel Products

Hi-Rel Products

All of the products at MMI were designed to operate over the entire military performance specification of $\pm 10\%$ V_{CC} tolerance and -55° to $+125^{\circ}\text{C}$ operating temperature ambient. Recently our 1024 bit Schottky PROM, MM5300-1/01-1 and our 2048 bit Schottky PROM, MM5305-1/06-1 was qualified to Part II of the MIL-M-38510 QPL. Other devices are in the process of QPL qualification.

Monolithic Memories offers a complete line of high reliability devices. All standard military temperature range devices can be processed to MIL-STD-883 as outlined on the following pages. Many devices are available from stock. In addition to standard MIL-STD-883 high reliability devices, Monolithic Memories has the ability to process parts to custom high reliability specifications. Some examples are:

- 100% Instant on (cold start) testing at -55°C
- Read and record data with Δ drift parameters
- Extended burn-in screening
- 100% AC, DC and functional testing at temperature extremes -55° and $+125^{\circ}\text{C}$
- DPA, Destructive Physical Analysis

- SEM, Scanning Electron Microscopic evaluation on a wafer lot basis
- Special lot traceability to critical wafer fabrication processes, i.e., metalization
- Residual gas analysis on hermetic packages
- Custom lot qualification tests
- Special customer source inspection at pre-cap, SEM, process control monitoring points or at lot qualification testing

If you want an off the shelf MIL-M-38510 QPL product call your factory representative for an up to date status on our QPL program.

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Flat Packs/Chip Carriers and Die

Most of our products are available in flat packs (see individual selection guides and the package appendix for details), and our manufacturing line can accommodate your chip carrier packaging requirements as well. If your needs are for the ultimate in density, we can also supply LSI chips for your hybrid applications. These can be furnished with special 100% testing and optical inspection screens geared for hybrid packaging.

Qualification & Quality Conformance Inspection

Subgroups and LTPD Levels as Given in MIL-STD-883, Method 5005, Class B and C Parts.

Table 1. Group A Electrical Tests

SUBGROUPS	LTPD		INITIAL SAMPLE SIZE*	
	B	C	B	C
Subgroup 1—Static Tests at $+25^{\circ}\text{C}$	5	5	45	45
Subgroup 2—Static Tests at Maximum Rated Operating Temperature	7	10	32	22
Subgroup 3—Static Tests at Minimum Rated Operating Temperature	7	10	32	22
Subgroup 4—Dynamic Tests at $+25^{\circ}\text{C}$ **	5	5	45	45
Subgroup 5—Dynamic Tests at Maximum Rated Operating Temperature**	7	10	32	22
Subgroup 6—Dynamic Tests at Minimum Rated Operating Temperature**	7	10	32	22
Subgroup 7—Functional Tests at $+25^{\circ}\text{C}$	5	5	45	45
Subgroup 8—Functional Tests at Maximum and Minimum Rated Operating Temperatures	10	15	22	15
Subgroup 9—Switching Tests at $+25^{\circ}\text{C}$ Except Unprogrammed PROM	7	10	32	22

*Groups A, B, C and D sampling plans are based on standard LTPD tables of MIL-M-38510, Appendix B. The smallest sample size, based on zero rejects allowed, has been chosen unless otherwise indicated. If necessary, the sample size will be increased once to the quantity corresponding to the next acceptance number.

**Dynamic tests are not applicable to digital memory devices; switching subgroup tests are performed to a specified functional pattern and dynamically exercised.

Hi-Rel Products

Hi-Rel Screening

MMI STANDARD HI-REL SCREENING*—MIL-STD-883 Class B/C, Method 5004

FLOW	METHOD*	883C				883B			
		PROM/FPLA/PAL		ROM	RAM/LSI*	PROM/FPLA/PAL		ROM	RAM/LSI*
		Unprogrammed	Programmed			Unprogrammed	Programmed		
Pre-cap visual (prior to seal)	2010 Cond. B	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Seal		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
High temp storage 24 hr. @ 150°C (after seal)	1008 Cond. C	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Temp. cycling 10 cycles, -65°C to +150°C	1010 Cond. C	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Constant acceleration: Y ₁ 30 KG	2001 Cond. E	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Leak: Fine—5 x 10 ⁻⁸ cc/sec	1014 Cond. A or B	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Gross—	1014 Cond. C								
Interim electrical test, DC & functional	MMI Data Sheet	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Test fuse/verify (DC)	MMI Std.	Yes	Yes	—	—	Yes	Yes	—	—
Program/verify	Customer Program	—	Yes	—	—	—	Yes	—	—
Burn-in 160 hr. @ 125°C	1015 Cond. D (Dynamic)	—	—	—	—	Yes	Yes	Yes	Yes
Final electrical test, DC, func. -55°C, +25°C, +125°C, AC @ 25°C	MMI Data Sheet	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Except AC +25°C for unprogrammed PROM									
Lot acceptance: group A									
-Sub. 1, 2, 3, 7, 8, 9—	Go/No Go	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Except sub 9 for unprogrammed PROMs	5005								

* LSI Logic Products

Table II. Group B Tests

TEST	METHOD*	CONDITIONS	LTPD	INITIAL*** SAMPLE SIZE
Subgroup 1				
A. Physical Dimensions	2016	MMI Data Sheet	No Failures	2
B. Internal Water-Vapor Content** D-1-B	1018	1000 ppm max. at +100°C	No Failures	3
Subgroup 2				
A. Resistance to Solvents	2015	Alcohol, mineral spirits, from solvents, Trichloroethelane, water	No Failures	3
B. Internal Visual and Mechanical	2014		No Failures	1
C. Bond Strength	2011	Condition D: 3 gram force minimum for aluminum wire, ultrasonic bonding	15	15 Wires from 10 Devices min.
Subgroup 3				
Solderability	2003	Soldering temperature of +260°C ± 10°C. 90% coverage, void concentration not to exceed 10% of area	15	15 Lead from 3 Devices min.

* MMI will screen and test to the latest issue in effect or as dictated by the contract.

** For packages with dessicant only.

*** All samples are devices unless otherwise stated.

Hi-Rel Products

Table III. Group C Tests (Die Related Tests)

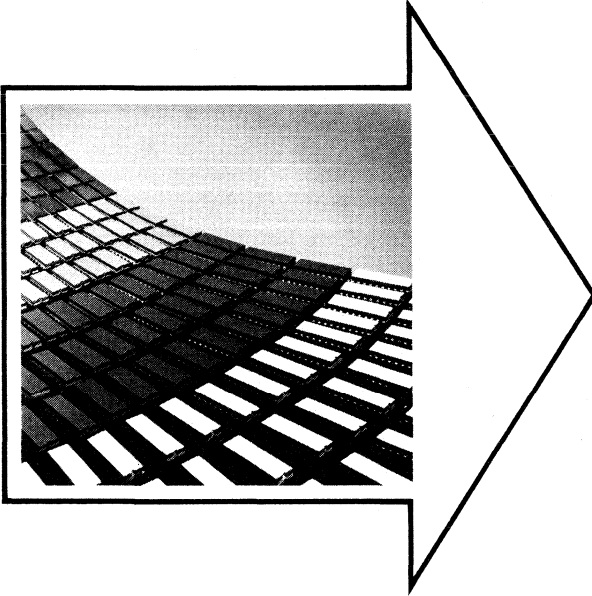
TEST	METHOD*	CONDITIONS	LTPD	INITIAL SAMPLE SIZE
Subgroup 1* Operating Life Test	1005.2	Steady state life: 1,000 hr., +125°C, condition D, dynamic	5	77 ACC = 1*
Subgroup 2* A. Temperature Cycling	1010	Test condition C: air to air, -65°C to +150°C, 10 cycles	15	15
B. Constant Acceleration (Centrifuge)	2001	Test condition E: 30kG centrifugal acceleration		
C. Seal (Fine and Gross)	1014	Test conditions test A or B and C		
D. Visual Examination	1010			

1

Table IV. Group D Tests (Package Related)

Subgroup 1 A. Physical Dimensions	2016	MMI Data Sheet	15	15
B. Internal Water Vapor Content	1018	5000 PPM max. @ 100°C	No Failures	3
Subgroup 2 A. Lead Fatigue	2004	Test condition B ₂ : 3 oz. for ribbon leads; 8 oz. for all others	15	15
B. Seal (Fine and Gross)	1014	Test conditions A or B and C	15	15
Subgroup 3* A. Thermal Shock	1011	Test method B: liquid to liquid, -55°C to +125°C, 15 cycles	15	15
B. Temperature Cycling	1010	Test condition C: air to air, -65°C to +150°C, 100 cycles		
C. Moisture Resistance	1004	Omit initial conditioning and vibration		
D. Seal (Fine and Gross)	1014	Test conditions A or B and C		
E. Visual examination	1004			
Subgroup 4* A. Mechanical Shock	2002	Test condition B: 5 shock pulses; 6 directions; 1500 g		
B. Vibration Variable Frequency	2007	Test condition A: 20 g	15	15
C. Constant Acceleration (Centrifuge)	2001	Test condition E: 30kg centrifugal acceleration		
D. Seal (Fine and Gross)	1014	Test conditions A or B and C		
E. Visual Examination	1010			
Subgroup 5 A. Salt Atmosphere (Corrosion)	1009	Test condition A: 24 hr.	15	15
B. Seal (Fine and Gross)	1014	Test conditions A or B and C		
C. Visual Examination	1009			

* Electrical end points, required for all subgroups (except in Group B and Subgroups 1, 2 and 5 of Group D), are room temperature, Subgroups 1, 2 and 3 of Group A DC tests, per MMI data sheet. Check factory for additional requirements.



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Bipolar PROM Selection Guide

Bipolar PROM Selection Guide

SIZE	MEMORY DESCRIPTION			MMI	AMD	FAIR-CHILD	HARRIS	INTEL	INTER-SIL	MOTOROLA	NATIONAL	RAYTHEON	SIGNETICS	TI		
	ORGANIZATION	OUTPUT	TYPE													
															PINS	
256	32x8	OC	STD	27S08/29750	6330-1	5600	HM-7602-5		5600		DM74S188		N82S23	SN74S188		
			S	27S18/27LS08	63S080*											
			LS	27LS08	63LS080*											
	1024	16	TS	STD	27S09/29751	6331-1	5610	HM-7603-5		5610		DM74S288		N82S123	SN74S288	
				S	27S19/27LS09	63S081*										
				LS	27LS09	63LS081*										
2048	256x4	OC	STD	29S10/29760	6300-1	5603	HM-7610-5	3601	5603		DM74S387	29660	N82S27/82S126	SN74S387		
			S	27S20	63S140								29662			
			LS		63LS140											
	2048	16	TS	PS		63PS140*							29661			
				STD	27S11/29761	6301-1	5623	HM-7611-5	3621	5623		DM74S287		N82S129	SN74S287	
				S	27S21	63S141										
2048	256x8	OC	STD		6308-1						DM74S470	29600		SN74S470		
			S		63S280*											
			LS		63LS280*											
	2048	16	TS	PS		63PS280*							29663			
				STD		6309-1							DM74S471	29601		SN74S471
				S		63S281*										
4096	512x8	OC	LS		63LS281*											
			PS		63PS281*											
			STD		6335-1											
	4096	512x8	TS	STD		6336-1										
				S		633A/283*										
				RA												
2048	512x4	OC	STD	27S12/29770	6305-1	5604	HM-7620-5	3602A	5604	MCM 7620	DM74S570	29610	N82S130			
			S	27S20	63S240											
			LS		63LS240											
	2048	16	TS	PS		63PS240*							29612			
				STD	27S13/29771	6306-1	5624	HM-7621-5	3602A	5624	MCM 7621	DM74S571	29611	N82S131		
				S	27S21	63S241										
4096	512x8	OC	LS		63LS241							29613				
			PS		63PS241*											
			STD		6348-1							DM74S473	29620	N82S146	SN74S473	
	4096	512x8	TS	S	27S28/29772	63S480*										
				LS		63LS480*										
				PS		63PS480*								29622		
4096	512x8	TS	STD		6349-1						DM74S472	29621	N82S147	SN74S472		
			S	27S29/29773	63S481*											
			LS		63LS481*											
			PS		63PS481*						29622					

Bipolar PROM Selection Guide

4096	512x8	24	OC	STD	6340-1 63S482* 63LS482* 63PS482*	27S30	93438	HM-7640-5 HM-7640A-5	3604A	5605	MCM 7640	DM87S295	29624	N82S140	SN74S475	
			TS	STD	6341-1 63S483* 63LS483* 63PS483*	27S31	93448	HM-7641-5 HM-7641-5	3624A	5625	MCM 7641	DM87S296	29625	N82S141	SN74S474	
			TS	RA	63RA483*		93452	HM-7642-5	3605	5606	MCM 7642	DM74S572		N82S136	SN74S477	
4096	1024x4	18	OC	STD	6352-1 63S440 63LS440 63PS440*	27S32		HM-7643-5	3625	5626	MCM 7643	DM74S573		N82S137	SN74S476	
			TS	STD	6353-1 63S441 63LS441 63PS441* 63RA441 63RS441	27S33	93453	HM-7680-5	3628	5618	MCM 7680	DM87S229	29630	N82S180	SN74S479	
			OC	S	63S880* 63LS880* 63PS880*		93450	HM-7680P-5	3628	5618	MCM 7681	DM87S228	29632	N82S181	SN74S478	
8192	1024x8	24	TS	STD	6381-1 63S881* 63LS881* 63PS881*		93451	HM-7681P-5								
			TS	RA	63RA883*											
			OC	S	63S840* 63LS840* 63PS840*											
8192	2048x4	18	TS	S	63S841* 63LS841* 63PS841*			HM-7685-5								
			TS	RA	63RA841*											
			OC	S	63S1680* 63LS1680* 63PS1680*											
16384	2048x8	24	TS	S	63S1681* 63LS1681* 63PS1681*			HM-76161-5	3636							
			TS	RA	63RA1683*											
			OC	S	63S1640* 63LS1640* 63PS1640*											
16384	4096x4	20	TS	S	63S1641* 63LS1641* 63PS1641* 63RA1641* 63RS1641*											

Note: Only Commercial Specification Part Numbers Are Listed.

*Preliminary Data: Check With Factory.

STD = Standard
S = High Speed Schottky

LS = Low Power
PS = Power Switched

RA = Registered Asynchronous
RS = Registered Synchronous



Standard Performance Schottky Generic PROM Family 53/63XX-1

Features/Benefits

- Standard Schottky processing
- Reliability proven nichrome fusible links
(qualified for MIL-M-38510)
- Drop in compatible ROMs
- PNP inputs for low input current
- Compatible pin configurations for upward expansion
- 4-bit-wide and 8-bit-wide for byte oriented applications

Application

- Microprogram instruction
- Microprocessor program store
- Look up table
- Character generator
- Random logic
- Code converter

Description

The 53/63XX-1-series generic PROM family offers the widest selection of sizes and organizations available in the industry. The 4-bit-wide PROMs range from 256x4 to 1024x4 and feature upward/downward pin out compatibility in the space saving 16 and 18 pin packages. The 8-bit-wide PROMs range from 32x8 to 1024x8 in a wide selection of package sizes. All PROMs have the same programming specifications allowing a single generic programmer.

The family features low input current PNP inputs, full Schottky clamping and three-state and open collector outputs. The nichrome fuses store a logical high and are programmed to the low state. Special on chip circuitry and extra fuses provide pre-programming tests which assure high programming yields and high reliability.

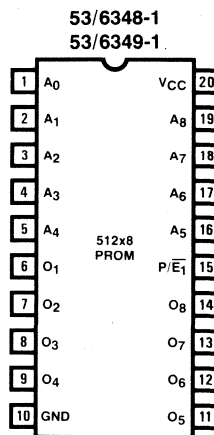
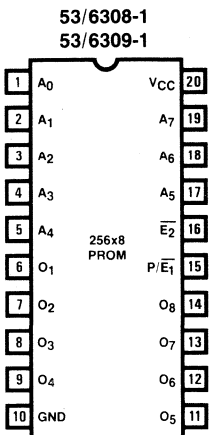
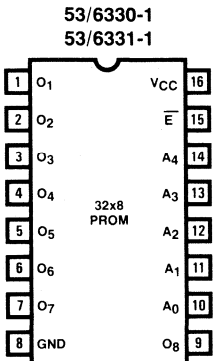
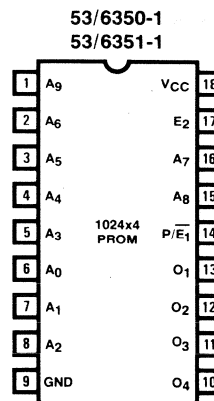
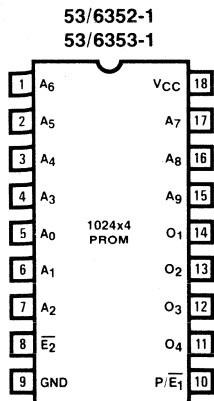
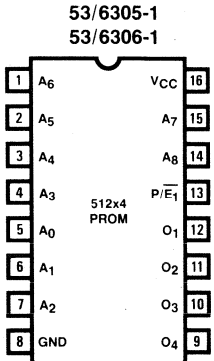
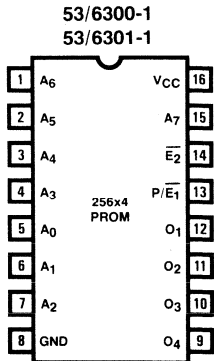
The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

Generic PROM Selection Guide

MEMORY			PACKAGE		DEVICE TYPE		INTERCHANGEABLE ROM		
SIZE	ORGANIZATION		PINS	TYPE*	0°C to +75°C	-55°C to +125°C	0°C to +75°C	-55°C to +125°C	
1K	256x4	OC	16	J, N, F	6300-1	5300-1	6200-1	5200-1	
		TS			6301-1	5301-1	6201-1	5201-1	
2K	512x4	OC	16	J, N, F	6305-1	5305-1	6205-1	5205-1	
		TS			6306-1	5306-1	6206-1	5206-1	
4K	1024x4	OC	18	J, N, F	6350-1	5350-1	6250-1	5250-1	
		TS			6351-1	5351-1	6251-1	5251-1	
		OC			6352-1	5352-1	6252-1	5252-1	
		TS			6353-1	5353-1	6253-1	5253-1	
¼K	32x8	OC	16	J, N, F	6330-1	5330-1	6230-1	5230-1	
		TS			6331-1	5331-1	6231-1	5231-1	
2K	256x8	OC	20	J, N	6308-1	5308-1	6208-1	5208-1	
		TS			6309-1	5309-1	6209-1	5209-1	
		OC	24	J, N, F	6335-1	5335-1	6235-1	5235-1	
		TS			6336-1	5336-1	6236-1	5236-1	
4K	512x8	OC	24	J, N, F	6340-1	5340-1	6240-1	5240-1	
		TS			6341-1	5341-1	6241-1	5241-1	
		OC	20	J, N	6348-1	5348-1	6248-1	5248-1	
		TS			6349-1	5349-1	6249-1	5249-1	
8K	1024x8	OC	24	J, N, F	6380-1	5380-1	6280-1	5280-1	
		TS			6381-1	5381-1	6281-1	5281-1	
		OC					5384-1*	6284-1	5284-1
		TS					5385-1*	6285-1	5285-1

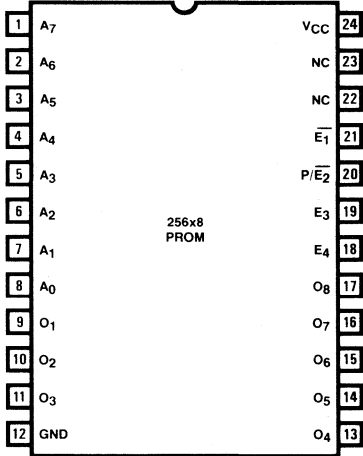
* Package Types: N is Plastic DIP, J is Ceramic DIP and F is Flat Pak

Pin Configurations

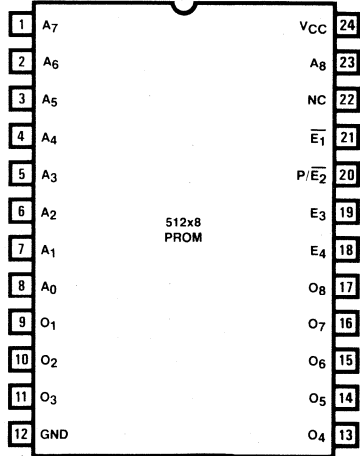


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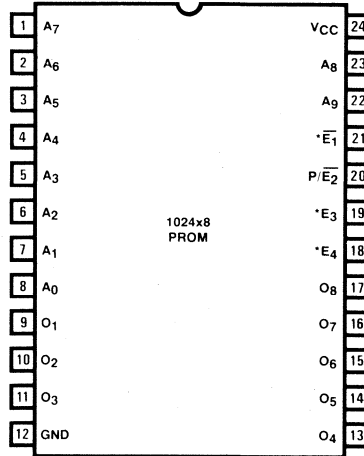
53/6335-1
53/6336-1



53/6340-1
53/6341-1



53/6380-1, *5384-1
53/6381-1, *5385-1



*NO CONNECTION Replacement for 2708 EPROM.
NOTE: Pin assignments for ceramic (J package), plastic (N package) and flat pack (F package) are the same.

Absolute Maximum Ratings

Supply Voltage, V_{CC}	-0.5V to +7.0V
Input Voltage	-1.5V to +5.5V
Input Current	-20 mA to +5 mA
Output Current	-100 mA to +100 mA
Storage Temperature Range	-65°C to +150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	Military			Commercial			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply Voltage	4.5	5.0	5.5	4.75	5.00	5.25	V
I_{OH}	High-Level Output Current			-2.0			-3.2	mA
I_{OL}	Low-Level Output Current	'00, '01, '05, '06, '08, '09, '35, '36, '40, '41, '48, '49, '50, '51, '52, '53		12			16	mA
		'30, '31, '80, '81, '84, '85		8		12	mA	
T_A	Operating Free Air Temperature	-55		125	0		75	°C

Electrical Characteristics**Over Recommended Operating Free Air Temperature Range (Unless Otherwise Noted)**

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-Level Input Voltage		2.0			V
V_{IL}	Low-Level Input Voltage				0.8	V
V_{IC}	Input Clamp Voltage	$V_{CC} = \text{MIN}, I_I = -18\text{mA}$			-1.5	V
V_{OL}	Low-Level Output Voltage	$V_{CC} = \text{MAX}, I_{OL} = \text{Max}$			0.50	V
I_I	Maximum Input Current	$V_{CC} = \text{MAX}, V_I = 4.5\text{V}$ (Program Pin) $V_I = 5.5\text{V}$ (Other Inputs)			1.0	mA
I_{IH}	High-Level Input Current	$V_{CC} = \text{MAX}, V_I = 2.4\text{V}$			40	μA
I_{IL}	Low-Level Input Current	$V_{CC} = \text{MAX}, V_I = 0.45\text{V}$			-250	μA
C_I	Input Capacitance	$V_{CC} = 5.0\text{V}$ $T_A = 25^\circ\text{C}$ $f = 1\text{MHz}$			7	pF
C_O	Output Capacitance	$V_I = 2.0\text{V}$ $V_O = 2.0\text{V}$			8	pF
I_{CC}	Supply Current	'30, '31		90	125	mA
		'00, '01, '05, '06		95	130	
		'08, '09, '48, '49	$V_{CC} = \text{MAX}$	115	155	
		'35, '36, '40, '41	All inputs grounded	125	170	
		'50, '51, '52, '53	All outputs open	130	175	
		'80, '81, '84, '85		135	180	

OPEN COLLECTOR OUTPUT CURRENT

I_{CEX}	Output Leakage Current	$V_{CC} = \text{MAX}, V_O = 2.4\text{V}$	100	μA
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THREE STATE OUTPUT ONLY

V_{OH}	High-Level Output Voltage	$V_{CC} = \text{MIN}, I_{OH} = \text{Max}$	2.4	V
I_{HZ}	High-Level OFF State Output Current	$V_{CC} = \text{MAX}, V_O = 2.4\text{V}$	100	μA
I_{LZ}	Low-Level OFF State Output Current	$V_{CC} = \text{MAX}, V_O = 0.5\text{V}$	-100	μA
I_{OS}	Output Short Circuit Current	$V_{CC} = 5.0\text{V}, V_O = 0\text{V}$	-20	-90

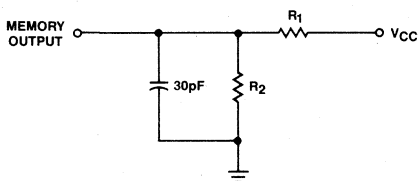
Switching Characteristics

Over Recommended Ranges of T_A and V_{CC} (Unless Otherwise Noted)

DEVICE TYPE	CONDITIONS (See standard test load)		t_{AA} (ns) ADDRESS ACCESS TIME	t_{EA} & t_{ER} (ns) ENABLE ACCESS & RECOVERY TIME
	R_1 (Ω)	R_2 (Ω)	MAX	MAX
6300-1, 6301-1	300	600	55	30
5300-1, 5301-1	375	750	75	40
6305-1, 6306-1	300	600	60	30
5305-1, 5306-1	375	750	75	40
6308-1, 6309-1	300	600	70	30
5308-1, 5309-1	375	750	80	40
6330-1, 6331-1	375	750	50	30
5330-1, 5331-1	560	1120	60	40
6335-1, 6336-1	300	600	70	30
5335-1, 5336-1	375	750	80	40
6340-1, 6341-1	300	600	70	30
5340-1, 5341-1	375	750	80	40
6348-1, 6349-1	300	600	70	30
5348-1, 5349-1	375	750	80	40
6350-1, 6351-1	300	600	60	30
5350-1, 5351-1	375	750	75	40
6352-1, 6353-1	300	600	60	30
5352-1, 5353-1	375	750	75	40
6380-1, 6381-1	375	750	90	40
5380-1, 5381-1	560	1120	125	40
5384-1, 5385-1	560	1120	125	40

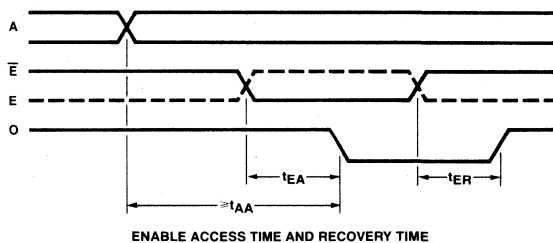
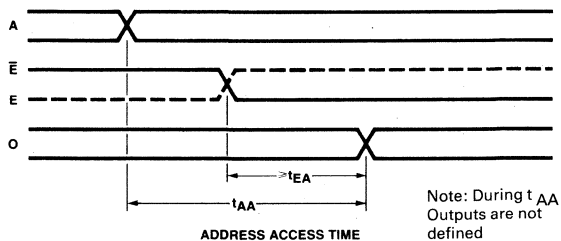
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Standard Test Load



Input Pulse Amplitude 3.0V
Input Rise and Fall Times 5ns from 1.0V to 2.0V
Measurements Made at 1.5V

Definition of Waveforms



Standard Performance Schottky PROM Programming Instructions 53/63XX-1

Device Description

The 53/63XX-1 Generic PROM Family is manufactured with all outputs high in all storage locations. To make an output low at a particular word, a nichrome fusible link must be changed from a low resistance to a high resistance. This procedure is called programming.

Programming Description

To select a particular fusible link for programming, the word address is presented with TTL levels on all inputs a V_{CC} of 5.50V is applied or left applied, and the program pin (ordinarily an enable input) and the output to be programmed are taken to an elevated voltage to supply the required current to program the fuse. The outputs must be programmed one output at a time, since internal decoding circuitry is capable of sinking only one unit of programming current at a time.

Other Enable Inputs

Other enable inputs are logic enables and are not used during programming. They may be high, low or open during programming. When checking that an output is programmed (which is called verification), the PROM must be enabled. The simplest procedure is to tie other enables into the enable position for programming and verification.

Programming Instructions

Timing

The programming procedure involves the use of the program pin (an enable) and the output pin. In order to guarantee that the output transistor is off before increasing the voltage on the output pin, the program pin's voltage pulse must come before the output pin's programming pulse. The programming pulse applied to the output pin and program pin must have a rise time rate of $0.34V/\mu\text{sec}$ to $0.46V/\mu\text{sec}$.

Verification

After programming a device, it can be checked for a low output by enabling the part. Since we must guarantee operation at minimum and maximum V_{CC} , load current and temperature, the device must be required to sink 12mA at 4.2V V_{CC} and 0.2mA at 6.0V V_{CC} at room temperature.

Unprogrammable Units

Visual inspection at 200X prior to encapsulation, test fuses and decoding circuitry tests are used to guarantee a high programming yield of the device in the field. However, because of random defects, it is impossible to guarantee that a link will open without actually programming it. Units returned to MMI as unprogrammable must be accompanied by a complete device truth table clearly indicating the location which could not be programmed, or which was falsely programmed. Otherwise, failure analysis is impossible.

Standard Schottky Generic PROM Family

MILITARY PART NO.	COMMERCIAL PART NO.	SIZE	CONFIGURATION	OUTPUT	NO. OF PINS	DATA I/O (ALL SERIES)		PRO-LOG (SERIES 90, 92)	
						PROGRAM CARD SET	SOCKET ADAPTER	PERSONALITY MODULE	PIN OUT ADAPTER
5300-1	6300-1	1K	256x4	OC	16	909-1226-1	715-1035-1	PM9037	PA16-1
5301-1	6301-1	1K	256x4	TS	16	909-1226-1	715-1035-1	PM9037	PA16-1
5305-1	6305-1	2K	512x4	OC	16	909-1226-1	715-1035-2	PM9037	PA16-1
5306-1	6306-1	2K	512x4	TS	16	909-1226-1	715-1035-2	PM9037	PA16-1
5308-1	6308-1	2K	256x8	OC	20	909-1226-1	715-1028-1	PM9037	PA20-2
5309-1	6309-1	2K	256x8	TS	20	909-1226-1	715-1028-1	F M9037	PA20-2
5330-1	6330-1	¼K	32x8	OC	16	909-1226-1	715-1046	PM9037	PA16-2
5331-1	6331-1	¼K	32x8	TS	16	909-1226-1	715-1046	PM9037	PA16-2
5335-1	6335-1	2K	256x8	OC	24	909-1226-1	715-1033-1	PM9037	PA24-1
5336-1	6336-1	2K	256x8	TS	24	909-1226-1	715-1033-1	PM9037	PA24-1
5340-1	6340-1	4K	512x8	OC	24	909-1226-1	715-1033-2	PM9037	PA24-1
5341-1	6341-1	4K	512x8	TS	24	909-1226-1	715-1033-2	PM9037	PA24-1
5348-1	6348-1	4K	512x8	OC	20	909-1226-1	715-1064	PM9037	PA20-2
5349-1	6349-1	4K	512x8	TS	20	909-1226-1	715-1064	PM9037	PA20-2
5350-1	6350-1	4K	1Kx4	OC	18	909-1226-1	715-1036	PM9037	PA18-1
5351-1	6351-1	4K	1Kx4	TS	18	909-1226-1	715-1036	PM9037	PA18-1
5352-1	6352-1	4K	1Kx4	OC	18	909-1226-1	715-1039-3	PM9037	PA18-2
5353-1	6353-1	4K	1Kx4	TS	18	909-1226-1	715-1039-3	PM9037	PA18-2
5380-1	6380-1	8K	1Kx8	OC	24	909-1226-1	715-1033-3	PM9037	PA24-1
5381-1	6381-1	8K	1Kx8	TS	24	909-1226-1	715-1033-3	PM9037	PA24-1
5384-1		8K	1Kx8	OC	24	909-1226-1	715-1033-3	PM9037	PA24-1
5385-1		8K	1Kx8	TS	24	909-1226-1	715-1033-3	PM9037	PA24-1

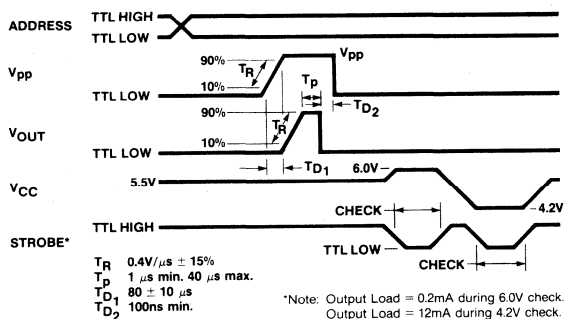
Programming Parameters

Do not test these parameters or you may program the device.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
t_R	Rise Time of Program Pulse Applied Data Out or Program Pin		0.34	0.40	0.46	V/ μ S
VCCP	VCC Required During Programming		5.40	5.50	5.60	V
IOLV ₁	Output Current Required During Verification	Chip Enabled T _A = +25°C, V _{CC} = 4.2V	11	12	13	mA
IOLV ₂	Output Current Required During Verification	Chip Enabled T _A = +25°C, V _{CC} = 6.0V	0.10	0.2	0.30	mA
MDC	Maximum Duty Cycle During Automatic Programming of Program Pin and Output Pin	t _P /t _C			25	%
V _{pp}	Required Programming Voltage on Program Pin		27		33	V
V _{out}	Required Programming Voltage on Output Pin		20		26	V
I _L	Current Limit of Power Supply Feeding Program Pin and Output During Programming	V _{pp} = 33V, V _{out} = 26V, V _{CC} = 5.50V	240			mA
t _{D1}	Required Time Delay Between Disabling Memory Output and Application of Output Programming Pulse	Measure at 10% Levels	70	80	90	μ S
t _{D2}	Required Time Delay Between Removal of Programming Pulse and Enabling Memory Output	Measure at 10% Levels	100			ns



Programming Timing



Programming Speed

Typically, fuses will blow on the rise time of the first pulse. In automated programmers which must copy devices in a short time because of the production requirements, the following pulse and voltage sequences have been found to maximize reliability, programming yield and throughput. The device should be verified after each programming attempt and be advanced to the next bit if the device has programmed.

PULSE NUMBER	PROGRAM PIN VOLTAGE	OUTPUT VOLTAGE
1 to 3	27V	20V
4 to 6	30V	23V
7 to 9	33V	26V

NOTE: The 5330/1 and 6330/1 do not have a program pin. For these devices the output only is used in programming a particular selected bit and the device must be in the disabled state.

Commercial Programmers

MMI PROMs are designed and tested to give a programming yield greater than 95%. Field reports agree with this expectation. Several companies make commercial programmers which will properly program MMI PROMs. MMI makes it a practice to review these commercial programmers and works closely with the manufacturers to maintain a high programming yield and high reliability of programmed parts. If your programming procedures have a lower yield, then check your programmer. It may not be properly calibrated for the "Dash-One" series of PROMs—53xx-1 and 63xx-1. Calibration must agree with the timing charts supplied in this publication. Monolithic Memories performs a systematic review of commercially available programmers, and will periodically issue a list of approved models.

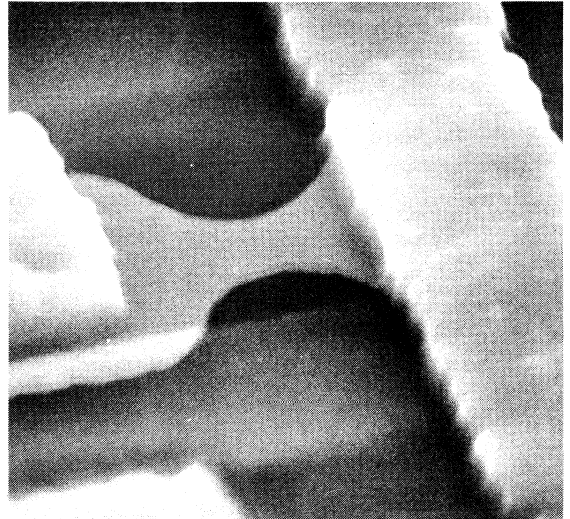
Programming is final manufacturing—it must be quality-controlled. Equipment must be calibrated as a regular routine, ideally under the actual conditions of use. The best method involves a storage scope, with DC current probes clamped over the external wires to the program pin and the output pin. The current should not be limited at a value less than 240mA. This can be checked by using a 50-ohm resistor as a load. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltages must meet published specifications for the device.

Remember—The best PROMs available can be made unreliable by improper programming techniques.

High Performance Schottky PROMs

Features/Benefits

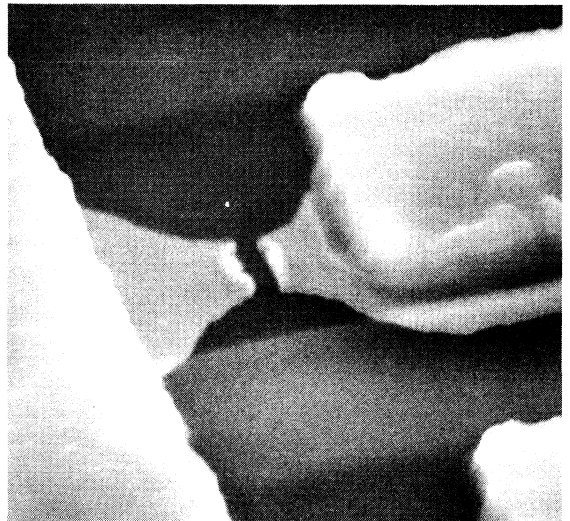
- New advanced platinum silicide Schottky process allows designs with fastest speeds over operating temperature ranges
- Four Generic Families
 - Schottky "S" for highest speed
 - Low power "LS" for with standard AC performance
 - Power switched "PS" low standby power in the disabled state
 - Registered "RA/RS" - edge triggered "D" registers for todays pipelined architectures
- Low voltage programming with reliable titanium-tungsten fuses
- Upwards pin compatibility in industry standard pin outs (most of which were first introduced by MMI in our Standard Performance PROM family).



Unblown Fuse

New Programming Technique:

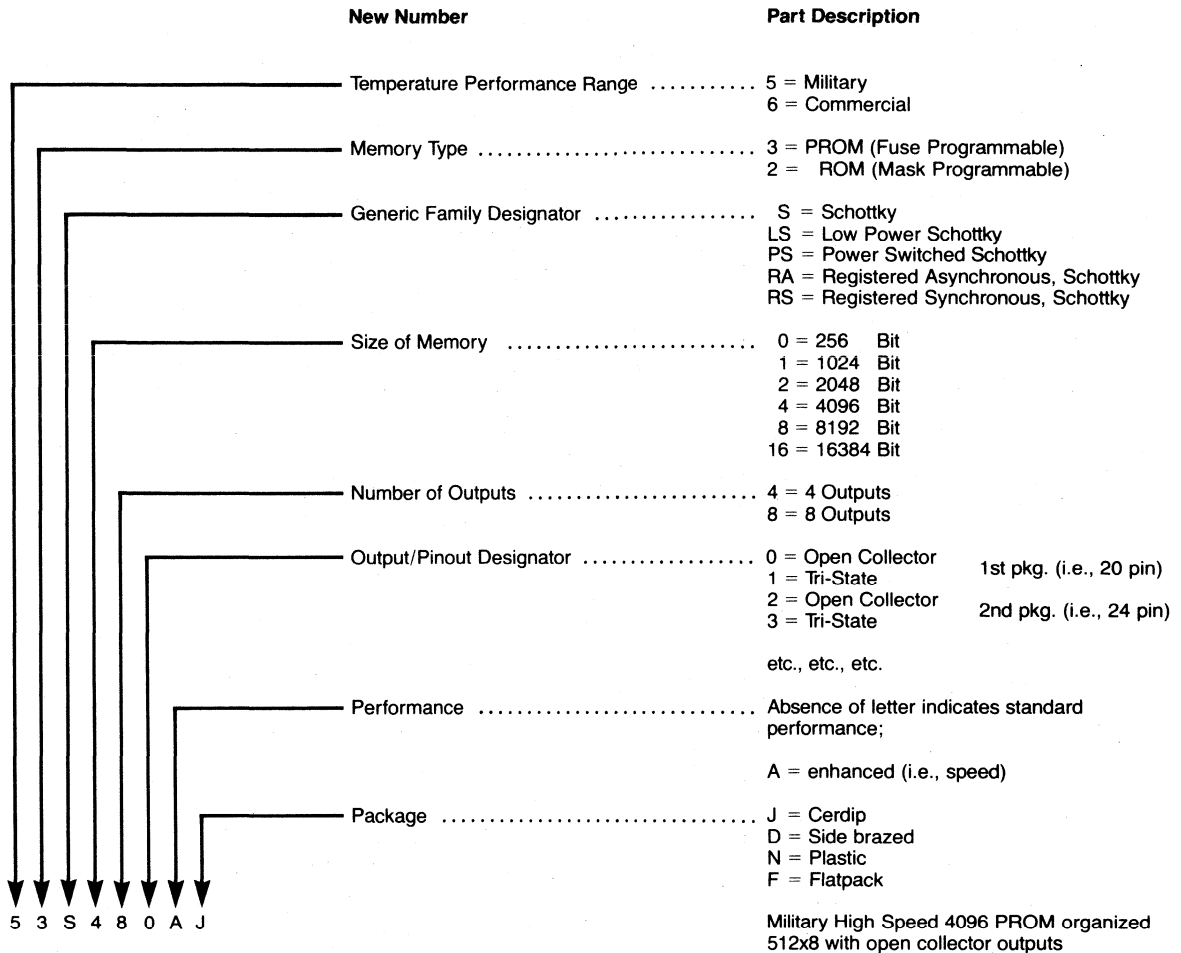
Our new HIGH Performance PROMs use an elevated voltage at V_{CC} instead of using a separate programming pin (one of the enables) as in the Standard Performance PROMs using nichrome fuses. Changes in the internal circuitry were made to optimize speed and accordingly the unblown fuse represents a LOW at the output. When a fuse is programmed it reflects a high at the output.*



Blown Fuse

* NOTE: This is opposite to that of our standard performance Schottky PROMs using nichrome fuses.

High Performance Schottky PROMs



Military High Speed 4096 PROM organized 512x8 with open collector outputs

MMI Part Numbering System

The new system approaches part numbering using the method of keying important attributes of the device. The military/commercial and PROM/ROM numbering system is preserved i.e., 5/6 - 3/2. These two digits are separated from the actual device number by a technology/configuration designator using letters.

- "S" = Schottky
- "LS" = Low Power Schottky
- "PS" = Power Switched
- "RA" = Registered Asynchronous
- "RS" = Registered Synchronous

The number following this code describes....

1. The size of the memory (bits)
2. The memory organization by specifying the number of outputs
3. Output configuration and pin out/package options

If a higher performance part co-exists i.e., faster speed, then a suffix letter (A) is added to distinguish between the two devices. The normal package letter designator follows last as is custom.

High Performance Schottky Generic PROM Family 53/63SXXX

Features/Benefits

- Highest speed Schottky PROM family available
- Advanced Schottky processing
- Pin compatible with standard Schottky PROMs and ROMs, 53/63XX-1, 52/62XX-1
- PNP inputs for low input current
- Compatible pin configurations for upward expansion
- 4-bit-wide and 8-bit-wide for byte oriented applications

Applications

- Microprogram control store
- Microprocessor program store
- Look up table
- Character generator
- Random logic
- Code converter

Description

The 53/63SXXX series generic PROM family offers the fastest and widest selection of sizes and organizations available in the industry. The 4-bit-wide PROMs range from 256x4 to 4096x4 and feature upward/downward pin out compatibility in the space saving 16, 18 and 20 pin packages. The 8-bit-wide PROMs range from 32x8 to 2048x8 in a wide selection of package sizes. All PROMs have the same programming specifications allowing a single generic programmer.

The family features low input current PNP inputs, full Schottky clamping and three-state and open collector outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on chip circuitry and extra fuses provide pre-programming testing which assure high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

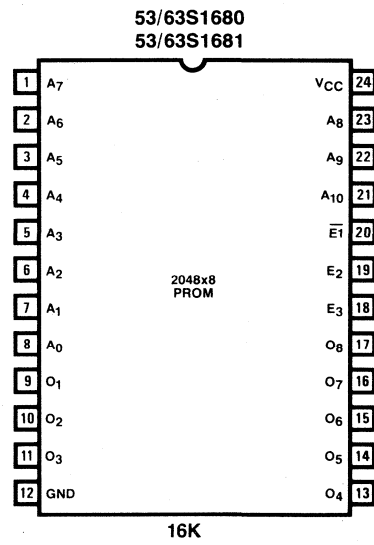
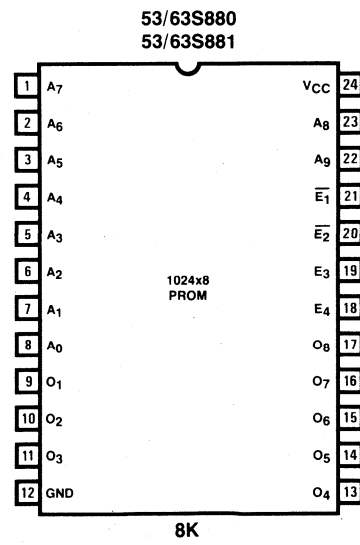
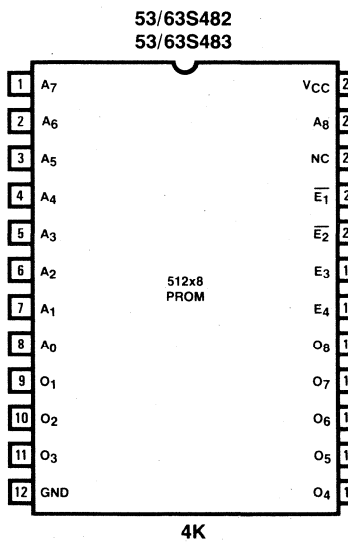
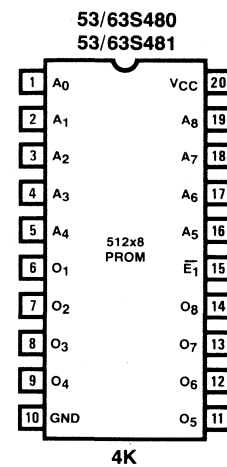
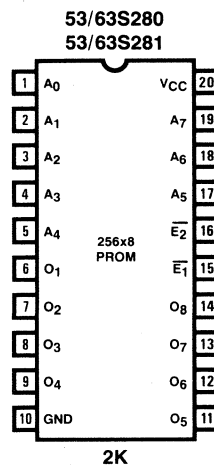
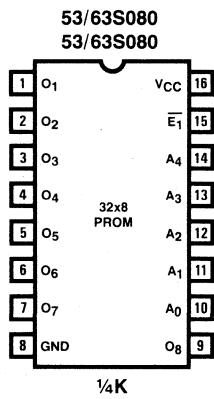
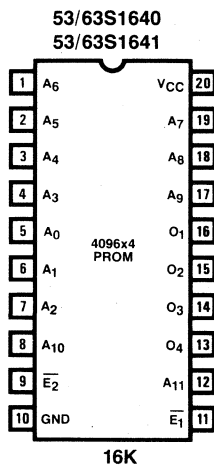
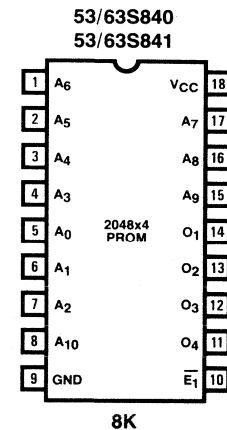
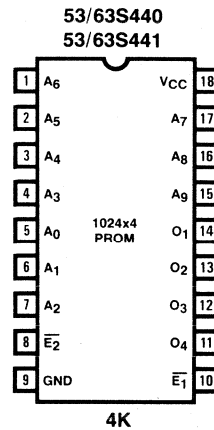
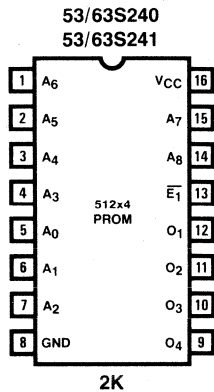
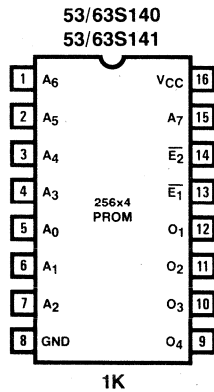
High Performance Generic PROM Selection Guide

MEMORY			PACKAGE		DEVICE TYPE	
SIZE	ORGANIZATION		PINS	TYPE	0°C to +75°C	-55°C to +125°C
¼K	32x8	OC	16	J,N,F	63S080*	53S080*
		TS			63S081*	53S081*
1K	256x4	OC	16	J,N,F	63S140	53S140
		TS			63S141	53S141
2K	512x4	OC	16	J,N,F	63S240	53S240
		TS			63S241	53S241
2K	256x8	OC	20	J,N	63S280*	53S280*
		TS			63S281*	53S281*
4K	1024x4	OC	18	J,N,F	63S440	53S440
		TS			63S441	53S441
4K	512x8	OC	20	J,N	63S480*	53S480*
		TS			63S481*	53S481*
4K	512x8	OC	24	J,N,F	63S482*	53S482*
		TS			63S483*	53S483*
8K	2048x4	OC	18	J,N,F	63S840*	53S840*
		TS			63S841*	53S841*
8K	1024x8	OC	24	J,N,F	63S880*	53S880*
		TS			63S881*	53S881*
16K	4096x4	OC	20	J,N	63S1640*	53S1640*
		TS			63S1641*	53S1641*
16K	2048x8	OC	24	J,N,F	63S1680*	53S1680*
		TS			63S1681*	53S1681

* Preliminary Data

Note: This is not a final specification. Some limits of characteristics are subject to change.

Pin Configurations



2

NOTE: Pin assignments for ceramic (J package), plastic (N package) and flat pack (F package) are the same.

Absolute Maximum Ratings

	Operating	Program
Supply voltage V_{CC}	-0.5V to 7V	12V
Input voltage	-1.5V to 5.5V	12V
Off-state output voltage	-1.5V to 5.5V	12V
Storage temperature range	-65°C to 150°C	

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.75	5.00	5.25	V
I_{OH}	High level output current			-2.0			-6.5	mA
I_{OL}	Low level output current			16			16	mA
T_A	Operating free air temperature	-55		125	0		75	°C

Electrical Characteristics

Over Recommended Operating Free Air Temperature Range

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.8	V
V_{IC}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18\text{mA}$			-1.2	V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V},$ $V_{IL} = 0.8\text{V}, I_{OL} = \text{MAX}$	53S		0.5	V
			63S		0.45	
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5\text{V}$			1.0	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4\text{V}$			25	μA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4\text{V}$			-250	μA
C_I	Input capacitance	$V_{CC} = 5.0\text{V}, f = 1\text{MHz}$	$V_I = 2.0\text{V}$	4		pF
C_O	Output capacitance	$T_A = 25^\circ\text{C}$	$V_O = 2.0\text{V}$	6		pF
I_{CC}	Supply current	$V_{CC} = \text{MAX}$ All inputs grounded All outputs open	080,081		65	mA
			140,141		78 120	
			240,241		85 130	
			280,281,480,481		105	
			440,441,840,841		110 170	
			880,881,1640,1641		117	
			1680,1681		124	

OPEN COLLECTOR OUTPUT CURRENT

I_{CEX}	Output leakage current	$V_{CC} = \text{MAX}, V_O = 2.4\text{V}$	50	μA
		$V_{CC} = \text{MAX}, V_O = 5.5\text{V}$	100	μA

THREE STATE OUTPUT ONLY

V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V},$ $V_{IL} = 0.8\text{V}, I_{OH} = \text{MAX}$	2.4	V
I_{OZH}	Off-state output current high-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2\text{V},$ $V_O = 2.4\text{V}$		100 μA
I_{OZL}	Off-state output current low-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2\text{V},$ $V_O = 0.4\text{V}$		-100 μA
I_{OS}	Short-circuit output current	$V_{CC} = \text{MAX}, V_O = 0\text{V}$	-30	-100 mA

Switching Characteristics

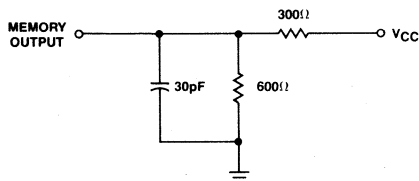
MAX = Over Recommended Ranges of T_A and V_{CC}

TYP = @ 5.0V V_{CC} , 25°C T_A

DEVICE TYPE	$t_{AA}(ns)$ ADDRESS ACCESS TIME		$t_{EA}(ns)$ ENABLE ACCESS TIME		$t_{ER}(ns)$ ENABLE RECOVERY TIME	
	TYP	MAX	TYP	MAX	TYP	MAX
63S080,081	13		13		16	
53S080,081	13		13		16	
63S140,141	28	45	13	25	16	25
53S140,141	28	55	13	30	16	30
63S240,241	30	45	13	25	16	25
53S240,241	30	55	13	30	16	30
63S280,281	30		13		16	
53S280,281	30		13		16	
63S440,441	32	50	13	25	16	25
53S440,441	32	60	13	30	16	30
63S480,1,2,3	30		13		16	
53S480,1,2,3	30		13		16	
63S840,841	38		13		16	
53S840,841	38		13		16	
63S880,881	34		13		16	
53S880,881	34		13		16	
63S1640,1641	46		13		16	
53S1640,1641	46		13		16	
63S1680,1681	46		13		16	
63S1680,1681	46		13		16	

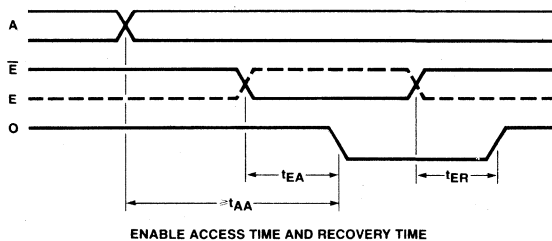
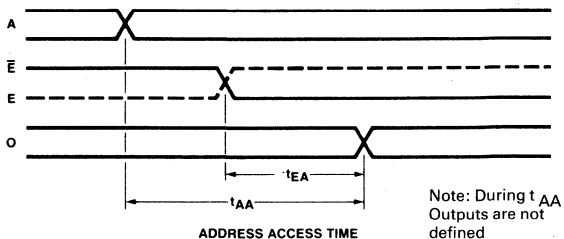
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Standard Test Load



Input Pulse Amplitude 3.0V
 Input Rise and Fall Times 5ns from 1.0V to 2.0V
 Measurements Made at 1.5V

Definition of Waveforms



High Performance Low Power Schottky Generic PROM Family 53/63LSXXX

Features/Benefits

- Largest generic low power Schottky PROM family available
- Advanced Schottky processing using ion implanted for low power and high speed
- Pin compatible with standard Schottky PROMs and ROMs, 53/63XX-1, 52/62XX-1
- PNP inputs for low input current
- Compatible pin configurations for upward expansion
- 4-bit-wide and 8-bit-wide for byte oriented applications

Applications

- Microprogram control store
- Microprocessor program store
- Look up table
- Character generator
- Random logic
- Code converter

Description

The 53/63LSXXX series generic PROM family offers the lowest power and fastest speeds available in the industry. The 4-bit-wide PROMs range from 256x4 to 2048x4 and feature upward/downward pin out compatibility in the space saving 16 and 18 pin packages. The 32x8 PROM is also included in our low power Schottky family and a typical access time of 24 ns makes it a natural programmable logic element choice. Other 8-Bit-Wide PROMs are available up to 2048x8. All PROMs have the same programming specifications allowing a single generic programmer.

The family features low input current PNP inputs, full Schottky clamping and three-state and open collector outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on chip circuitry and extra fuses provide pre-programming testing which assure programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military range.

High Performance Low Power Schottky Generic PROM Selection Guide

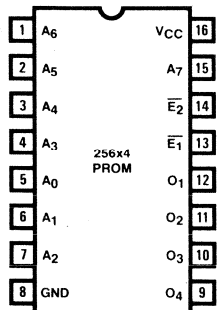
MEMORY			PACKAGE		DEVICE TYPE	
SIZE	ORGANIZATION		PINS	TYPE	0°C to +75°C	-55°C to +125°C
¼K	32x8	OC	16	J,N,F	63LS080*	53LS080*
		TS			63LS081*	53LS081*
1K	256x4	OC	16	J,N,F	63LS140	53LS140
		TS			63LS141	53LS141
2K	512x4	OC	16	J,N,F	63LS240	53LS240
		TS			63LS241	53LS241
2K	256x8	OC	20	J,N	63LS280*	53LS280*
		TS			63LS281*	53LS281*
4K	1024x4	OC	18	J,N,F	63LS440	53LS440
		TS			63LS441	53LS441
4K	512x8	OC	20	J,N	63LS480*	53LS480*
		TS			63LS481*	53LS481*
4K	512x8	OC	24	J,N,F	63LS482*	53LS482*
		TS			63LS483*	53LS483*
8K	2048x4	OC	18	J,N,F	63LS840*	53LS840*
		TS			63LS841*	53LS841*
8K	1024x8	OC	24	J,N,F	63LS880*	53LS880*
		TS			63LS881*	53LS881*
16K	4096x4	OC	20	J,N	63LS1640*	53LS1640*
		TS			63LS1641*	53LS1641*
16K	2048x8	OC	24	J,N,F	63LS1680*	53LS1680*
		TS			63LS1681*	53LS1681*

* Preliminary Data

Note: This is not a final specification. Some limits of characteristics are subject to change.

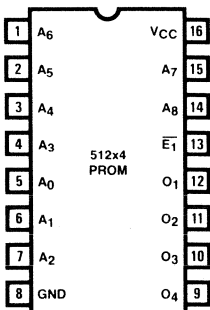
Pin Configurations

53/63LS140
53/63LS141



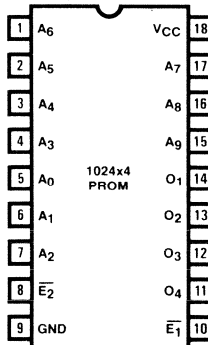
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53/63LS240
53/63LS241



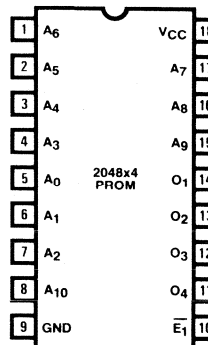
2K

53/63LS440
53/63LS441



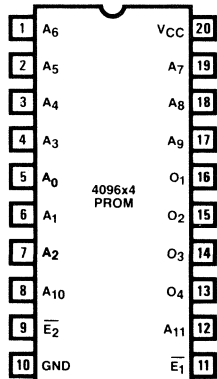
4K

53/63LS840
53/63LS841



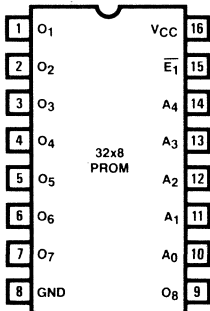
8K

53/63LS1640
53/63LS1641



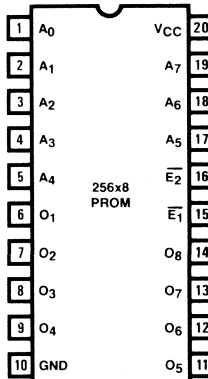
16K

53/63LS080
53/63LS081



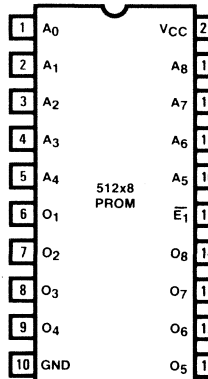
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53/63LS280
53/63LS281



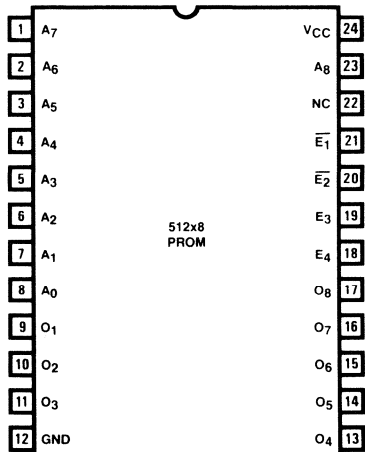
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53/63LS480
53/63LS481



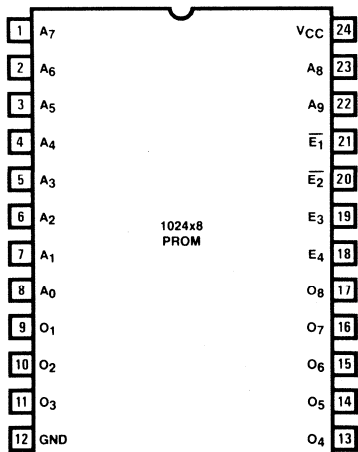
4K

53/63LS482
53/63LS483



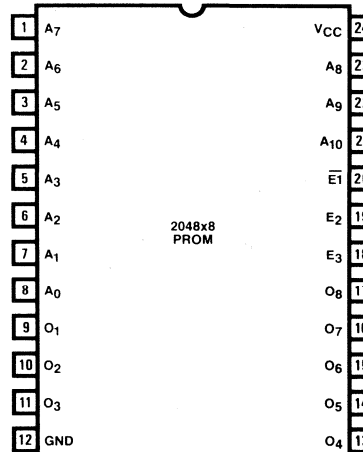
4K

53/63LS880
53/63LS881



8K

53/63LS1680
53/63LS1681



16K

2

NOTE: Pin assignments for ceramic (J package), plastic (N package) and flat pack (F package) are the same

Absolute Maximum Ratings

Supply voltage V_{CC}	Operating	Program
Input voltage	-0.5V to 7V	12V
Off-state output voltage	-1.5V to 5.5V	12V
Storage temperature range	-1.5V to 5.5V	12V
	-65°C to 150°C	

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.75	5.00	5.25	V
I_{OH}	High level output current			-2.0			-6.5	mA
I_{OL}	Low level output current			12			16	mA
T_A	Operating free air temperature	-55		125	0		75	°C

Electrical Characteristics

Over Recommended Operating Free Air Temperature Range

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
V_{IH}	High-level input voltage		2		V_{CC}	V	
V_{IL}	Low-level input voltage		0		0.8	V	
V_{IC}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18\text{mA}$			-1.2	V	
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V},$ $V_{IL} = 0.8\text{V}, I_{OL} = \text{MAX}$	53LS		0.5	V	
			63LS		0.45		
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5\text{V}$			1.0	mA	
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4\text{V}$			25	μA	
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4\text{V}$			-250	μA	
C_I	Input capacitance	$V_{CC} = 5.0\text{V}, f = 1\text{MHz}$	$V_I = 2.0\text{V}$		4	pF	
C_O	Output capacitance	$T_A = 25^\circ\text{C}$	$V_O = 2.0\text{V}$		6	pF	
I_{CC}	Supply current	$V_{CC} = \text{MAX}$ All inputs grounded All outputs open	080,081		35	mA	
			140,141		46		65
			240,241		49		70
			280,281,480,481		55		
			440,441,840,841		60		85
			880,881,1640,1641		63		
1680,1681		67					

OPEN COLLECTOR OUTPUT CURRENT

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{CEX}	Output leakage current	$V_{CC} = \text{MAX}, V_O = 2.4\text{V}$		50	μA
		$V_{CC} = \text{MAX}, V_O = 5.5\text{V}$		100	μA

THREE STATE OUTPUT ONLY

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V},$ $V_{IL} = 0.8\text{V}, I_{OH} = \text{MAX}$	2.4		V
I_{OZH}	Off-state output current high-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2\text{V},$ $V_O = 2.4\text{V}$		100	μA
I_{OZL}	Off-state output current low-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2\text{V},$ $V_O = 0.4\text{V}$		-100	μA
I_{OS}	Short-circuit output current	$V_{CC} = \text{MAX}, V_O = 0\text{V}$	-30	-100	mA

Switching Characteristics

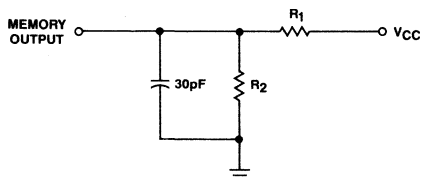
MAX = Over Recommended Ranges of T_A and V_{CC}

TYP = 5.0V V_{CC} , 25°C T_A

DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME		t_{EA} (ns) ENABLE ACCESS TIME		t_{ER} (ns) ENABLE RECOVERY TIME	
	TYP	MAX	TYP	MAX	TYP	MAX
63LS080,081	24		15		21	
53LS080,081	24		15		21	
63LS140,141	40	55	15	30	21	30
53LS140,141	40	65	15	35	21	35
63LS240,241	42	60	15	30	21	30
53LS240,241	42	70	15	35	21	35
63LS280,281	51		15		21	
53LS280,281	51		15		21	
63LS440,441	53	65	15	30	21	30
53LS440,441	53	75	15	35	21	35
63LS480,1,2,3	51		15		21	
53LS480,1,2,3	51		15		21	
63LS840,841	62		15		21	
53LS840,841	62		15		21	
63LS880,881	55		15		21	
53LS880,881	55		15		21	
63LS1640,1641	66		15		21	
53LS1640,1641	66		15		21	
63LS1680,1681	66		15		21	
53LS1680,1681	66		15		21	

2

Standard Test Load



Input Pulse Amplitude 3.0V
Input Rise and Fall Times 5ns from 1.0V to 2.0V
Measurements Made at 1.5V

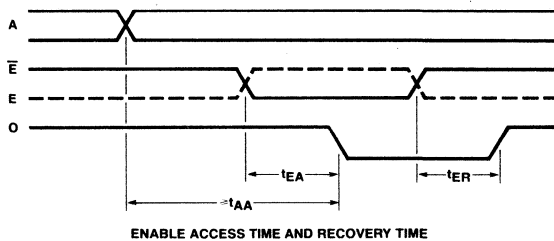
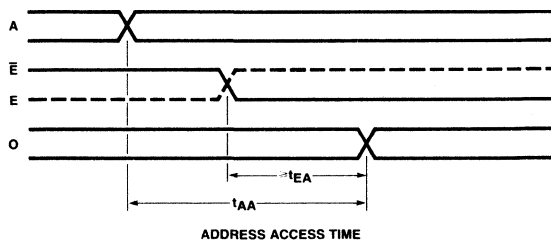
$R_1 = 300\Omega$ for 63LSXXX

$R_2 = 600\Omega$ for 63LSXXX

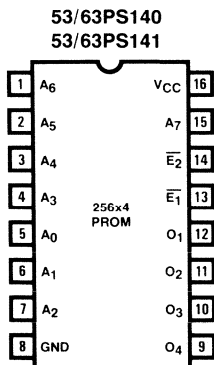
$R_1 = 375\Omega$ for 53LSXXX

$R_2 = 750\Omega$ for 53LSXXX

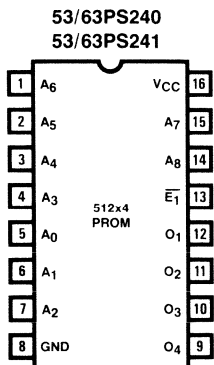
Definition of Waveforms



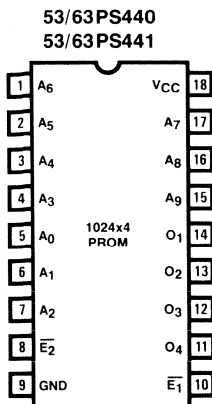
Pin Configurations



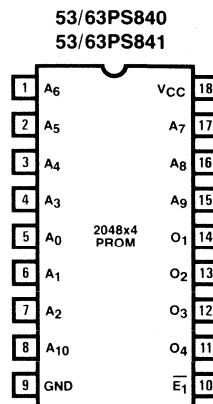
1K



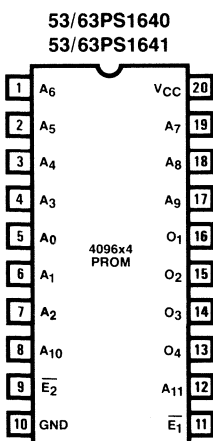
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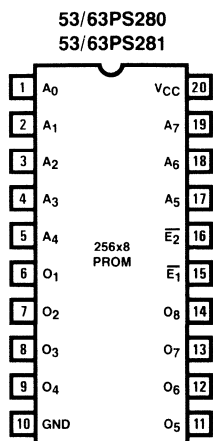
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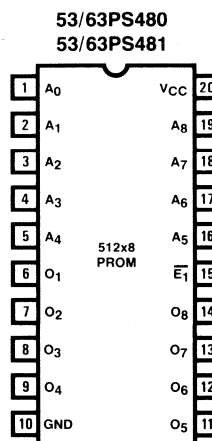
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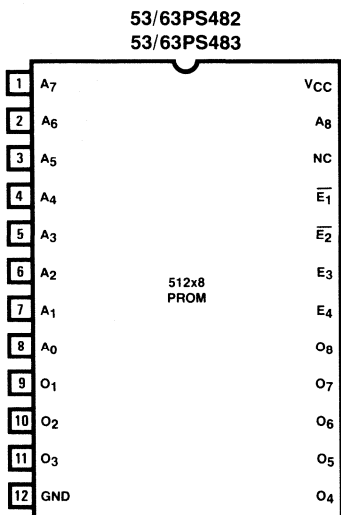
16K



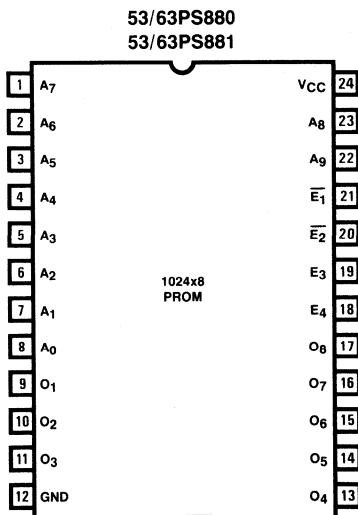
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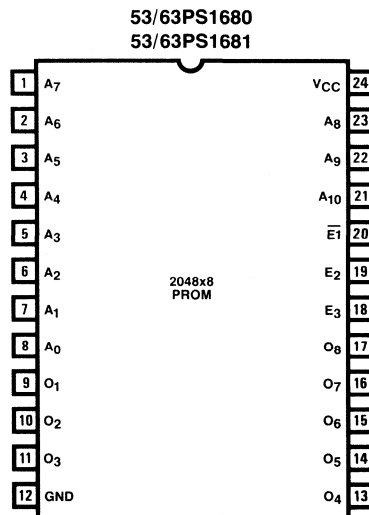
4K



4K



8K



16K

NOTE: Pin assignments for ceramic (J package), plastic (N package) and flat pack (F package) are the same.



Absolute Maximum Ratings

Supply voltage V_{CC}	Operating	Program
Input voltage	-0.5V to 7V	12V
Off-state output voltage	-1.5V to 5.5V	12V
Storage temperature range	-1.5V to 5.5V	12V
	-65°C to 150°C	

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.75	5.00	5.25	V
I_{OH}	High level output current			-2.0			-6.5	mA
I_{OL}	Low level output current			16			16	mA
T_A	Operating free air temperature	-55		125	0		75	°C

Electrical Characteristics**Over Recommended Operating Free Air Temperature Range**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.8	V
V_{IC}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18\text{mA}$			-1.2	V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V},$ $V_{IL} = 0.8\text{V}, I_{OL} = \text{MAX}$	53PS		0.5	V
			63PS		0.45	
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5\text{V}$			1.0	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4\text{V}$			25	μA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4\text{V}$			-250	μA
C_I	Input capacitance	$V_{CC} = 5.0\text{V}, f = 1\text{MHz}$		4		pF
C_O	Output capacitance	$T_A = 25^\circ\text{C}$		6		pF

OPEN COLLECTOR OUTPUT CURRENT

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CEX}	Output leakage current	$V_{CC} = \text{MAX}, V_O = 2.4\text{V}$			50	μA
		$V_{CC} = \text{MAX}, V_O = 5.5\text{V}$			100	μA

THREE STATE OUTPUT ONLY

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V},$ $V_{IL} = 0.8\text{V}, I_{OH} = \text{MAX}$	2.4			V
I_{OZH}	Off-state output current high-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2\text{V},$ $V_O = 2.4\text{V}$			100	μA
I_{OZL}	Off-state output current low-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2\text{V},$ $V_O = 0.4\text{V}$			-100	μA
I_{OS}	Short-circuit output current	$V_{CC} = \text{MAX}, V_O = 0\text{V}$	-30		-100	mA

Switching Characteristics

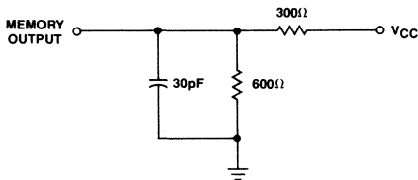
MAX = Over Recommended Ranges of T_A and V_{CC}

TYP = 5.0V V_{CC} , 25°C T_A

DEVICE TYPE	I_{CC}						$t_{AA}(ns)$ ADDRESS ACCESS TIME		$t_{EA}(ns)$ ENABLE ACCESS TIME		$t_{ER}(ns)$ ENABLE RECOVERY TIME	
	ENABLED		DISABLED				TYP	MAX	TYP	MAX	TYP	MAX
	TYP	MAX	TYP		MAX							
			OC	TS	OC	TS						
63PS140,141	78		20	25			27		27		16	
53PS140,141	78		20	25			27		27		16	
63PS240,241	85		20	25			30		30		16	
53PS240,241	85		20	25			30		30		16	
63PS280,281	105		25	30			33		33		16	
53PS280,281	105		25	30			33		33		16	
63PS440,441	105		20	25			33		33		16	
53PS440,441	105		20	25			33		33		16	
63PS480,1,2,3	105		25	30			36		36		16	
53PS480,1,2,3	105		25	30			36		36		16	
63PS840,841	110		20	25			39		39		16	
53PS840,841	110		20	25			39		39		16	
63PS880,881	117		25	30			39		39		16	
53PS880,881	117		25	30			39		39		16	
63PS1640,1641	117		25	30			45		45		16	
53PS1640,1641	117		25	30			45		45		16	
63PS1680,1681	124		30	35			48		48		16	
53PS1680,1681	124		30	35			48		48		16	

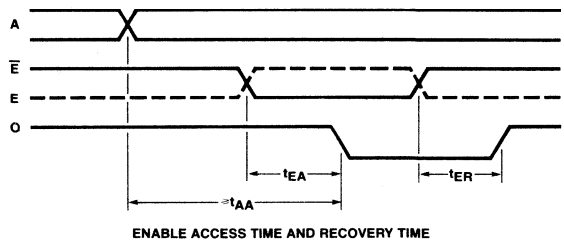
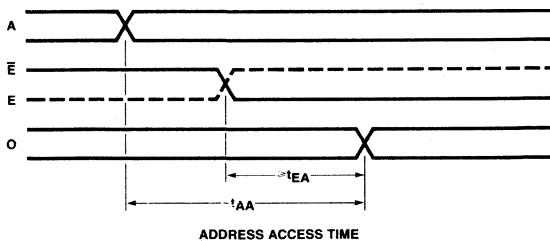
2

Standard Test Load



Input Pulse Amplitude 3.0V
 Input Rise and Fall Times 5ns from 1.0V to 2.0V
 Measurements Made at 1.5V

Definition of Waveforms



High Performance Registered Schottky —4-Bit-Wide Generic PROM Family 53/63RAXXX, 53/63RSXXX

Features/Benefits

- Largest generic PROM family available incorporating edge triggered "D" registers.
- Advanced Schottky processing.
- 4-bit-wide in 18 and 20 pin Skinny DIPs™ for high board density.
- Synchronous enable allow easy busing of outputs for word expansion.
- Lower system package counts.
- Lower system power.
- Faster cycle times.
- 25ns clock to output and 40ns address set-up times guaranteed over commercial specification.
- 24mA I_{OL} output drive capability.

Applications

- Pipelined microprogramming
- State sequencers
- Next address generation
- Mapping PROM

Description

A family of registered PROMs offers new savings for designers of pipelined microprogrammable systems. The wide instruction register, which holds the microinstruction during execution, is now incorporated into the PROM chip.

Edge Triggered Register

The PROM output is loaded into a 4-bit register on the rising edge of the clock. The use of the term "register" is to be distinguished from the term "latch," in that a register contains master slave flip-flops and the latch contains gated flip-flops. The advantages of using a register are that system timing is simplified, and faster micro cycle times can be obtained.

The output of the register is buffered by three-state drivers which are compatible with the new low-power Schottky three-state bus standard, i.e., I_{OL} is 24mA at V_{OL} of 0.5V.

The 4-bit-wide family in 18-pin and 20-pin packages feature either synchronous or asynchronous enables the synchronous enables and upwards pin compatibility. The synchronous enable powers up in the high impedance state and is used when more than one registered PROM is bused together to increase word length. All devices are specified over both commercial and military temperature ranges.

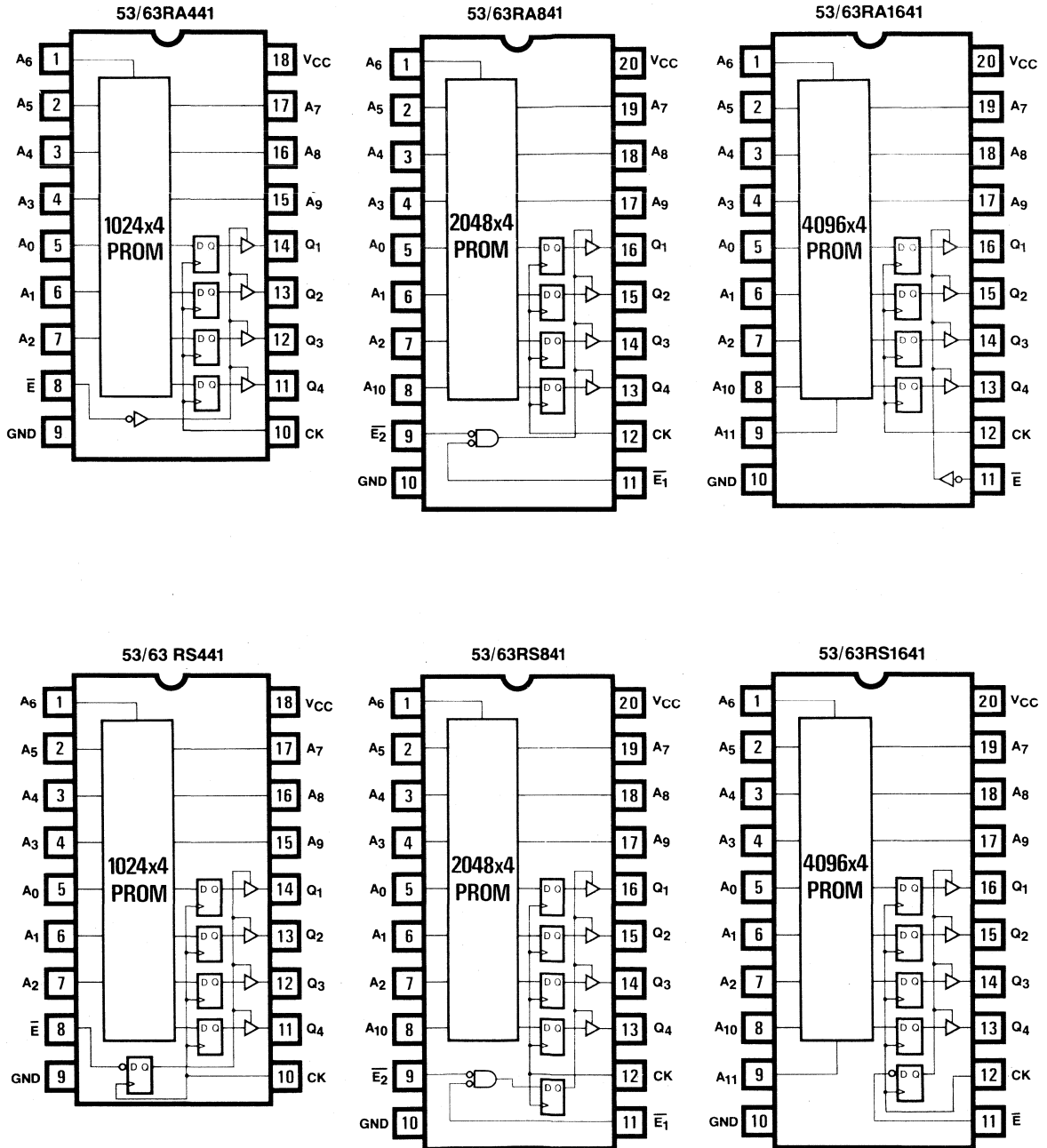
High Performance Generic PROM Selection Guide

MEMORY			PACKAGE		DEVICE TYPE	
SIZE	ORGANIZATION		PINS	TYPE	0°C to 75°C	-55°C to 125°C
4K	1024x4	ASYN	18	J,N,F	63RA441	53RA441
		SYN			63RS441	53RS441
8K	2048x4	ASYN	20	J,N	63RA841*	53RA841*
		SYN			63RS841*	53RS841*
16K	4096x4	ASYN	20	J,N	63RA1641*	53RA1641*
		SYN			63RS1641*	53RS1641*

* Preliminary Data

Note: This is not a final specification. Some limits of characteristics are subject to change.

Pin Configurations



2

Absolute Maximum Ratings

Supply voltage V_{CC}	Operating	Program
Input voltage	-5V to 7V	12V
Off-state output voltage	-1.5V to 5.5V	12V
Storage temperature	-1.5V to 5.5V	12V
	-65°C to 150°C	

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.75	5.00	5.25	V
I_{OH}	High-level output current			-2.0	2.4		-6.5	mA
I_{OL}	Low-level output current			16			24	mA
T_A	Operating free air temperature	-55		125	0		75	°C

Electrical Characteristics

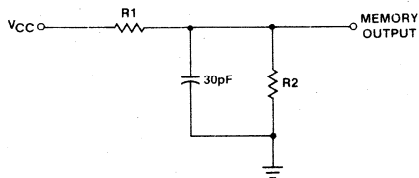
Over Recommended Operating Free Air Temperature Range

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT	
V_{IH}	High-level input voltage			2.0		V_{CC}	V	
V_{IL}	Low-level input voltage			0		0.8	V	
V_{IC}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18\text{mA}$				-1.2	V	
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V}, V_{IL} = 0.8\text{V}, I_{OH} = \text{MAX}$		2.4			V	
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V}, V_{IL} = 0.8\text{V}, I_{OL} = \text{MAX}$				0.5	V	
I_{OZH}	Off-state output current high-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2\text{V}, V_O = 2.4\text{V}$				100	μA	
I_{OZL}	Off-state output current low-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2\text{V}, V_O = 0.4\text{V}$				-100	μA	
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5\text{V}$				1.0	mA	
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4\text{V}$				25	μA	
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4\text{V}$				-250	μA	
I_{OS}	Short-circuit output current	$V_{CC} = \text{MAX}$		-30		-100	mA	
C_I	Input capacitance	$V_{CC} = 5.0\text{V}, f = 1\text{MHz}$			4	10	pF	
C_O	Output capacitance	$T_A = 25^\circ\text{C}$			6	12	pF	
I_{CC}	Supply current	441,	$V_{CC} = \text{MAX}$	All inputs GND All outputs open		125	180	mA
		841, 1641				130		

Switching CharacteristicsMin/Max = Over Recommended Ranges of T_A and V_{CC} Typ = 5.0V V_{CC} , 25°C T_A

SYMBOL	PARAMETER	DEVICE TYPE	MILITARY			COMMERCIAL		
			MIN	TYP	MAX	MIN	TYP	MAX
t_{pd}	Clock to output	(All)		18	30		18	25
t_{su}	Address set-up	RA441	45	30		40	30	
		RA841		35			35	
		RA1641		45			45	
		RS441	45	30		40	30	
		RS841		35			35	
		RS1641		45			45	
t_h	Address hold	(All)	0	-5		0	-5	
t_{pzx}	\bar{E} to output enable	(All "RA")		15	30		15	25
t_{pzx}	\bar{E} to output disable	(All "RA")		15	30		15	25
t_{pzx}	CK to output enable	(All "RS")		25	40		25	35
t_{pzx}	CK to output disable	(All "RS")		25	40		25	35
t_{su}	Enable set-up	(All "RS")	20	10		15	10	
t_h	Enable hold	(All "RS")	0	-5		0	-5	
t_w	Pulse width	(All)	20	12		20	12	
MAX	Maximum Clock frequency	RS/RA 441	20	24		25	33	
		RS/RA 841		29			33	
		RS/RA1641		25			25	

(See "Definition of Terms and Waveforms")

Standard Test Load

Input Pulse Amplitude 3.0V
 Input Rise and Fall Times 5ns from 1.0V to 2.0V
 Measurements Made at 1.5V
 Commercial $R_1 = 200\Omega$, $R_2 = 390\Omega$
 Military $R_1 = 300\Omega$, $R_2 = 600\Omega$

2

THE INFORMATION CONTAINED
HEREIN IS UNCLASSIFIED
DATE 08-14-2011 BY 60322
ARC SUBJECT TO OADR

High Performance Registered Schottky—8-Bit-Wide Generic PROM Family 53/63RAXXX

Features/Benefits

- Largest generic PROM family available incorporating edge triggered "D" registers.
- Advanced Schottky processing.
- 8-bit-wide output organizations in 24-pin Skinny DIPs™ (.300 mil wide).
- 25ns clock-to-output and 45ns address set-up times guaranteed over entire commercial specification.
- Preset and clock enable control functions for extra flexibility at the system level.
- Lower system level package count and power.
- 20mA output drive capability

Applications

- Pipelined microprogramming
- State sequencers
- Next address generation
- Mapping PROM

Description

An 8-bit-wide generic family of registered PROMs offers savings in printed circuit board space as well as additional control functions for designers of pipelined microprogrammable systems. The devices are packaged in a new space saving 24-pin Skinny DIP™ with 300 mil wide row spacing as well as the larger 600 mil wide package. The wide instruction register, which holds the microinstructions during execution, is incorporated into the PROM chip.

System Level Flexibility

For additional flexibility at the system level, clock enable and preset control pins have been added. All devices are upwards compatible to allow the designer to expand in the word direction by simply plugging in a larger register.

Registered PROM Selection Guide

MEMORY		PACKAGE		DEVICE TYPE	
SIZE	ORGANIZATION	PINS	TYPE	0°C to +75°C	-55°C to +125°C
2K	256x8 ASYN	24S*	J,N	63RA283	53RA283
4K	512x8 ASYN	24S*	J,N	63RA483	53RA483
8K	1024x8 ASYN	24S*	J,N	63RA883	53RA883
16K	2048x8 ASYN	24S*	J,N	63RA1683	53RA1683
2K	256x8 ASYN	24	J,N	63RA281	53RA281
4K	512x8 ASYN	24	J,N	63RA481	53RA481
8K	1024x8 ASYN	24	J,N	63RA881	53RA881
16K	2048x8 ASYN	24	J,N	63RA1681	53RA1681

Edge Triggered Register

The PROM output is loaded into an 8-bit register on the rising edge of the clock. The use of the term "register" is to be distinguished from the term "latch," in that a register contains master slave flip-flops and the latch contains gated flip-flops. The advantages of using a register are that system timing is simplified, and faster micro cycle times can be obtained.

The output of the register is buffered by three-state drivers which are compatible with the low-power Schottky three-state bus standard, i.e., I_{OL} is 20mA at V_{OL} of 0.5V.

Preset

When a microprogrammed system is powered up or initialized the asynchronous PRESET allows easy initialization of the register outputs to the desired "HIGH" state required for driving active LOW controls, i.e., write enable (\overline{WE}), \overline{CLEAR} , memory acknowledge, (\overline{MACK}), etc. A PRESET may also be issued to seek a "HOME" location, i.e., instruction fetch.

Clock Enable

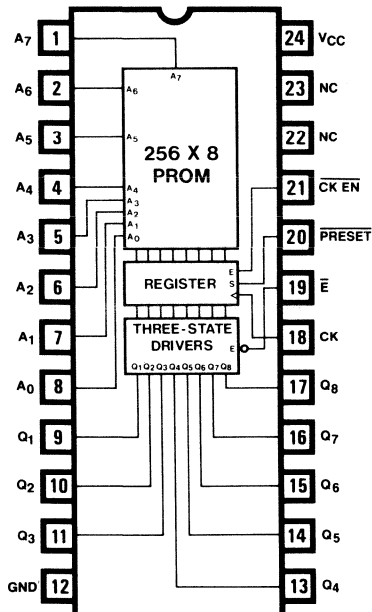
The clock enable function can be used to inhibit the clock from loading the next state (instruction) when CK EN is "HIGH" within the specified set-up time, t_{SU}. This allows the decision of whether or not to load the next state to be made at the latest possible point in the microcycle. This is an important feature in a micro-instruction loop which repeats the same micro-instruction until a specified branch condition allows a continue to the next micro-instruction.

Upwards Compatibility

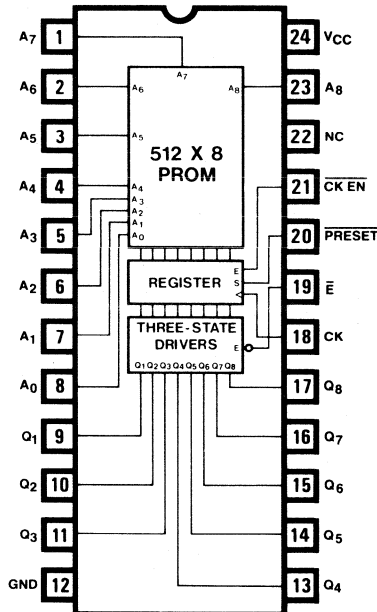
Designers have the flexibility to increase the size of their microprogram store in the word direction without any costly changes in board layout. All devices from the 256x8 up to the 2048x8 fit into the same socket. The use of one enable assures this concept of upwards compatibility and does not limit the user in word expansion since a large selection of word organizations are offered.

Logic Diagrams

53/63RA281/3

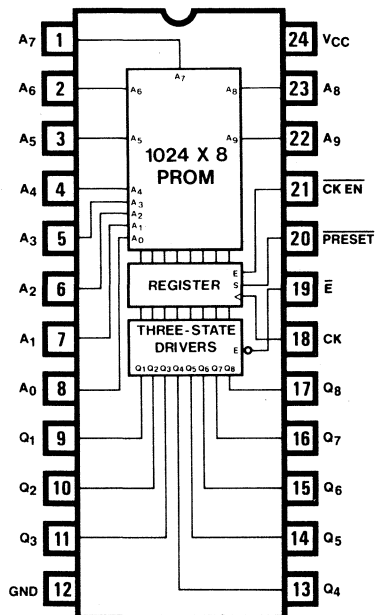


53/63RA481/3

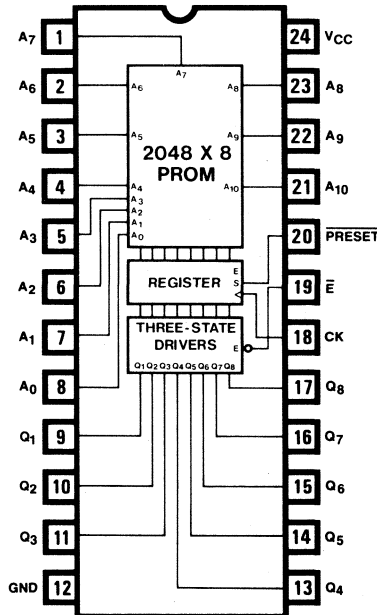


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53/63RA881/3



53/63RA1681/3



Functional Table

INPUT				OUTPUT	OPERATION
CLOCK ENABLE	CLOCK	PRESET	ENABLE		
X	X	L	L	H	Preset
X	X	L	H	Z	Preset
H	↑	H	L	Q	NOP
H	↑	H	H	Z	NOP
L	↑	H	L	PROM	Load Q with PROM
L	↑	H	H	Z	Load Q with PROM

Absolute Maximum Ratings

Operating/Program

Supply voltage V_{CC}	7V/12V
Input voltage	5.5V/12V
Off-state output voltage	5.5V/12V
Storage temperature range	-65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.75	5.00	5.25	V
I_{OH}	High-level output current			-2.0			-6.5	mA
I_{OL}	Low-level output current			16			20	mA
T_A	Operating free air temperature	-55		125	0		75	°C

Electrical Characteristics Over Recommended Operating Free Air Temperature Range

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2.0		V_{CC}	V
V_{IL}	Low-level input voltage		0.0		0.8	V
V_{IC}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18\text{mA}$			-1.2	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V}, V_{IL} = 0.8\text{V}, I_{OH} = \text{MAX}$	2.4			V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V}, V_{IL} = 0.8\text{V}, I_{OL} = \text{MAX}$			0.5	V
I_{OZH}	Off-state output current high-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2\text{V}, V_O = 2.4\text{V}$			100	μA
I_{OZL}	Off-state output current low-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2\text{V}, V_O = 0.4\text{V}$			-100	μA
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5\text{V}$			1.0	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4\text{V}$			25	μA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4\text{V}$			-250	μA
I_{OS}	Short-circuit output current	$V_{CC} = \text{MAX}$	-30		-100	mA
C_I	Input Capacitance	$V_{CC} = 5.0\text{V}, f = 1\text{MHz}$		$V_I = 2.0\text{V}$	4	pF
C_O	Output Capacitance	$T_A = 25^\circ\text{C}$		$V_O = 2.0\text{V}$	6	pF
I_{CC}	Supply current	281/3	$V_{CC} = \text{MAX}$ all inputs GND,		110	mA
		481/3, 881/3	All outputs open		125	
		1681/3			130	

Switching Characteristics

MIN/MAX = Over Recommended Ranges of T_A and V_{CC}

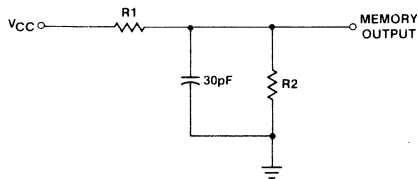
TYP = 5.0V, V_{CC} , 25°C T_A

(See Definition of Terms and Waveforms)

SYMBOL	PARAMETER	DEVICE TYPE	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Clock to output	All		20		20		ns	
t_{su}	Address set-up	'RA281/3		30		30		ns	
		'RA481/3		30		30			
		'RA881/3		35		35			
		'RA1681/3		45		45			
t_h	Address hold	All		-5		-5		ns	
t_{pd}	Preset to any Q	All		20		20		ns	
t_{su}	Preset to Clock set-up	All		10		10		ns	
t_{su}	Clock enable set-up	All		20		20		ns	
t_h	Clock enable hold	All		-5		-5		ns	
t_{PZX}	\bar{E} to output enable	All		20		20		ns	
t_{PXZ}	\bar{E} to output disable	All		20		20		ns	
t_w	Pulse width	All		12		12		ns	
f_{MAX}	Maximum clock frequency	RA281/3		40		40		MHz	
		RA481/3		40		40			
		RA881/3		33		33			
		RA1681/3		25		25			

(See "Definition of Terms and Waveforms")

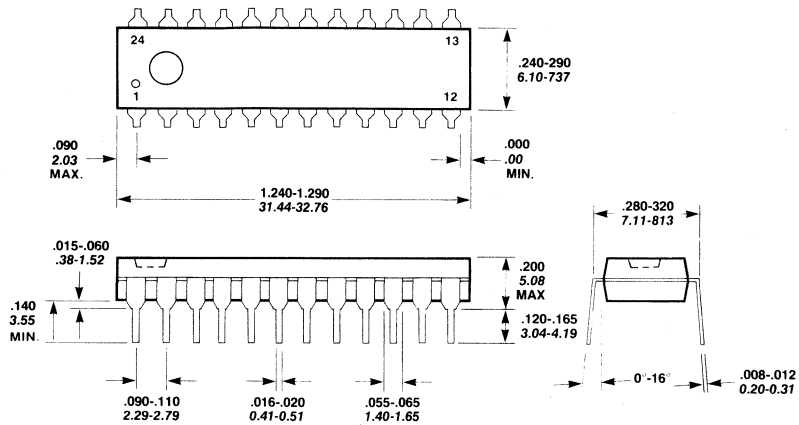
Standard Test Load



Input Pulse Amplitude 3.0V
 Input Rise and Fall Times 5ns from 1.0V to 2.0V
 Measurements Made at 1.5V
 Commercial $R_1 = 240\Omega$, $R_2 = 470\Omega$
 Military $R_1 = 300\Omega$, $R_2 = 600\Omega$

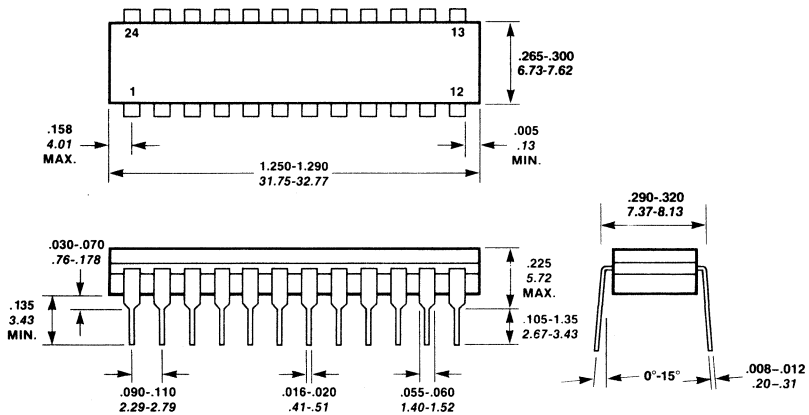
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N24S Plastic Kool "Skinny" DIP™



UNLESS OTHERWISE SPECIFIED:
 ALL DIMENSIONS MIN.-MAX. IN INCHES.
 ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS

J24S Ceramic "Skinny" DIP™



UNLESS OTHERWISE SPECIFIED:
 ALL DIMENSIONS MIN.-MAX. IN INCHES.
 ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.

High Performance Schottky PROM Programming Instructions

Device Description

All of the High Performance Generic Schottky PROM Families are manufactured with all outputs low in all storage locations. To produce a high at a particular word, a Titanium-Tungsten Fusible-Link must be changed from a low resistance to a high resistance. This procedure is called programming.

Programming Description

To program a particular bit normal TTL levels are applied to all inputs. Programming occurs when:

1. V_{CC} is raised to an elevated level.
2. The output to be programmed is raised to an elevated level.
3. The device is enabled.

In order to avoid misprogramming the PROM only one output at a time is to be programmed. Outputs not being programmed should be left open.

Programming Sequence

The sequence of programming conditions is critical and must occur in the following order:

1. Select the appropriate address with chip disabled
2. Increase V_{CC} to programming voltage
3. Increase appropriate output voltage to programming voltage
4. Enable chip for programming pulse width
5. Decrease V_{OUT} and V_{CC} to normal levels

Programming Timing

In order to insure the proper sequence, a delay of 100ns or greater must be allowed between steps. The enabling pulse must not occur less than 100ns after the output voltage reaches programming level. The rise time of the voltage on V_{CC} and the output must be between 1 and 10 V/ μ s.

Programming Parameters

Do not test these parameters or you may program the device.

SYMBOL	PARAMETER	MIN	RECOMMENDED VALUE	MAX	UNIT
V_{CCP}	Required V_{CC} for programming	10.5	11.0	11.5	V
V_{OP}	Required output voltage for programming	10.5	11.0	11.5	V
t_R	Rise time of V_{CC} or V_{OUT}	1.0	5.0	10.0	V/ μ s
I_{CCP}	Current limit of V_{CCP} supply	800	1000	—	mA
I_{OP}	Current limit of V_{OP} supply	15	20	—	mA
t_{PW}	Programming pulse width (enabled)	9	10	11	μ s
V_{CC}	Low V_{CC} for verification	3.9	4.0	4.1	V
V_{CC}	High V_{CC} for verification	5.8	6.0	6.2	V
MDC	Maximum duty cycle of V_{CCP}	—	25	25	%
t_D	Delay time between programming steps	100	120	—	ns
V_{IL}	Input low level	0	0	0.5	V
V_{IH}	Input high level	2.4	3.0	5.5	V

Verification

After each programming pulse verification of the programmed bit should be made with both low and high V_{CC} . The loading of the output is not critical and any loading within the DC specifications of the part is satisfactory.

Additional Pulses

Up to 10 programming pulses should be applied until verification indicates that the bit has programmed. After verification an additional 5 programming pulses must be applied to insure the reliability of the programmed bit.

Board Level Programming

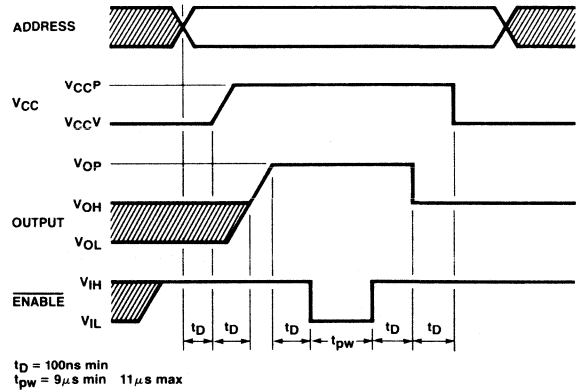
Board level programming is easily accomplished since only an enabled PROM is programmed. At the board level only the desired PROM and output should be enabled.

Programming Registered PROMs

The asynchronous registered PROM is programmed in the same manner as standard PROMs.

The synchronous registered PROM is programmed in similar fashion with one exception: the program enable is registered and therefore must be clocked.

Programming Waveforms



NOTE: Programming pulse t_{pw} is applied for 5 additional pulses after verification indicates a bit is blown.

Figure 1.



Programmer Cross Reference

High Performance Schottky Generic PROM Family "S"

MILITARY PART NO.	COMMERCIAL PART NO.	SIZE	CONFIGURATION	OUTPUT	NO. OF PINS	DATA I/O (ALL SERIES)		PRO-LOG (SERIES 90, 92)	
						PROGRAM CARD SET	SOCKET ADAPTER	PERSONALITY MODULE	PINOUT ADAPTER
53S080	63S080	¼K	32x8	OC	16	909-1515-1	715-1037	PM9066	PA16-2
53S081	63S081	¼K	32x8	TS	16	909-1515-1	715-1037	PM9066	PA16-2
53S140	63S140	1K	256x4	OC	16	909-1515-1	715-1035-1	PM9066	PA16-1
53S141	63S141	1K	256x4	TS	16	909-1515-1	715-1035-1	PM9066	PA16-1
53S240	63S240	2K	512x4	OC	16	909-1515-1	715-1035-2	PM9066	PA16-1
53S241	63S241	2K	512x4	TS	16	909-1515-1	715-1035-2	PM9066	PA16-1
53S280	63S280	2K	256x8	OC	20	909-1515-1	715-1028-1	PM9066	PA20-2
53S281	63S281	2K	256x8	TS	20	909-1515-1	715-1028-1	PM9066	PA20-2
53S440	63S440	4K	1Kx4	OC	18	909-1515-1	715-1039-3	PM9066	PA18-2
53S441	63S441	4K	1Kx4	TS	18	909-1515-1	715-1039-3	PM9066	PA18-2
53S480	63S480	4K	512x8	OC	20	909-1515-1	715-1064	PM9066	PA20-1
53S481	63S481	4K	512x8	TS	20	909-1515-1	715-1064	PM9066	PA20-1
53S482	63S482	4K	512x8	OC	24	909-1515-1	715-1602-1	PM9066	PA24-1
53S483	63S483	4K	512x8	TS	24	909-1515-1	715-1602-1	PM9066	PA24-1
53S840	63S840	8K	2Kx4	OC	18	909-1515-1	715-1603	PM9066	PA18-2
53S841	63S841	8K	2Kx4	TS	18	909-1515-1	715-1603	PM9066	PA18-2
53S880	63S880	8K	1Kx8	OC	24	909-1515-1	715-1602-2	PM9066	PA24-1
53S881	63S881	8K	1Kx8	TS	24	909-1515-1	715-1602-2	PM9066	PA24-1
53S1640	63S1640	16K	4Kx4	OC	20	909-1515-1	715-1605	PM9066	TBD
53S1641	63S1641	16K	4Kx4	TS	20	909-1515-1	715-1605	PM9066	TBD
53S1680	63S1680	16K	2Kx8	OC	24	909-1515-1	715-1604	PM9066	PA24-1
53S1681	63S1681	16K	2Kx8	TS	24	909-1515-1	715-1604	PM9066	PA24-1

High Performance Low Power Schottky Generic PROM Family "LS"

MILITARY PART NO.	COMMERCIAL PART NO.	SIZE	CONFIGURATION	OUTPUT	NO. OF PINS	DATA I/O (ALL SERIES)		PRO-LOG (SERIES 90, 92)	
						PROGRAM CARD SET	SOCKET ADAPTER	PERSONALITY MODULE	PINOUT ADAPTER
53LS080	63LS080	¼K	32x8	OC	16	909-1515-1	715-1037	PM9066	PA16-2
53LS081	63LS081	¼K	32x8	TS	16	909-1515-1	715-1037	PM9066	PA16-2
53LS140	63LS140	1K	256x4	OC	16	909-1515-1	715-1035-1	PM9066	PA16-1
53LS141	63LS141	1K	256x4	TS	16	909-1515-1	715-1035-1	PM9066	PA16-1
53LS240	63LS240	2K	512x4	OC	16	909-1515-1	715-1035-2	PM9066	PA16-1
53LS241	63LS241	2K	512x4	TS	16	909-1515-1	715-1035-2	PM9066	PA16-1
53LS280	63LS280	2K	256x8	OC	20	909-1515-1	715-1028-1	PM9066	PA20-2
53LS281	63LS281	2K	256x8	TS	20	909-1515-1	715-1028-1	PM9066	PA20-2
53LS440	63LS440	4K	1Kx4	OC	18	909-1515-1	715-1039-3	PM9066	PA18-2
53LS441	63LS441	4K	1Kx4	TS	18	909-1515-1	715-1039-3	PM9066	PA18-2
53LS480	63LS480	4K	512x8	OC	20	909-1515-1	715-1064	PM9066	PA20-1
53LS481	63LS481	4K	512x8	TS	20	909-1515-1	715-1064	PM9066	PA20-1
53LS482	63LS482	4K	512x8	OC	24	909-1515-1	715-1602-1	PM9066	PA24-1
53LS483	63LS483	4K	512x8	TS	24	909-1515-1	715-1602-1	PM9066	PA24-1
53LS840	63LS840	8K	2Kx4	OC	18	909-1515-1	715-1603	PM9066	PA18-2
53LS841	63LS841	8K	2Kx4	TS	18	909-1515-1	715-1603	PM9066	PA18-2
53LS880	63LS880	8K	1Kx8	OC	24	909-1515-1	715-1602-2	PM9066	PA24-1
53LS881	63LS881	8K	1Kx8	TS	24	909-1515-1	715-1602-2	PM9066	PA24-1
53LS1640	63LS1640	16K	4Kx4	OC	20	909-1515-1	715-1605	PM9066	TBD
53LS1641	63LS1641	16K	4Kx4	TS	20	909-1515-1	715-1605	PM9066	TBD
53LS1680	63LS1680	16K	2Kx8	OC	24	909-1515-1	715-1604	PM9066	PA24-1
53LS1681	63LS1681	16K	2Kx8	TS	24	909-1515-1	715-1604	PM9066	PA24-1

Programmer Cross Reference

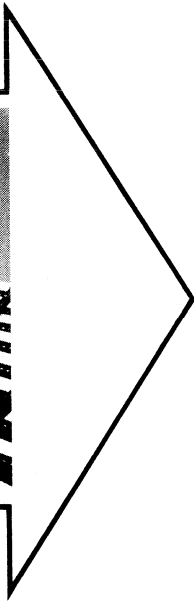
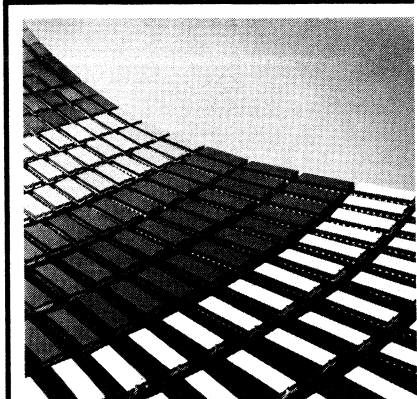
High Performance Power Switched Schottky Generic PROM Family "PS"

MILITARY PART NO.	COMMERCIAL PART NO.	SIZE	CONFIGURATION	OUTPUT	NO. OF PINS	DATA I/O (ALL SERIES)		PRO-LOG (SERIES 90, 92)	
						PROGRAM CARD SET	SOCKET ADAPTER	PERSONALITY MODULE	PINOUT ADAPTER
53PS080	63PS080	¼K	32x8	OC	16	909-1515-1	715-1037	PM9066	PA16-2
53PS081	63PS081	¼K	32x8	TS	16	909-1515-1	715-1037	PM9066	PA16-2
53PS140	63PS140	1K	256x4	OC	16	909-1515-1	715-1035-1	PM9066	PA16-1
53PS141	63PS141	1K	256x4	TS	16	909-1515-1	715-1035-1	PM9066	PA16-1
53PS240	63PS240	2K	512x4	OC	16	909-1515-1	715-1035-2	PM9066	PA16-1
53PS241	63PS241	2K	512x4	TS	16	909-1515-1	715-1035-2	PM9066	PA16-1
53PS280	63PS280	2K	256x8	OC	20	909-1515-1	715-1028-1	PM9066	PA20-2
53PS281	63PS281	2K	256x8	TS	20	909-1515-1	715-1028-1	PM9066	PA20-2
53PS440	63PS440	4K	1Kx4	OC	18	909-1515-1	715-1039-3	PM9066	PA18-2
53PS441	63PS441	4K	1Kx4	TS	18	909-1515-1	715-1039-3	PM9066	PA18-2
53PS480	63PS480	4K	512x8	OC	20	909-1515-1	715-1064	PM9066	PA20-1
53PS481	63PS481	4K	512x8	TS	20	909-1515-1	715-1064	PM9066	PA20-1
53PS482	63PS482	4K	512x8	OC	24	909-1515-1	715-1602-1	PM9066	PA24-1
53PS483	63PS483	4K	512x8	TS	24	909-1515-1	715-1602-1	PM9066	PA24-1
53PS840	63PS840	8K	2Kx4	OC	18	909-1515-1	715-1603	PM9066	PA18-2
53PS841	63PS841	8K	2Kx4	TS	18	909-1515-1	715-1603	PM9066	PA18-2
53PS880	63PS880	8K	1Kx8	OC	24	909-1515-1	715-1602-2	PM9066	PA24-1
53PS881	63PS881	8K	1Kx8	TS	24	909-1515-1	715-1602-2	PM9066	PA24-1
53PS1640	63PS1640	16K	4Kx4	OC	20	909-1515-1	715-1605	PM9066	TBD
53PS1641	63PS1641	16K	4Kx4	TS	20	909-1515-1	715-1605	PM9066	TBD
53PS1680	63PS1680	16K	2Kx8	OC	24	909-1515-1	715-1604	PM9066	PA24-1
53PS1681	63PS1681	16K	2Kx8	TS	24	909-1515-1	715-1604	PM9066	PA24-1

2

High Performance Registered Schottky Generic PROM Family

MILITARY PART NO.	COMMERCIAL PART NO.	SIZE	CONFIGURATION	PKG	PRE SET	ENABLE	CLK EN	DATA I/O (ALL SERIES)		PRO-LOG (SERIES 90, 92)	
								PROGRAM CARD SET	SOCKET ADAPTER	PERSONALITY MODULE	PINOUT ADAPTER
53RA281	63RA281	2K	256x8	24	YES	ASYNCH.	YES	909-1515-1	715-1601-1	PM9066	TBD
53RA283	63RA283	2K	256x8	24S	YES	ASYNCH.	YES	909-1515-1	715-1601-1	PM9066	TBD
53RA441	63RA441	4K	1Kx4	18	NO	ASYNCH.	NO	909-1515-1	715-1435	PM9066	PA18-5
53RS441	63RS441	4K	1Kx4	18	NO	SYNCH.	NO	909-1515-1	715-1435	PM9066	PA18-5
53RA481	63RA481	4K	512x8	24	YES	ASYNCH.	YES	909-1515-1	715-1601-2	PM9066	TBD
53RA483	63RA483	4K	512x8	24S	YES	ASYNCH.	YES	909-1515-1	715-1601-2	PM9066	TBD
53RA841	63RA841	8K	2Kx4	20	NO	ASYNCH.	NO	909-1515-1	715-1415-1	PM9066	PA20-6
53RS841	63RS841	8K	2Kx4	20	NO	SYNCH.	NO	909-1515-1	715-1415-1	PM9066	PA20-6
53RA881	63RA881	8K	1Kx8	24	YES	ASYNCH.	YES	909-1515-1	715-1601-3	PM9066	TBD
53RA883	63RA883	8K	1Kx8	24S	YES	ASYNCH.	YES	909-1515-1	715-1601-3	PM9066	TBD
53RA1641	63RA1641	16K	4Kx4	20	NO	ASYNCH.	NO	909-1515-1	715-1606	PM9066	TBD
53RS1641	63RS1641	16K	4Kx4	20	NO	SYNCH.	NO	909-1515-1	715-1606	PM9066	TBD
53RA1681	63RA1681	16K	2Kx8	24	YES	ASYNCH.	NO	909-1515-1	715-1601-4	PM9066	TBD
53RA1683	63RA1683	16K	2Kx8	24S	YES	ASYNCH.	NO	909-1515-1	715-1601-4	PM9066	TBD



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Standard Performance Schottky Generic ROM Family 52/62XX-1, 52/62XX-2

Features/Benefits

- Largest generic ROM family available
- PNP inputs for low input current
- Compatible pin configurations for upward expansions
- 4-bit-wide and 8-bit-wide for byte oriented applications
- Bit density from 256 to 16384
- Interchangeable PROM compatibility
- High speed Schottky technology

Applications

- High speed for microprogrammed applications
- Microprocessor program store
- Look up table
- Character generator
- Random logic
- Code converter

Description

The 52/6200-series generic ROM family offers the widest selection of sizes and organizations available in the industry. The 4-bit-wide ROMs range from 256x4 to 1024x4 and feature upward/downward pinout compatibility in the space saving 16 and 18 pin packages. The 8-bit-wide ROMs range from 32x8 to 2048x8 in a wide selection of package sizes. Additional 5-bit, 9-bit and 10-bit-wide output configurations are available for your custom logic or character generator applications.

The family features low input current PNP inputs, full Schottky clamping and three-state and open collector outputs.

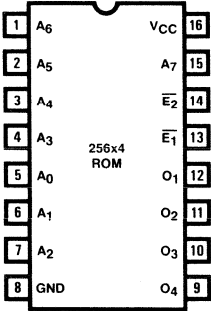
The 62 series is specified for operation over the commercial temperature and voltage range. The 52 series is specified for the military ranges. 52XX-2 and 62XX-2 devices offer enhanced speed specifications.

Generic ROM Selection Guide

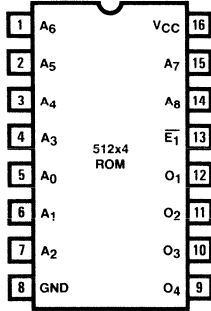
MEMORY			PACKAGE		DEVICE TYPE		INTERCHANGEABLE PROM	
Size	Organization		Pins	Type	0°C to +75°C	-55°C to +125°C	0°C to +75°C	-55°C to +125°C
1024	256x4	OC	16	J, N, F	6200-1	5200-1	6300-1	5300-1
		TS			6201-1	5201-1	6301-1	5301-1
2048	512x4	OC	16	J, N, F	6205-1	5205-1	6305-1	5305-1
		TS			6206-1	5206-1	6306-1	5306-1
4096	1024x4	OC	18	J, N, F	6250-1	5250-1	6350-1	5350-1
		TS			6251-1	5251-1	6351-1	5351-1
		OC			6252-1	5252-1	6352-1	5352-1
		TS			6253-1	5253-1	6353-1	5353-1
1280	256x5	OC	16	J, N, F	6210-1	5210-1	—	—
2560	512x5	OC	18	J, N	6225-1	5225-1	—	—
256	32x8	OC	16	J, N, F	6230-1	5230-1	6330-1	5330-1
		TS			6231-1	5231-1	6331-1	5331-1
2048	256x8	OC	20	J, N	6208-1	5208-1	6308-1	5308-1
		TS			6209-1	5209-1	6309-1	5309-1
2048	256x8	OC	24	J, N, F	6235-1	5235-1	6335-1	5335-1
		TS			6236-1	5236-1	6336-1	5336-1
4096	512x8	OC	20	J, N	6248-1	5248-1	6348-1	5348-1
		TS			6249-1	5249-1	6349-1	5349-1
4096	512x8	OC	24	J, N, F	6240-1	5240-1	6340-1	5340-1
		TS			6241-1	5241-1	6341-1	5341-1

Pin Configurations

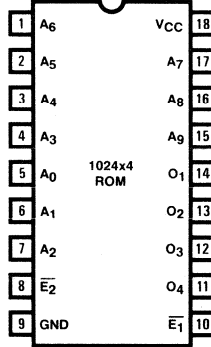
52/6200-1
52/6201-1



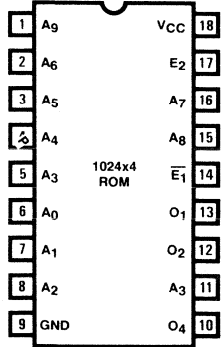
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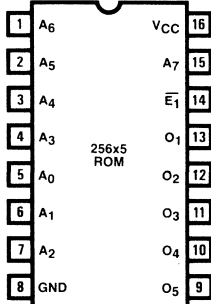
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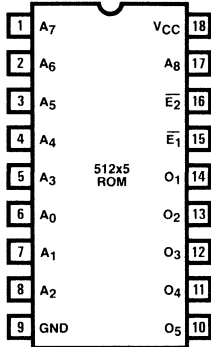
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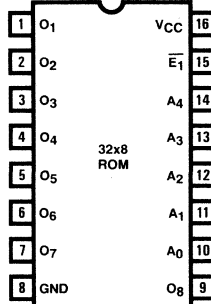
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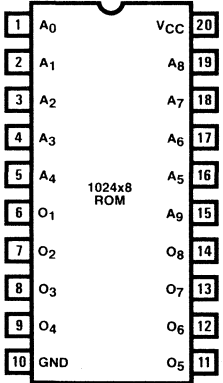
52/6225-1



52/6230-1
52/6231-1

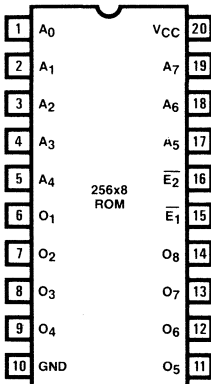


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52/6289-2

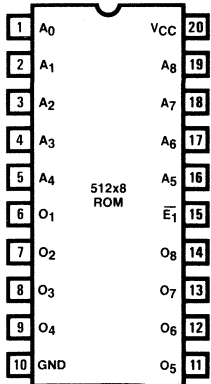


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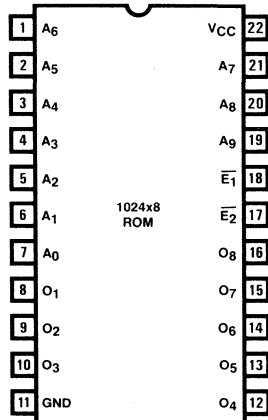
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52/6209-1



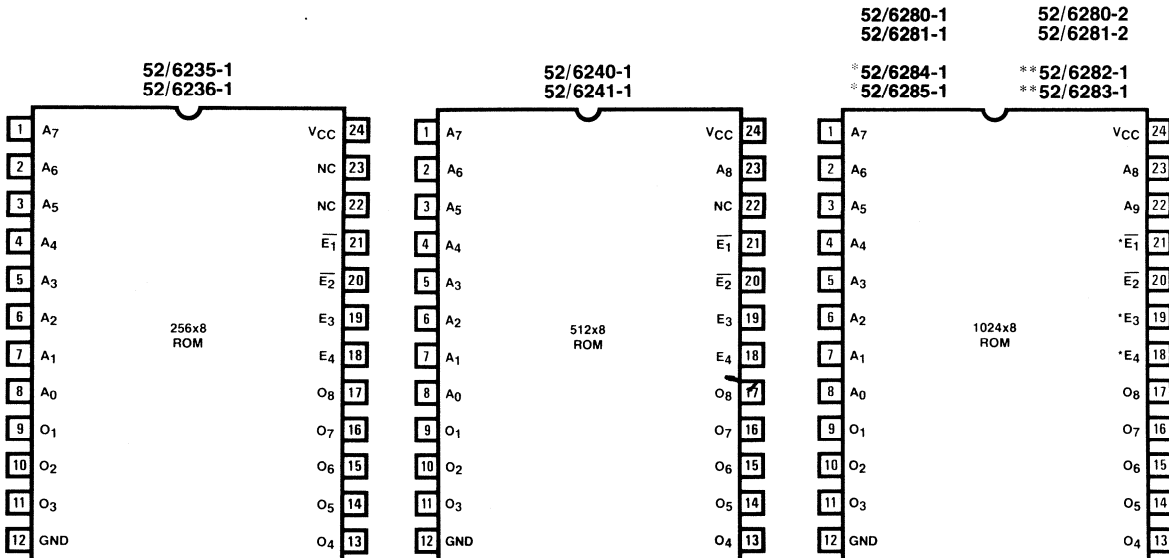
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52/6249-1



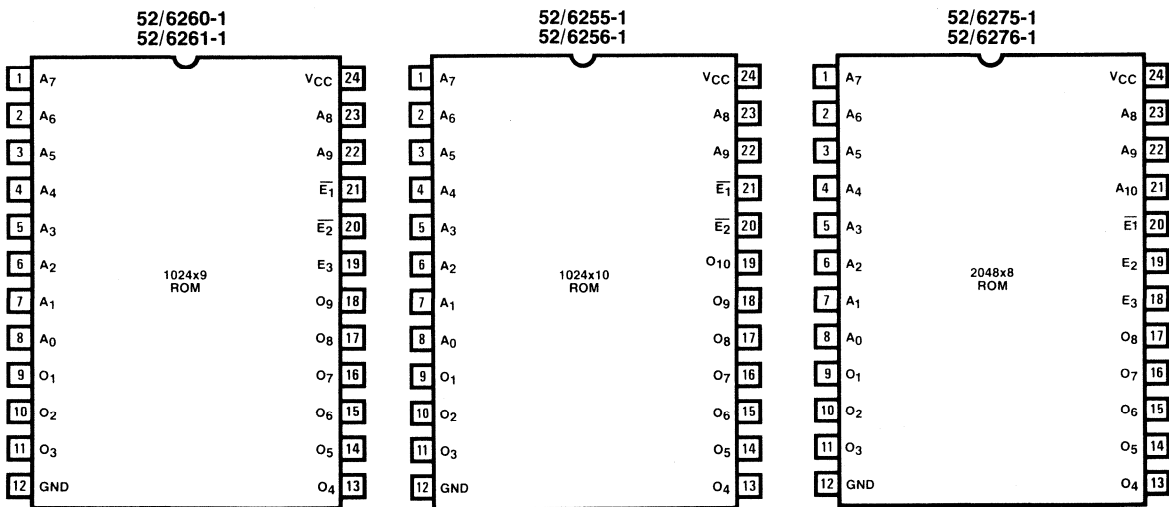
52/6286-1
52/6287-1



Pin Configurations



*NO CONNECTION
**"OR" ENABLE LIKE 6156
(see page 4-6)



NOTE:
Pin assignments for ceramic (J package), plastic (N package) and flat pack (F package) are the same.

Generic ROM Selection Guide

MEMORY			PACKAGE		DEVICE TYPE		INTERCHANGEABLE PROM	
SIZE	ORGANIZATION		PINS	TYPE	0°C to +75°C	-55°C to +125°C	0°C to +75°C	-55°C to +125°C
8192	1024x8	OC	24	J, N, F	6280-1	5280-1	6380-1	5380-1
		TS			6281-1	5281-1	6381-1	5381-1
		OC			6280-2	5280-2	—	—
		TS			6281-2	5281-2	—	—
		OC			6282-1	5282-1	—	—
		TS			6283-1	5283-1	—	—
		OC			6284-1	5284-1	—	5384-1
		TS			6285-1	5285-1	—	5385-1
		OC	22	J, N	6286-1	5286-1	—	—
		TS			6287-1	5287-1	—	—
		OC			6286-2	5286-2	—	—
		TS			6287-2	5287-2	—	—
		Active Pullup	20	J, N	6289-1	5289-1	—	—
					6289-2	5289-2	—	—
16384	2048x8	OC	24	J, N, F	6275-1	5275-1	635-1680	535-1680
		TS			6276-1	5276-1	635-1681	535-1681
9216	1024x9	OC	24	J, N, F	6260-1	5260-1	—	—
		TS			6261-1	5261-1	—	—
10240	1024x10	OC	24	J, N, F	6255-1	5255-1	—	—
		TS			6256-1	5256-1	—	—

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Absolute Maximum Ratings

Supply voltage V_{CC}-0.5V to +7.0V
Input voltage-1.5V to +5.5V
Input current-20 mA to +5 mA
Output current-100 mA to +100 mA
Storage temperature range-65°C to +150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	Military			Commercial			UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX		
V_{CC}	Supply voltage	4.5	5.0	5.5	4.75	5.00	5.25	V	
I_{OH}	High-level output current			-1.0			-2.0	mA	
I_{OL}	Low-level operating current	'05, '06, '08, '09, '48, '49, '50, '51, '52, '53			12			16	mA
		'00, '01, '10, '25			10		15		
		'30, '31			8		12		
		'35, '36, '40, '41, '80, '81, '82, '83, '84, '85, '86, '87, '89, '75, '76			8		10		
		'55, '56, '60, '61			6		6		
T_A	Operating free air temperature	-55	25	125	0	25	75	°C	

Electrical Characteristics Over Recommended Operating Free Air Temperature Range

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT		
V _{IH}	High level input voltage		2.0		V _{CC}	V		
V _{IL}	Low level input voltage		0		0.8	V		
V _{IC}	Input clamp voltage	V _{CC} = MIN, I _I = -18mA		-1.0	-1.5	V		
V _{OL}	Low level output voltage	V _{CC} = MIN, I _{OL} = MAX			0.50	V		
I _I	Maximum input current	V _{CC} = MAX, V _I = 5.5 V			1.0	mA		
I _{IH}	High level input current	V _{CC} = MAX, V _I = 2.4V			40	μA		
I _{IL}	Low level input current	V _{CC} = MAX, V _I = 0.45V			-250	μA		
C _I	Input capacitance	V _{CC} = 5.0V T _A = 25°C f = 1 MHz		7		pF		
C _O	Output capacitance	V _O = 2.0V		8		pF		
I _{CC}	Supply current	V _{CC} = MAX All inputs grounded All outputs open			'00, '01, '30, '31	92	125	mA
					'05, '06	96	130	
					'08, '09, '48, '49	115	155	
					'55, '60	122	165	
					'10, '25, '35, '40, '41, '80, '82	126	170	
					'84, '86, '89	130	175	
					'36, '50, '51, '52, '53, '56, '61	133	180	
					'81, '83, '85, '87	141	190	

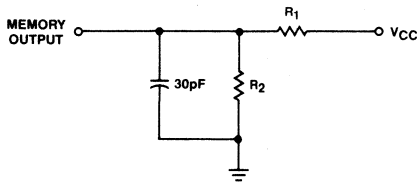
OPEN COLLECTOR OUTPUT CURRENT

I _{CEx}	Output leakage current	V _{CC} = MAX, V _O = 2.4V	100	μA
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THREE STATE OUTPUT ONLY

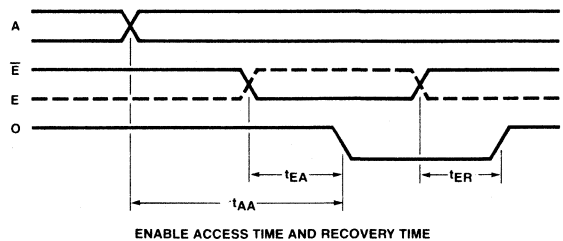
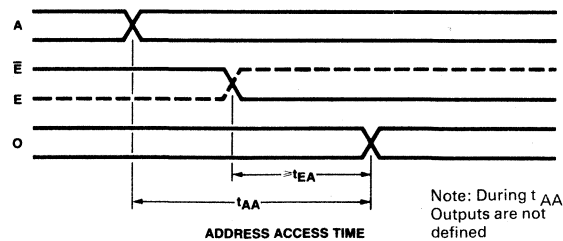
V _{OH}	High level output voltage	V _{CC} = MIN, I _{OH} = MAX	2.4		V
I _{HZ}	High level off State output current	8k, 9k, 10k		50	μA
		All others		100	
I _{LZ}	Low level off State output current	8k, 9k, 10k		-50	μA
		All others		-100	
I _{OS}	Output short circuit current	V _{CC} = 5.0V, V _O = 0V	-20	-90	mA

Standard Test Load



Input Pulse Amplitude 3.0V
Input Rise and Fall Times 5ns from 1.0V to 2.0V
Measurements Made at 1.5V

Definition of Waveforms



Switching CharacteristicsOver Recommended Ranges of T_A and V_{CC} (Unless Otherwise Noted)

DEVICE TYPE	CONDITIONS (See standard test load)		$t_{AA}(ns)$ ADDRESS ACCESS TIME	$t_{EA}(ns)$ ENABLE ACCESS TIME	$t_{ER}(ns)$ ENABLE RECOVERY TIME
	$R_1 \Omega$	$R_2 \Omega$	MAX	MAX	MAX
6200-1, 6201-1	300	600	45	35	35
5200-1, 5201-1	450	900	60	35	35
6205-1, 6206-1	280	560	60	30	30
5205-1, 5206-1	375	750	75	40	40
6210-1	300	600	100	70	45
5210-1	450	900	175	90	50
6225-1	300	600	100	70	45
5225-1	450	900	175	90	50
6230-1, 6231-1	375	750	50	30	25
5230-1, 5231-1	560	1120	60	30	25
6208-1, 6209-1	280	560	70	30	30
5208-1, 5209-1	375	750	80	40	40
6235-1, 6236-1	450	900	100	70	45
5235-1, 5236-1	560	1120	175	90	50
6248-1, 6249-1	280	560	70	30	30
5248-1, 5249-1	375	750	80	40	40
6240-1, 6241-1	450	900	100	70	45
5240-1, 5241-1	560	1120	175	90	50
6250-1, 6251-1	280	560	60	30	30
5250-1, 5251-1	375	750	75	40	40
6252-1, 6253-1	280	560	60	30	30
5252-1, 5253-1	375	750	75	40	40
6255-1, 6256-1	750	1500	100	70	40
5255-1, 5256-1	750	1500	150	80	45
6260-1, 6261-1	750	1500	100	70	40
5260-1, 5261-1	750	1500	150	80	45
6275-1, 6276-1	450	900	110	40	40
5275-1, 5276-1	560	1120	120	50	50
6280-1, 6281-1	450	900	100	70	45
5280-1, 5281-1	560	1120	175	90	50
6280-2, 6281-2	450	900	55	30	30
5280-2, 5281-2	560	1120	75	35	35
6282-1, 6283-1	450	900	100	70	45
5282-1, 5283-1	560	1120	175	90	50
6284-1, 6285-1	450	900	100	70	45
5284-1, 5285-1	560	1120	175	90	50
6286-1, 6287-1	450	900	100	70	45
5286-1, 5287-1	560	1120	175	90	50
6286-2, 6287-2	450	900	55	30	30
5286-2, 5287-2	560	1120	75	35	35
6289-1	750	1500	100	70	45
5289-1	750	1500	175	90	50
6289-2	750	1500	55	30	30
5289-2	750	1500	75	35	35

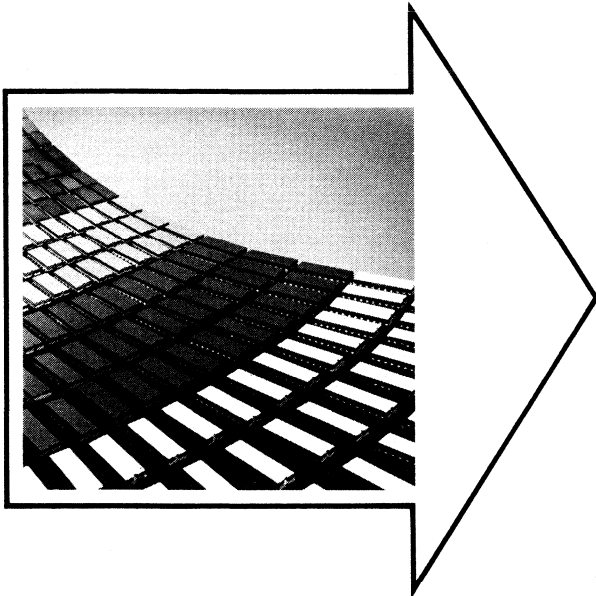
High Performance Schottky ROMs

ROM mates to our High Performance Schottky Generic PROM family members are available through the use of a metal and contact mask option. This allows us to replace the titanium-tungsten fuse structure with a normal aluminum interconnect. Actual bit patterns are then optioned by either making a cut in the oxide or not at contact mask. Since ROMs represent a custom part, with minimum volumes available and involve non-standard lead times in production, please contact your factory representative for more details.

ROM Mates Are Available in all Four Generic Families

1. Schottky "S" high speed
2. Low power "LS"
3. Power switched "PS"
4. Registered "RA/RS"

Please refer to the appropriate High Performance Schottky PROM GENERIC family data sheet for the detail device operating specification. Your ROM mate will be identical.



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High Speed Bipolar 5x7 Character Generator Family 5/6XXX

Features/Benefits

- Schottky high speed 10 MHz
- Low power dissipation—500 mW
- Standard packaging—18 pin dip/24 pin dip
- Single 5 volt supply
- 100 ns max. access time
- 64/128 characters in one package
- Open collector or three-state

Description

The intended application for these devices is the generation of 64 or 128 ASCII alpha-numeric characters utilizing a read out system which generates the characters either horizontally or vertically, one word line at a time.

Applications

- A single package high speed bipolar replacement for slow multiple package MOS character generators
- CRT displays
- Printing calculators
- LED arrays
- Typesetting

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Character Generator Selection Guide

PART NUMBER	MATRIX	CHARACTERS	SCAN	OUTPUT	TEMPERATURE	PACKAGE
6055	5x7	64	Row	OC	C	N18
5055	5x7	64	Row	OC	M	J18
6056	5x7	64	Column	OC	C	N24
5056	5x7	64	Column	OC	M	J24
6061	5x7	128	Row	OC	C	N24
5061	5x7	128	Row	OC	M	J24
6062	5x7	128	Column	OC	C	N24
5062	5x7	128	Column	OC	M	J24
6155	5x7	64	Row	TS	C	N18
5155	5x7	64	Row	TS	M	J18
6156	5x7	64	Column	TS	C	N24
5156	5x7	64	Column	TS	M	J24
6161	5x7	128	Row	TS	C	N24
5161	5x7	128	Row	TS	M	J24
6162	5x7	128	Column	TS	C	N24
5162	5x7	128	Column	TS	M	J24

Absolute Maximum Ratings

Supply voltage V_{CC}	Operating -0.5V to 7V
Input voltage	-1.5V to 5.5V
Off-state output voltage	-1.5V to 5.5V
Storage temperature range	-65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.75	5.00	5.25	V
I_{OH}	High level output current			-1.0			-2.0	mA
I_{OL}	Low level output current			8			10	mA
T_A	Operating free air temperature	-55		125	0		75	°C

Electrical Characteristics**Over Recommended Operating Free Air Temperature Range**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2		V_{CC}	V
V_{IL}	Low-level input voltage		0.0		0.8	V
V_{IC}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$		-1.0	-1.5	V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V},$ $V_{IL} = 0.8\text{V}, I_{OL} = \text{MAX}.$			0.5	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5\text{V}$			1.0	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4\text{V}$			40	μA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.45\text{V}$			-250	μA
C_I	Input capacitance	$V_{CC} = 5.0\text{V}, f = 1\text{MHz}$		7.0		pF
C_O	Output capacitance	$T_A = 25^\circ\text{C}$		8.0		
I_{CC}	Supply current	$V_{CC} = \text{MAX}$			170	mA
			OC		180	
		TS				

OPEN COLLECTOR OUTPUT CURRENT

I_{CEX}	Output Leakage Current	$V_{CC} = \text{MAX}, V_O = 2.4\text{V}$		100	μA
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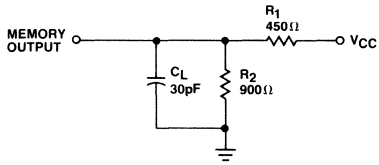
THREE STATE OUTPUT ONLY

V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V},$ $V_{IL} = 0.8\text{V}, I_{OH} = \text{MAX}$	2.4		V
I_{OZH}	Off-state output current high-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2\text{V},$ $V_O = 2.4\text{V}$		100	μA
I_{OZL}	Off-state output current low-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2\text{V},$ $V_O = 0.5\text{V}$		-100	μA
I_{OS}	Short-circuit output current	$V_{CC} = \text{MAX}, V_O = 0\text{V}$	-20	-90	mA

Switching Characteristics**Over Recommended Ranges of T_A and V_{CC}**

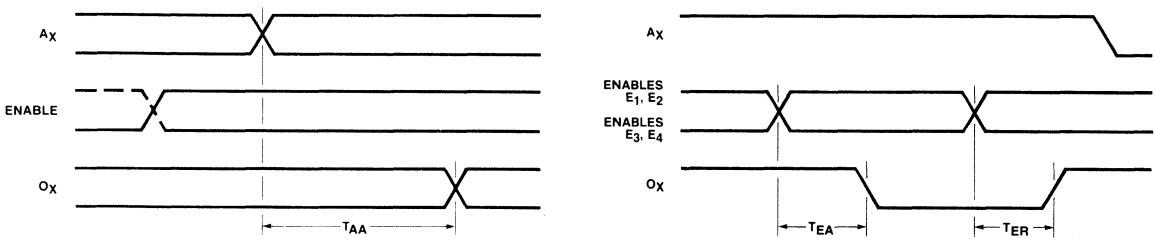
SYMBOL	PARAMETER	MILITARY		COMMERCIAL		UNIT
		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$		$T_A = -0^\circ\text{C to } +75^\circ\text{C}$		
		$V_{CC} = 5.0\text{V} \pm 10\%$		$V_{CC} = 5.0\text{V} \pm 5\%$		
		MIN	MAX	MIN	MAX	
t_{AA}	Address access time		175		100	ns
t_{EA}	Enable access time		90		70	ns
t_{ER}	Enable recovery time		50		45	ns

Standard Test Load



Input pulse amplitude = 3.0V.
 Input pulse rise and fall times must be 5 ns between 1.0V and 2.0V.
 Speed measurements are made at 1.5V.
 Output Loading is 10mA and 30pF as given in standard load.

Test Waveforms



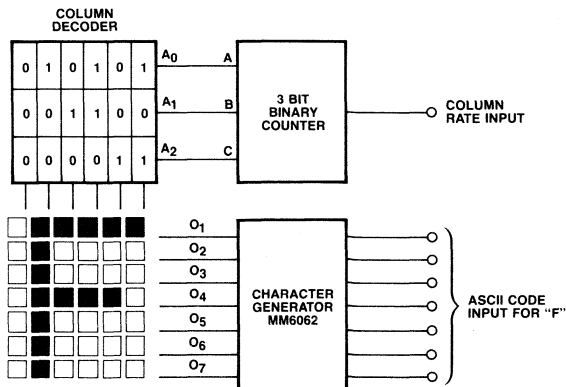
Note: During t_{AA}
 Outputs are not
 defined

A_X = Any Address
 O_X = Any Output

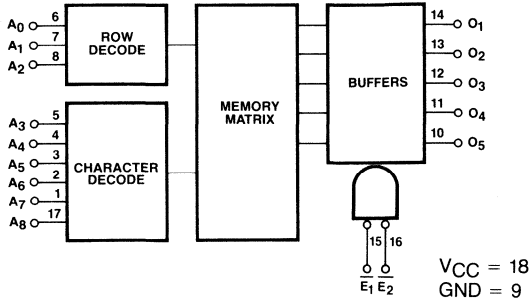
Fig. 2 Enable Access Time and Recovery Time

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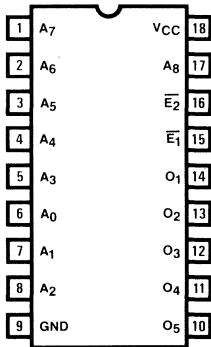
Generation of the Letter "F"



Block Diagram—60/6155, 50/5155



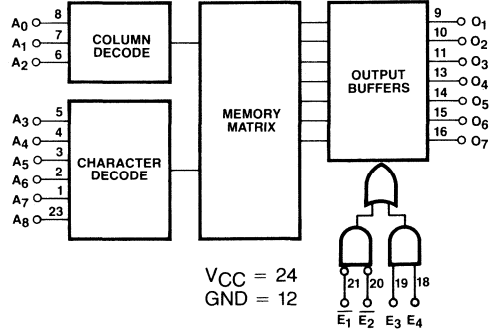
Pin Configuration



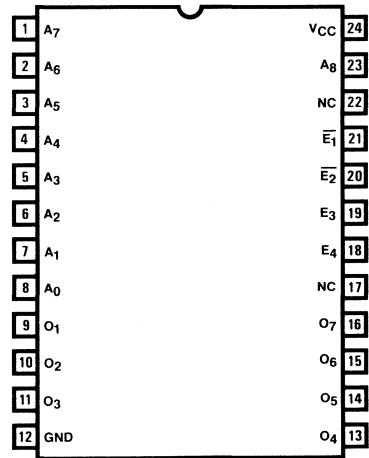
Note: A₀, A₁, A₂, A₃ are used for the character scan.

5x7 Row Scan, 64 Characters

Block Diagram—60/6156, 50/5156



Pin Configuration



5x7 Column Scan, 64 Characters

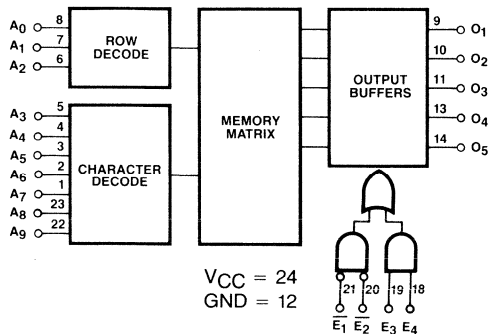
**Character Generator Operation—
6055, 6155**

The intended application for the MM6055 device is the generation of 64 USACII characters utilizing a readout system which generates the characters horizontally a 5-bit line at a time. Each 35-bit character is composed of 7 distinct 5-bit lines. One of the 64 characters is selected by the 6-bit address applied to A₃ through A₈. The particular 5-bit line within each character is determined by the 3-bit address applied to A₀, A₁ and A₂. The binary address 000 on A₀, A₁ and A₂ provides a blank line for character line spacing. The memory is enabled when both \bar{E}_1 and \bar{E}_2 are low (logic "0").

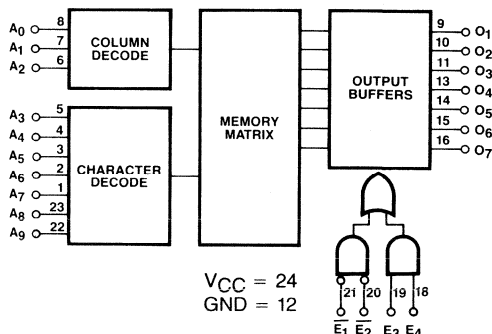
**Character Generator Operation—
6056, 6156**

The intended application for the MM6056 is the generation of 64 USACII characters utilizing a readout system which generates the characters vertically a 7-bit line at a time. Each 35-bit character is composed of 7 distinct 5-bit lines. One of the 64 characters is selected by the 6-bit address applied to A₃ thru A₈. The particular 5-bit line within each character is determined by the 3 bit address applied to A₀, A₁ and A₂. The binary address 000 on A₀, A₁ and A₂ provides a blank line for character line spacing. The memory is enabled when either E₁ and E₂ are high (logic "1") or E₃ and E₄ are high (logic "1").

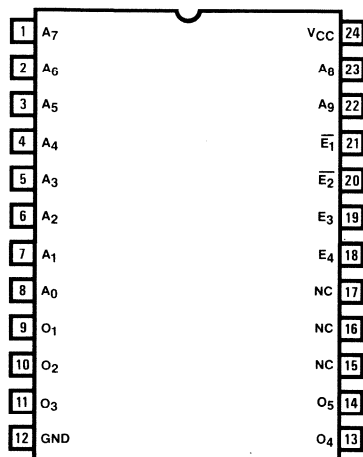
Block Diagram 60/6161, 50/5161



Block Diagram—60/6162, 50/5162

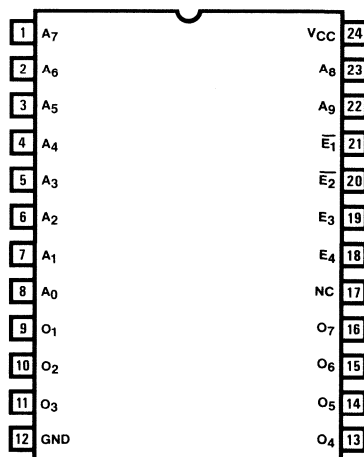


Pin Configuration



5x7 Row Scan, 128 Characters

Pin Configuration



5x7 Column Scan, 128 Characters

Note: A₀, A₁, A₂, A₃ are used for the character scan.

**Character Generator Operation—
6061, 6161**

The intended application for the MM6061 is the generation of 128 USACII characters utilizing a readout system which generates the characters horizontally a 5-bit line at a time. Each 35-bit character is composed of 7 distinct 5-bit lines. One of the 128 characters is selected by the 7-bit address applied to A₃ thru A₉. The particular 5-bit line within each character is determined by the 3-bit address applied to A₀, A₁ and A₂. The binary address 000 on A₀, A₁ and A₂ provides a blank line for character line spacing. The memory is enabled when either E₁ and E₂ are low (logic "0") or E₃ and E₄ are high (logic "1").

**Character Generator Operation—
6062, 6162**

The intended application for the MM6062 is the generation of 128 USACII characters utilizing a readout system which generates the characters vertically a 7-bit line at a time. Each 35-bit character is composed of 7 distinct 5-bit lines. One of the 128 characters is selected by the 7-bit address applied to A₃ thru A₉. The particular 5-bit line within each character is determined by the 3-bit address applied to A₀, A₁ and A₂. The binary address 000 on A₀, A₁ and A₂ provides a blank line for character line spacing. The memory is enabled when either E₁ and E₂ are low (logic "0") or E₃ and E₄ are high (logic "1").



A "Filled In" Dot Represents a Low Memory Output

ASCII INPUT ADDRESS	A ₃ A ₄ A ₅ 000	A ₃ A ₄ A ₅ 100	A ₃ A ₄ A ₅ 010	A ₃ A ₄ A ₅ 110	A ₃ A ₄ A ₅ 001	A ₃ A ₄ A ₅ 101	A ₃ A ₄ A ₅ 011	A ₃ A ₄ A ₅ 111
A ₆ A ₇ A ₈ 000	Q1 Q2 Q3 Q4 Q5 Q6 Q7							
A ₆ A ₇ A ₈ 100	Q1 Q2 Q3 Q4 Q5 Q6 Q7							
A ₆ A ₇ A ₈ 010	Q1 Q2 Q3 Q4 Q5 Q6 Q7							
A ₆ A ₇ A ₈ 110	Q1 Q2 Q3 Q4 Q5 Q6 Q7							
A ₆ A ₇ A ₈ 001	Q1 Q2 Q3 Q4 Q5 Q6 Q7							
A ₆ A ₇ A ₈ 101	Q1 Q2 Q3 Q4 Q5 Q6 Q7							
A ₆ A ₇ A ₈ 011	Q1 Q2 Q3 Q4 Q5 Q6 Q7							
A ₆ A ₇ A ₈ 111	Q1 Q2 Q3 Q4 Q5 Q6 Q7							

4

*From the USASCII code A₈ = B₇ = B₆.

A "Filled In" Dot Represents a Low Memory Output

ASCII INPUT ADDRESS	B7B6B5 A9A8A7 000 O5O4O3O2O1	A9A8A7 001	A9A8A7 010	A9A8A7 011	A9A8A7 100	A9A8A7 101	A9A8A7 110	A9A8A7 111
B4B3B2B1 A6A5A4A3 0000	 (NUL)*	 (DLE)*						
A6A5A4A3 0001	 (SOH)*	 (DC1)*						
A6A5A4A3 0010		 (DC2)*						
A6A5A4A3 0011	 (ETX)*	 (DC3)*						
A6A5A4A3 0100	 (EOT)*	 (DC4)*						
A6A5A4A3 0101	 (ENQ)*	 (NAK)*						
A6A5A4A3 0110	 (ACK)*	 (SYN)*						
A6A5A4A3 0111	 (BEL)*	 (ETB)*						

*The letters in parenthesis identify the control code corresponding to the appropriate 35 bit pictorial representation. These representations were obtained from the USASI X 3.2 Code Practice Manual.

A "Filled In" Dot Represents a Low Memory Output

ASCII INPUT ADDRESS	B7B6B5 AgA8A7 000 O5O4O3O2O1	A9A8A7 001	A9A8A7 010	A9A8A7 011	A9A8A7 100	A9A8A7 101	A9A8A7 110	A9A8A7 111
B4B3B2B1 AgA5A4A3 1000	(BS)*	(CAN)*	(HT)*	(EM)*	(LF)*	(SUB)*	(VT)*	(ESC)*
AgA5A4A3 1001	(FF)*	(FS)*	(CR)*	(GS)*	(SO)*	(RS)*	(SI)*	(US)*
AgA5A4A3 1010	(DEL)*	(DEL)*	(DEL)*	(DEL)*	(DEL)*	(DEL)*	(DEL)*	(DEL)*
AgA5A4A3 1011	(DEL)*	(DEL)*	(DEL)*	(DEL)*	(DEL)*	(DEL)*	(DEL)*	(DEL)*
AgA5A4A3 1100	(DEL)*	(DEL)*	(DEL)*	(DEL)*	(DEL)*	(DEL)*	(DEL)*	(DEL)*
AgA5A4A3 1101	(DEL)*	(DEL)*	(DEL)*	(DEL)*	(DEL)*	(DEL)*	(DEL)*	(DEL)*
AgA5A4A3 1110	(DEL)*	(DEL)*	(DEL)*	(DEL)*	(DEL)*	(DEL)*	(DEL)*	(DEL)*
AgA5A4A3 1111	(DEL)*	(DEL)*	(DEL)*	(DEL)*	(DEL)*	(DEL)*	(DEL)*	(DEL)*

4

*The letters in parenthesis identify the control code corresponding to the appropriate 35 bit pictorial representation. These representations were obtained from the USASI X 3.2 Code Practice Manual.

A "Filled In" Dot Represents a Low Memory Output

ASCII INPUT ADDRESS	B ₇ B ₆ B ₅ A ₉ A ₈ A ₇ 000	A ₉ A ₈ A ₇ 001	A ₉ A ₈ A ₇ 010	A ₉ A ₈ A ₇ 011	A ₉ A ₈ A ₇ 100	A ₉ A ₈ A ₇ 101	A ₉ A ₈ A ₇ 110	A ₉ A ₈ A ₇ 111	
B ₄ B ₃ B ₂ B ₁ A ₆ A ₅ A ₄ A ₃ 0000	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇ (NUL)*	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇ (DLE)*	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	
A ₆ A ₅ A ₄ A ₃ 0001	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇ (SOH)*	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇ (DC1)*	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	
A ₆ A ₅ A ₄ A ₃ 0010	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇ (STX)*	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇ (DC2)*	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇
A ₆ A ₅ A ₄ A ₃ 0011	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇ (ETX)*	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇ (DC3)*	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇
A ₆ A ₅ A ₄ A ₃ 0100	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇ (EOT)*	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇ (DC4)*	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇
A ₆ A ₅ A ₄ A ₃ 0101	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇ (ENQ)*	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇ (NAK)*	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇
A ₆ A ₅ A ₄ A ₃ 0110	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇ (ACK)*	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇ (SYN)*	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇
A ₆ A ₅ A ₄ A ₃ 0111	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇ (BEL)*	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇ (ETB)*	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇	0 ₁ 0 ₂ 0 ₃ 0 ₄ 0 ₅ 0 ₆ 0 ₇

*The letters in parenthesis identify the control code corresponding to the appropriate 35 bit pictorial representation. These representations were obtained from the USASI X 3.2 Code Practice Manual.

A "Filled In" Dot Represents a Low Memory Output

ASCII INPUT ADDRESS	B7B6B5 A9A8A7 000	A9A8A7 001	A9A8A7 010	A9A8A7 011	A9A8A7 100	A9A8A7 101	A9A8A7 110	A9A8A7 111	
B4B3B2B1 A6A5A4A3 1000	O1 <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> O2 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> O3 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> O4 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> O5 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> O6 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> O7 <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> <input checked="" type="checkbox"/> <input checked="" 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High Speed Bipolar 7x9 Character Generator Family 5/6XXX

Features/Benefits

- Schottky high speed 10 MHz
- 64/128 alpha- numerics in one package
- Low power dissipation—500 mW
- Standard packaging—24 pin dip
- Single 5 volt supply
- 125 ns max. access time

Applications

- A single package high speed bipolar replacement for slow multiple package MOS character generators
- CRT displays
- Printing calculators
- LED arrays
- Typesetting

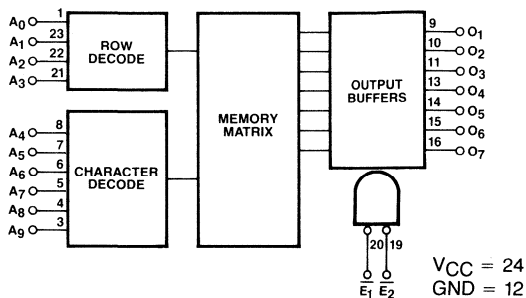
Description

The intended application for these devices is the generation of 64 or 128 ASCII alpha-numeric characters utilizing a read out system which generates the characters either horizontally or vertically, one word line at a time.

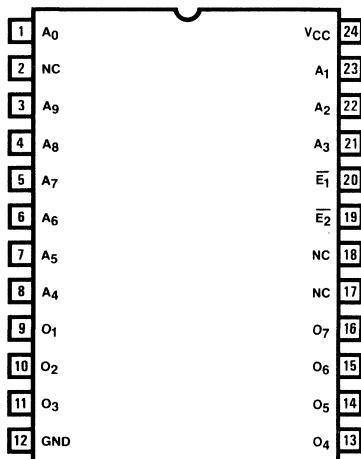
Character Generator Selection Guide

PART NUMBER	MATRIX	CHARACTERS	SCAN	OUTPUT	TEMPERATURE	PACKAGE
6071	7x9	64	Row	OC	C	N24
5071	7x9	64	Row	OC	M	J24
6072	7x9	128	Row	OC	C	N24
5072	7x9	128	Row	OC	M	J24
6073	7x9	128	Column	OC	C	N24
5073	7x9	128	Column	OC	M	J24
6074	7x9	64	Column	OC	C	N24
5074	7x9	64	Column	OC	M	J24
6171	7x9	64	Row	TS	C	N24
5171	7x9	64	Row	TS	M	J24
6172	7x9	128	Row	TS	C	N24
5172	7x9	128	Row	TS	M	J24
6173	7x9	128	Column	TS	C	N24
5173	7x9	128	Column	TS	M	J24
6174	7x9	64	Column	TS	C	N24
5174	7x9	64	Column	TS	M	J24

Block Diagram—60/6171, 50/5171



Pin Configuration



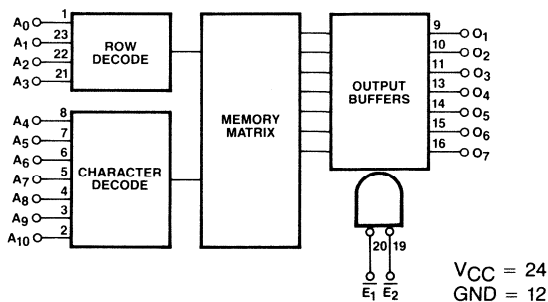
NOTE: A₀, A₁, A₂, A₃ are used for the character scan.

7x9 Row Scan, 64 Characters

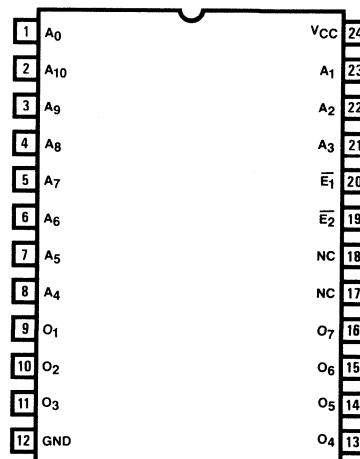
Character Generator Operation—6071, 6171

The intended application for the MM6071 is the generation of 64 USASCII characters utilizing a readout system which generates the characters horizontally a 7-bit line at a time. Each 63-bit character is composed of 9 distinct 7-bit lines. One of the 64 characters is selected by the 6-bit address applied to A₄ thru A₉. The particular 7-bit line within each character is determined by the 4-bit address applied to A₀, A₁, A₂ and A₃. The binary addresses 9 thru 15 on A₀, A₁, A₂ and A₃ do not exist in the memory (since we want a 7 x 9 character) and will result in a low output if they are selected. Since the characters are produced by low outputs binary addresses 9 thru 15 should be avoided to eliminate confusion. This can be accomplished by "short counting" a 4-bit binary counter so that states 9 thru 15 don't exist. The memory is enabled when both E₁ and E₂ are low.

Block Diagram—60/6172, 50/5172



Pin Configuration

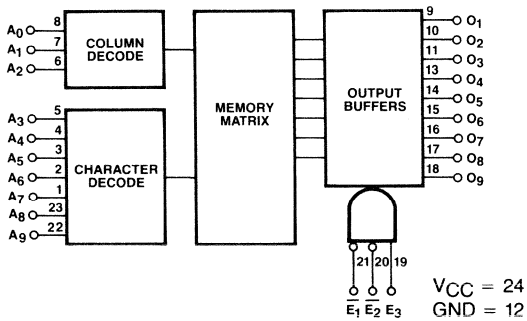


7x9 Row Scan, 128 Characters

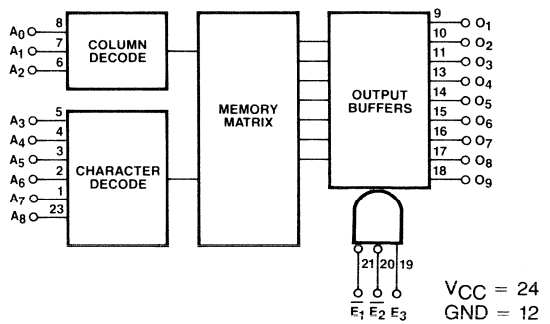
Character Generator Operation—6072, 6172

The intended application for the MM6072 is the generation of 128 USASCII characters utilizing a readout system which generates the characters horizontally a 7-bit line at a time. Each 63-bit character is composed of 9 distinct 7-bit lines. One of the 128 characters is selected by the 7-bit address applied to A₄ thru A₁₀. The particular 7-bit line within each character is determined by the 4-bit address applied to A₀, A₁, A₂ and A₃. The binary addresses 9 thru 15 on A₀, A₁, A₂ and A₃ do not exist in the memory (since we want a 7 x 9 character) and will result in a low output if they are selected. Since the characters are produced by low outputs binary addresses 9 thru 15 should be avoided to eliminate confusion. This can be accomplished by "short counting" a 4-bit binary counter so that states 9 thru 15 don't exist. The MM6072 is an 1152 word ROM (128 characters at 9 rows each) and words 1152 thru 2047 do not exist and should be avoided. The memory is enabled when both E₁ and E₂ are low.

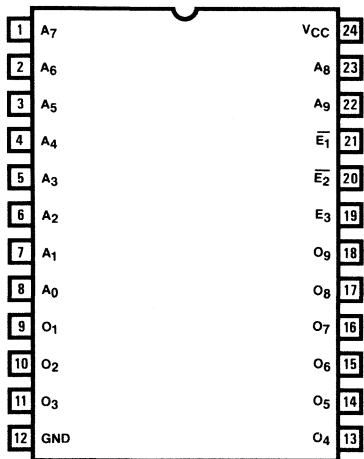
Block Diagram—60/6173, 50/5173



Block Diagram—60/6174, 50/5174

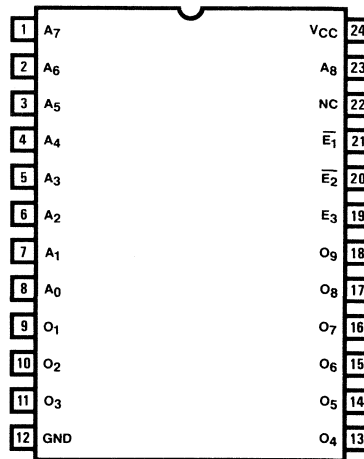


Pin Configuration



7x9 Column Scan, 128 Characters

Pin Configuration



7x9 Column Scan, 64 Characters

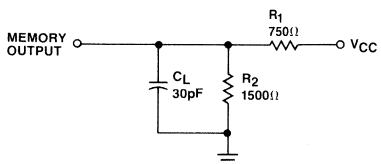
**Character Generator Operation—
6073, 6173**

The intended application for the MM6073 is the generation of 128 USACII characters utilizing a readout system which generates the characters vertically a 9-bit column at a time. Each 63-bit character is composed of 7 distinct 9-bit lines. One of the 128 characters is selected by the 7-bit address applied to A₃ thru A₉. The particular 9-bit column within each character is determined by the 3-bit address applied to A₀, A₁ and A₂. The binary address 000 on A₀, A₁ and A₂ provides a blank line for character line spacing. The memory is enabled when both E₁ and E₂ are low and E₃ is high.

**Character Generator Operation—
6074, 6174**

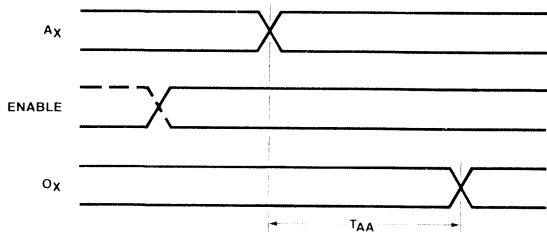
The intended application for the MM6074 is the generation of 64 USACII characters utilizing a readout system which generates the characters vertically a 9-bit column at a time. Each 63-bit character is composed of 7 distinct 9-bit lines. One of the 64 characters is selected by the 6-bit address applied to A₃ thru A₈. The particular 9-bit column within each character is determined by the 3-bit address applied to A₀, A₁ and A₂. The binary address 000 on A₀, A₁, and A₂ provides a blank line for character line spacing. The memory is enabled when both E₁ and E₂ are low and E₃ is high.

Standard Test Load



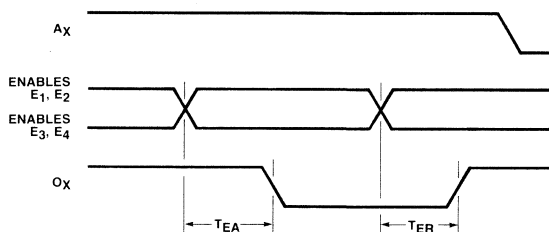
Input pulse amplitude = 3.0V.
 Input pulse rise and fall times must be 5ns between 1.0V and 2.0V.
 Speed measurements are made at 1.5V.
 Output loading is 6mA and 30pF as given in standard load.

Test Waveforms



Note: During t_{AA}
 Outputs are not
 defined

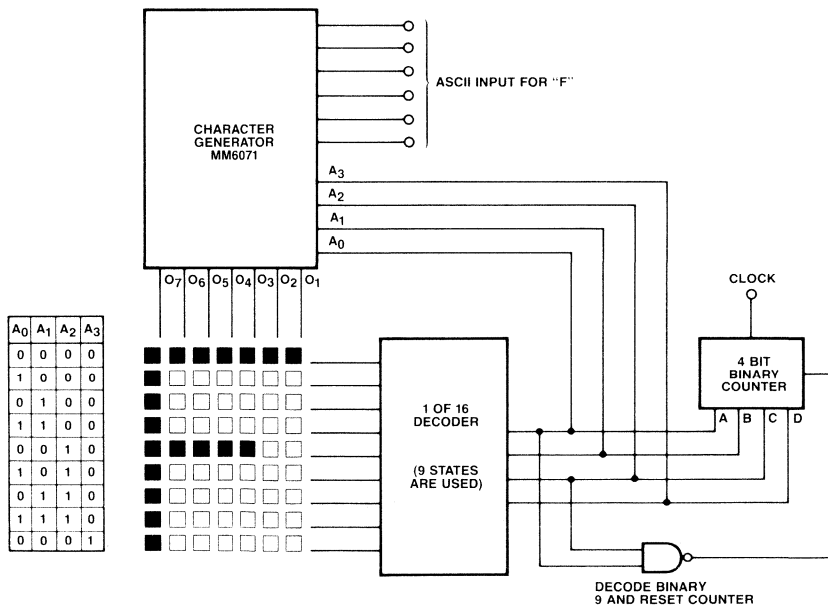
Fig. 1 Access Time



A_X = Any Address
 O_X = Any Output

Fig. 2 Enable Access Time and Recovery Time

Generation of the Letter "F"



A "Filled In" Dot Represents a Low Memory Output

ASCII INPUT ADDRESS	B7B6B5 AgAgA7 000	B7B6B5 AgAgA7 001	B7B6B5 AgAgA7 010	B7B6B5 AgAgA7 011	B7B6B5 AgAgA7 100	B7B6B5 AgAgA7 101	B7B6B5 AgAgA7 110	B7B6B5 AgAgA7 111
B3B2B1 AgA4A3 000	O1 O2 O3 O4 O5 O6 O7 O8 O9							
B3B2B1 AgA4A3 001	O1 O2 O3 O4 O5 O6 O7 O8 O9							
B3B2B1 AgA4A3 010	O1 O2 O3 O4 O5 O6 O7 O8 O9							
B3B2B1 AgA4A3 011	O1 O2 O3 O4 O5 O6 O7 O8 O9							
B3B2B1 AgA4A3 100	O1 O2 O3 O4 O5 O6 O7 O8 O9							
B3B2B1 AgA4A3 101	O1 O2 O3 O4 O5 O6 O7 O8 O9							
B3B2B1 AgA4A3 110	O1 O2 O3 O4 O5 O6 O7 O8 O9							
B3B2B1 AgA4A3 111	O1 O2 O3 O4 O5 O6 O7 O8 O9							

4

*These representations were obtained from the USASI X 3.2 Code Practice Manual. Address Ag = B7 = B̄5.

A "Filled In" Dot Represents a Low Memory Output

ASCII INPUT ADDRESS	B7B6B5 A10A9A8 000 07060504030201	B7B6B5 A10A9A8 001 07060504030201	B7B6B5 A10A9A8 010 07060504030201	B7B6B5 A10A9A8 011 07060504030201	B7B6B5 A10A9A8 100 07060504030201	B7B6B5 A10A9A8 101 07060504030201	B7B6B5 A10A9A8 110 07060504030201	B7B6B5 A10A9A8 111 07060504030201
B4B3B2B1 A7A6A5A4 0000								
	(NUL)*	(DLE)*						
B4B3B2B1 A7A6A5A4 0001								
	(SOH)*	(DC1)*						
B4B3B2B1 A7A6A5A4 0010								
		(DC2)*						
B4B3B2B1 A7A6A5A4 0011								
	(ETX)*	(DC3)*						
B4B3B2B1 A7A6A5A4 0100								
	(EOT)*	(DC4)*						
B4B3B2B1 A7A6A5A4 0101								
	(ENO)*	(NAK)*						
B4B3B2B1 A7A6A5A4 0110								
	(ACK)*	(SYN)*						
B4B3B2B1 A7A6A5A4 0111								
	(BEL)*	(ETB)*						

*The letters in parenthesis identify the control code corresponding to the appropriate 63 bit pictorial representation. These representations were obtained from the USASI X 3.2 Code Practice Manual.

A "Filled In" Dot Represents a Low Memory Output

ASCII INPUT ADDRESS	B7B6B5 A9A8A7 000	B7B6B5 A9A8A7 001	B7B6B5 A9A8A7 010	B7B6B5 A9A8A7 011	B7B6B5 A9A8A7 100	B7B6B5 A9A8A7 101	B7B6B5 A9A8A7 110	B7B6B5 A9A8A7 111
B4B3B2B1 A6A5A4A3 0000	O1	■	■	■	■	■	■	■
	O2	■	■	■	■	■	■	■
	O3	■	■	■	■	■	■	■
	O4	■	■	■	■	■	■	■
	O5	■	■	■	■	■	■	■
	O6	■	■	■	■	■	■	■
	O7	■	■	■	■	■	■	■
	O8	■	■	■	■	■	■	■
	O9	■	■	■	■	■	■	■
	(NUL)*	(DLE)*						
B4B3B2B1 A6A5A4A3 0001	O1	■	■	■	■	■	■	■
	O2	■	■	■	■	■	■	■
	O3	■	■	■	■	■	■	■
	O4	■	■	■	■	■	■	■
	O5	■	■	■	■	■	■	■
	O6	■	■	■	■	■	■	■
	O7	■	■	■	■	■	■	■
	O8	■	■	■	■	■	■	■
	O9	■	■	■	■	■	■	■
	(SOH)*	(DC1)*						
B4B3B2B1 A6A5A4A3 0010	O1	■	■	■	■	■	■	■
	O2	■	■	■	■	■	■	■
	O3	■	■	■	■	■	■	■
	O4	■	■	■	■	■	■	■
	O5	■	■	■	■	■	■	■
	O6	■	■	■	■	■	■	■
	O7	■	■	■	■	■	■	■
	O8	■	■	■	■	■	■	■
	O9	■	■	■	■	■	■	■
		(DC2)*						
B4B3B2B1 A6A5A4A3 0011	O1	■	■	■	■	■	■	■
	O2	■	■	■	■	■	■	■
	O3	■	■	■	■	■	■	■
	O4	■	■	■	■	■	■	■
	O5	■	■	■	■	■	■	■
	O6	■	■	■	■	■	■	■
	O7	■	■	■	■	■	■	■
	O8	■	■	■	■	■	■	■
	O9	■	■	■	■	■	■	■
	(ETX)*	(DC3)*						
B4B3B2B1 A6A5A4A3 0100	O1	■	■	■	■	■	■	■
	O2	■	■	■	■	■	■	■
	O3	■	■	■	■	■	■	■
	O4	■	■	■	■	■	■	■
	O5	■	■	■	■	■	■	■
	O6	■	■	■	■	■	■	■
	O7	■	■	■	■	■	■	■
	O8	■	■	■	■	■	■	■
	O9	■	■	■	■	■	■	■
	(EOT)*	(DC4)*						
B4B3B2B1 A6A5A4A3 0101	O1	■	■	■	■	■	■	■
	O2	■	■	■	■	■	■	■
	O3	■	■	■	■	■	■	■
	O4	■	■	■	■	■	■	■
	O5	■	■	■	■	■	■	■
	O6	■	■	■	■	■	■	■
	O7	■	■	■	■	■	■	■
	O8	■	■	■	■	■	■	■
	O9	■	■	■	■	■	■	■
	(ENG)*	(NAK)*						
B4B3B2B1 A6A5A4A3 0110	O1	■	■	■	■	■	■	■
	O2	■	■	■	■	■	■	■
	O3	■	■	■	■	■	■	■
	O4	■	■	■	■	■	■	■
	O5	■	■	■	■	■	■	■
	O6	■	■	■	■	■	■	■
	O7	■	■	■	■	■	■	■
	O8	■	■	■	■	■	■	■
	O9	■	■	■	■	■	■	■
	(ACK)*	(SYN)*						
B4B3B2B1 A6A5A4A3 0111	O1	■	■	■	■	■	■	■
	O2	■	■	■	■	■	■	■
	O3	■	■	■	■	■	■	■
	O4	■	■	■	■	■	■	■
	O5	■	■	■	■	■	■	■
	O6	■	■	■	■	■	■	■
	O7	■	■	■	■	■	■	■
	O8	■	■	■	■	■	■	■
	O9	■	■	■	■	■	■	■
	(BEL)*	(ETB)*						

*The letters in parenthesis identify the control code corresponding to the appropriate 63 bit pictorial representation. These representations were obtained from the USASI X 3.2 Code Practice Manual.

A "Filled In" Dot Represents a Low Memory Output

ASCII INPUT ADDRESS	B7B6B5 A10A9A8 000 07060504030201	B7B6B5 A10A9A8 001 07060504030201	B7B6B5 A10A9A8 010 07060504030201	B7B6B5 A10A9A8 011 07060504030201	B7B6B5 A10A9A8 100 07060504030201	B7B6B5 A10A9A8 101 07060504030201	B7B6B5 A10A9A8 110 07060504030201	B7B6B5 A10A9A8 111 07060504030201
B4B3B2B1 A7A6A5A4 1000	(BS)*	(CAN)*						
B4B3B2B1 A7A6A5A4 1001	(HT)*	(EM)*						
B4B3B2B1 A7A6A5A4 1010	(LF)*	(SUB)*						
B4B3B2B1 A7A6A5A4 1011	(VT)*	(ESC)*						
B4B3B2B1 A7A6A5A4 1100	(FF)*	(FS)*						
B4B3B2B1 A7A6A5A4 1101	(CR)*	(GS)*						
B4B3B2B1 A7A6A5A4 1110	(SO)*	(SX)*						
B4B3B2B1 A7A6A5A4 1111	(SI)*	(US)*						(DEL)*

4

*The letters in parenthesis identify the control code corresponding to the appropriate 63 bit pictorial representation. These representations were obtained from the USASI X 3.2 Code Practice Manual.

A "Filled In" Dot Represents a Low Memory Output

ASCII INPUT ADDRESS	B ₅ B ₄ A ₉ A ₈ A ₇ 000	B ₅ B ₄ A ₉ A ₈ A ₇ 001	B ₅ B ₄ A ₉ A ₈ A ₇ 010	B ₅ B ₄ A ₉ A ₈ A ₇ 011	B ₅ B ₄ A ₉ A ₈ A ₇ 100	B ₅ B ₄ A ₉ A ₈ A ₇ 101	B ₅ B ₄ A ₉ A ₈ A ₇ 110	B ₅ B ₄ A ₉ A ₈ A ₇ 111
	07060504030201	07060504030201	07060504030201	07060504030201	07060504030201	07060504030201	07060504030201	07060504030201
B ₃ B ₂ B ₁ A ₆ A ₅ A ₄ 000								
B ₃ B ₂ B ₁ A ₆ A ₅ A ₄ 001								
B ₃ B ₂ B ₁ A ₆ A ₅ A ₄ 010								
B ₃ B ₂ B ₁ A ₆ A ₅ A ₄ 011								
B ₃ B ₂ B ₁ A ₆ A ₅ A ₄ 100								
B ₃ B ₂ B ₁ A ₆ A ₅ A ₄ 101								
B ₃ B ₂ B ₁ A ₆ A ₅ A ₄ 110								
B ₃ B ₂ B ₁ A ₆ A ₅ A ₄ 111								

*These representations were obtained from the USASI X 3.2 Code Practice Manual. Address A₉ = B₇ = $\overline{B_6}$.

Bipolar Custom Character Generator ROMs

52/6290, 52/6291, 52/6292, 52/6293

Features/Benefits

- Schottky—high speed 10MHz
- Specifically designed for custom 7 x 9 row scan and 9 x 9 font character generators
- Up to 128 characters in one package
- Low power dissipation—500mW
- Standard packaging—24 pin dip
- Single 5 volt supply
- 125 ns max. access time

Applications

- A single package high speed bipolar replacement for slow multiple package MOS character generators
- CRT displays
- Printing calculators
- LED arrays
- Typesetting
- Navigation systems

Description

A 7 x 9 font row scan character has 7 outputs and 9 rows per character. The character is formed one row at a time. 9 words of a ROM with 7 outputs per word are required for each character. 128 characters required on 1152 x 7 ROM which is the size of the 5290/1, 6290/1. For custom column scan 7 x 9 characters consult the standard bipolar 7 x 9 character generator data sheet.

A 9 x 9 font character has 9 outputs and 9 rows of columns per character depending upon whether we are forming a row or column scan. 9 words of a ROM with 9 outputs per row are required for each character. 128 characters require an 1152 x 9 ROM which is the 5292/3, 6292/3.

S₃, S₂, S₁, and S₀ pins are used to scan through the 9 ROM words per character. This is usually implemented by "short counting" a 4 bit binary counter so that it counts from 0000 to 1000 (9 counts) continuously (See applications section). B₁ thru B₇ are used to pick one of the 128 characters. B₁ is the least significant binary digit and B₇ is the most significant binary digit.

The memory outputs are open collector and pullup resistors are required. The enable E₁, and E₂ must both be low to activate the part. A disabled part (E₁ or E₂ high) has high memory outputs permitting wire ORing or blanking.

Custom Font

It's easy to go from custom font to the punched card or tape format preferred by Monolithic Memories Inc. Several examples are shown. We have arbitrarily assumed that a character is formed by a series of low memory outputs in a background of high memory outputs. The assumption, of course can be reversed.

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Custom Character Generator Selection Guide

PART NUMBER	MATRIX	CHARACTERS (MAX)	SCAN	OUTPUT	TEMPERATURE	PACKAGE
6290	7x9	128	Row	OC	C	N18
5290	7x9	128	Row	OC	M	J18
6291	7x9	128	Row	TS	C	N24
5291	7x9	128	Row	TS	M	J24
6292	9x9	128	Row/Column	OC	C	N24
5292	9x9	128	Row/Column	OC	M	J24
6293	9x9	128	Row/Column	TS	C	N24
5293	9x9	128	Row/Column	TS	M	J24

Absolute Maximum Ratings

Supply voltage V_{CC}	Operating	Program
Input voltage	-0.5V to 7V	V
Off-state output voltage	-1.5V to 5.5V	V
Storage temperature range	-1.5V to 5.5V	V
	-65°C to 150°C	

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.75	5.00	5.25	V
I_{OH}	High level output current			-1.0			-2.0	mA
I_{OL}	Low level output current			6			6	mA
T_A	Operating free air temperature	-55		125	0		75	°C

Electrical Characteristics**Over Recommended Operating Free Air Temperature Range**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
V_{IH}	High-level input voltage		2			V	
V_{IL}	Low-level input voltage				0.8	V	
V_{IC}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -5.0 \text{ mA}$		-1.0	-1.5	V	
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V}, I_{OL} = 10 \text{ mA}$			0.5	V	
		$V_{IL} = 0.8\text{V}, I_{OL} = 8 \text{ mA}$			0.5		
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5\text{V}$			1.0	mA	
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4\text{V}$			40	μA	
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.45\text{V}$			-250	μA	
C_I	Input capacitance	$V_{CC} = 5.0\text{V}, f = 1\text{MHz}$		$V_I = 2.0\text{V}$	7.0	pF	
C_O	Output capacitance	$T_A = 25^\circ\text{C}$		$V_O = 2.0\text{V}$	8.0		
I_{CC}	Supply current	$V_{CC} = \text{MAX}$		OC	126	170	mA
				TS	133	180	

OPEN COLLECTOR OUTPUT CURRENT

I_{CEX}	Output leakage current	$V_{CC} = \text{MAX}, V_O = 2.4\text{V}$			100	μA
-----------	------------------------	--	--	--	-----	---------------

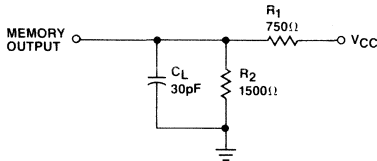
THREE STATE OUTPUT ONLY

V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V}, V_{IL} = 0.8\text{V}, I_{OH} = \text{MAX}$	2.4			V
I_{OZH}	Off-state output current high-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2\text{V}, V_O = 2.4\text{V}$			100	μA
I_{OZL}	Off-state output current low-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2\text{V}, V_O = 0.5\text{V}$			-100	μA
I_{OS}	Short-circuit output current	$V_{CC} = \text{MAX}, V_O = 0\text{V}$	-20		-90	mA

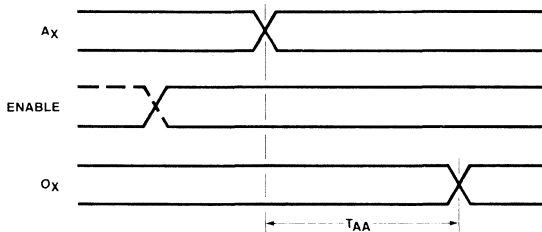
Switching Characteristics
Over Recommended Ranges of T_A and V_{CC}

SYMBOL	PARAMETER	MILITARY $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		COMMERCIAL $T_A = -0^{\circ}\text{C}$ to $+75^{\circ}\text{C}$ $V_{CC} = 5.0\text{V} \pm 5\%$		UNIT
		MIN	MAX	MIN	MAX	
t_{AA}	Address access time		150		125	ns
t_{EA}	Enable access time		85		75	ns
t_{ER}	Enable recovery time		50		40	ns

Standard Test Load



Input pulse amplitude = 3.0V.
Input pulse rise and fall times must be 5ns between 1.0V and 2.0V.
Speed measurements are made at 1.5V.
Output loading is 6mA and 30pF as given in standard load.



Note: During t_{AA}
Outputs are not
defined

Fig. 1 Access Time

A_X = Any Address
 O_X = Any Output

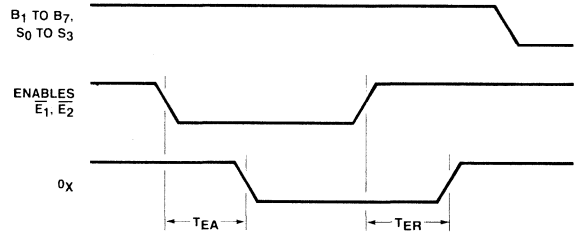
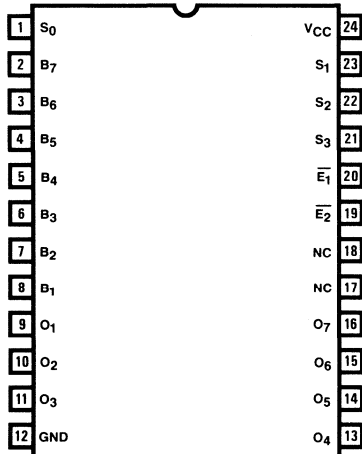


Fig. 2 Enable Access Time and Recovery Time

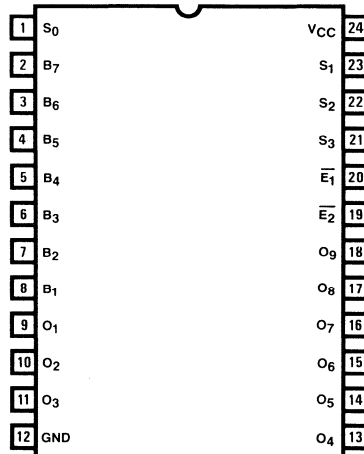
4

Pin Configuration

5290/1, 6290/1 (7 x 9 Row Scan)



5292/3, 6292/3 (9 x 9 Row or Column Scan)



Note 1): S_0, S_1, S_2, S_3 are used for the character scan.
2): Both enables must be low to activate the device.

Custom Truth Table Coding—5290/1, 6290/1

7 x 9 ROW SCAN

The characters \$, &, *, are shown below along with the ROM coding. A "filled in" dot is arbitrarily coded with a low (L)

CHARACTER SELECT							ROM WORD (DECIMAL)	OUTPUTS							FONT							
B7	B6	B5	B4	B3	B2	B1		O7	O6	O5	O4	O3	O2	O1	O7	O6	O5	O4	O3	O2	O1	
L	L	L	L	L	L	L		CHARACTER #1	0	H	H	L	H	L	H	H	□	□	■	□	■	□
							1		H	L	L	L	L	L	L	□	■	■	■	■	■	■
							2		L	H	L	H	L	H	H	■	□	■	□	■	□	□
							3		L	H	L	H	L	H	H	■	□	■	□	■	□	□
							4		H	L	L	L	L	L	H	□	■	■	■	■	■	□
							5		H	H	L	H	L	H	L	□	□	■	□	■	□	■
							6		H	H	L	H	L	H	L	□	□	■	□	■	□	■
							7		L	L	L	L	L	L	H	■	■	■	■	■	■	□
							8	H	H	L	H	L	H	H	□	□	■	□	■	□	□	
L	L	L	L	L	L	H	CHARACTER #2	9	H	L	L	H	H	H	H	□	■	■	□	□	□	□
								10	L	H	H	L	H	H	H	■	□	□	■	□	□	□
								11	L	H	H	L	H	H	H	■	□	□	■	□	□	□
								12	H	L	L	H	H	H	H	□	■	■	□	□	□	□
								13	H	L	L	H	H	H	H	□	■	■	□	□	□	□
								14	L	H	H	L	H	L	H	■	□	□	■	□	■	□
								15	L	H	H	H	L	L	H	■	□	□	□	■	■	□
								16	L	H	H	H	H	L	H	■	□	□	□	□	■	□
H	H	H	H	H	H	H	CHARACTER #128	1143	H	H	H	L	H	H	H	□	□	□	■	□	□	□
								1144	L	H	H	L	H	H	L	■	□	□	■	□	□	■
								1145	H	L	H	L	H	L	H	□	■	□	■	□	■	□
								1146	H	H	L	L	L	H	H	□	□	■	■	■	□	□
								1147	H	H	H	L	H	H	H	□	□	□	■	□	□	□
								1148	H	H	L	L	L	H	H	□	□	■	■	■	□	□
								1149	H	L	H	L	H	L	H	□	■	□	■	□	■	□
								1150	L	H	H	L	H	H	L	■	□	□	■	□	□	■
							1151	H	H	H	L	H	H	H	□	□	□	■	□	□	□	

Use of Custom Truth Table Form—5290/1, 6290/1

Truth table forms are available from Monolithic Memories upon request. For customers desiring to make their own forms an example is shown below coded to the 7 x 9 Row Scan example:

WORD NUMBER	OUTPUTS						
	PIN 16 O7	15 O6	14 O5	13 O4	11 O3	10 O2	9 O1
0	H	H	L	H	L	H	H
1	H	L	L	L	L	L	L
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
1151	H	H	H	L	H	H	H

NOTE:
A high voltage on the data out lines is signified by an "H". A low voltage on the data out lines is signified by an "L". The word number assumes positive logic on the address pin so for example word 511 = HHHHHHHH.

Custom Truth Table Coding—5292/3, 6292/3

9 x 9 COLUMN SCAN

The characters \$, &, *, can be seen in the font if this page is rotated 90° clockwise. A "filled in" dot is arbitrarily coded with a low (L).

9 x 9 ROW SCAN

The 9 x 9 row scan translation would be similar to the 7 x 9 row scan previously shown except that there would be a 9 x 9 font for each character and outputs 8 and 9 in the ROM would be used and coded.

CHARACTER SELECT								ROM WORD (DECIMAL)	OUTPUTS									FONT								
B7	B6	B5	B4	B3	B2	B1	O9		O8	O7	O6	O5	O4	O3	O2	O1	O9	O8	O7	O6	O5	O4	O3	O2	O1	
L	L	L	L	L	L	L	CHARACTER #1	8	H	L	H	H	H	L	L	H	H	□	■	□	□	□	■	■	□	□
L	L	L	L	L	L	L		7	H	L	H	H	L	H	H	L	H	□	■	□	□	■	□	□	■	□
L	L	L	L	L	L	L		6	H	L	H	H	L	H	H	L	H	□	■	□	□	■	□	□	■	□
L	L	L	L	L	L	L		5	L	L	L	L	L	L	L	L	L	■	■	■	■	■	■	■	■	■
L	L	L	L	L	L	L		4	H	L	H	H	L	H	H	L	H	□	■	□	□	■	□	□	■	□
L	L	L	L	L	L	L		3	L	L	L	L	L	L	L	L	L	■	■	■	■	■	■	■	■	■
L	L	L	L	L	L	L		2	H	L	H	H	L	H	H	L	H	□	■	□	□	■	□	□	■	□
L	L	L	L	L	L	L		1	H	L	H	H	L	H	H	L	H	□	■	□	□	■	□	□	■	□
L	L	L	L	L	L	L		0	H	H	L	L	H	H	H	L	H	□	□	■	■	□	□	□	■	□
L	L	L	L	L	L	H		CHARACTER #2	17	H	H	H	H	H	H	H	H	H	□	□	□	□	□	□	□	□
L	L	L	L	L	L	H	16		H	H	H	H	H	L	H	L	□	□	□	□	□	□	■	□	■	
L	L	L	L	L	L	H	15		H	H	H	H	H	L	L	H	□	□	□	□	□	□	■	■	□	
L	L	L	L	L	L	H	14		H	H	H	H	H	L	H	L	□	□	□	□	□	□	■	□	■	
L	L	L	L	L	L	H	13		H	L	L	L	L	H	H	L	□	■	■	■	■	■	□	□	■	
L	L	L	L	L	L	H	12		L	H	H	L	L	H	H	L	■	□	□	■	■	□	□	□	■	
L	L	L	L	L	L	H	11		L	H	H	L	L	H	H	L	■	□	□	■	■	□	□	□	■	
L	L	L	L	L	L	H	10		L	H	H	L	L	H	H	L	■	□	□	■	■	□	□	□	■	
L	L	L	L	L	L	H	9		H	L	L	H	H	L	L	H	□	■	■	□	□	■	■	□	□	
H	H	H	H	H	H	H	CHARACTER #128		1151	H	H	H	H	H	H	H	H	□	□	□	□	□	□	□	□	□
H	H	H	H	H	H	H		1150	H	L	H	H	H	H	L	H	□	■	□	□	□	□	□	■	□	
H	H	H	H	H	H	H		1149	H	H	L	H	H	L	H	H	□	□	■	□	□	□	□	■	□	
H	H	H	H	H	H	H		1148	H	H	H	L	H	L	H	H	□	□	□	■	□	■	□	□	□	
H	H	H	H	H	H	H		1147	L	L	L	L	L	L	L	L	■	■	■	■	■	■	■	■	■	
H	H	H	H	H	H	H		1146	H	H	H	L	H	L	H	H	□	□	□	■	□	■	□	□	□	
H	H	H	H	H	H	H		1145	H	H	L	H	H	L	H	H	□	□	■	□	□	□	■	□	□	
H	H	H	H	H	H	H		1144	H	L	H	H	H	H	L	H	□	■	□	□	□	□	□	■	□	
H	H	H	H	H	H	H		1143	H	H	H	H	H	H	H	H	□	□	□	□	□	□	□	□	□	

4

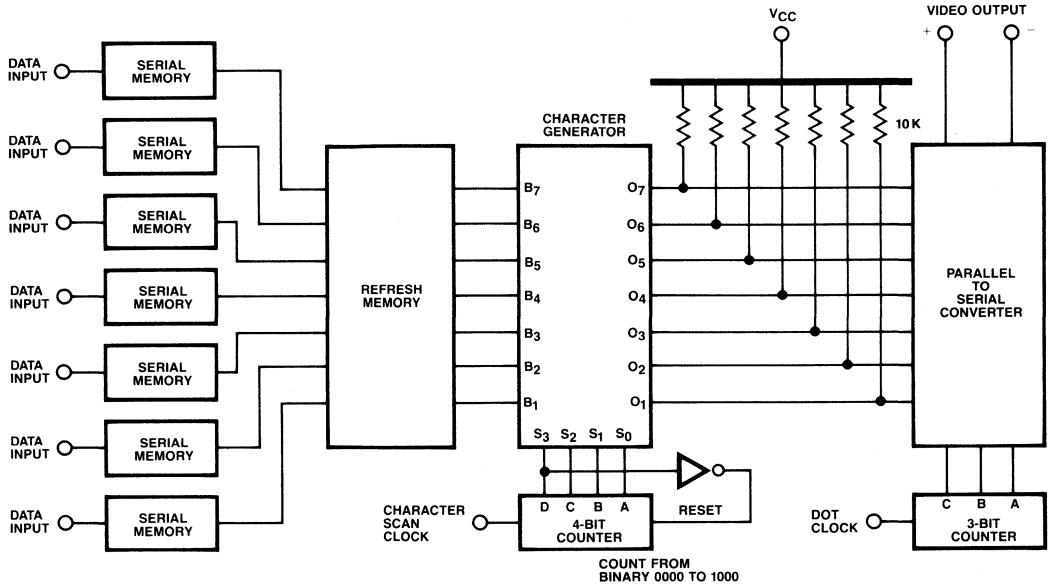
Use of Custom Truth Table Form—5292/3, 6292/3

Truth table forms are available from Monolithic Memories upon request. For customers desiring to make their own forms an example is shown below coded to the 9 x 9 column scan example:

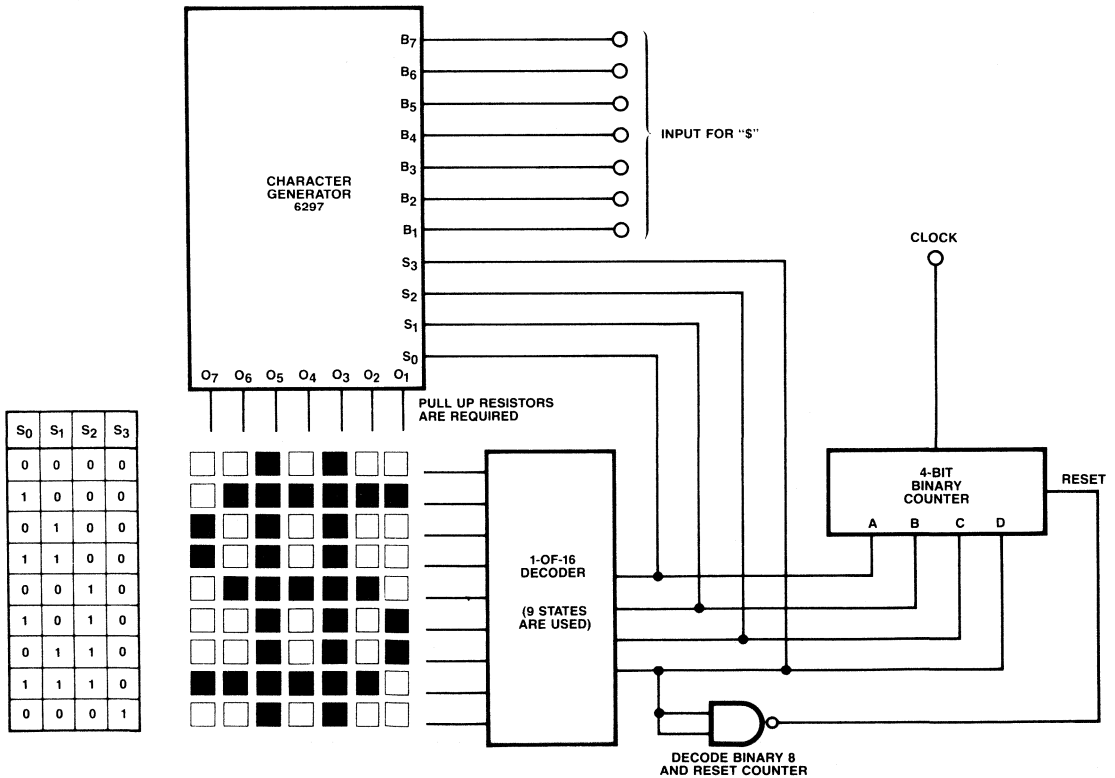
WORD NUMBER	OUTPUTS									
	PIN	18 O9	17 O8	16 O7	15 O6	14 O5	13 O4	11 O3	10 O2	9 O1
0		H	H	L	L	H	H	H	L	H
1		H	L	H	H	L	H	H	L	H
•		•	•	•	•	•	•	•	•	•
•		•	•	•	•	•	•	•	•	•
•		•	•	•	•	•	•	•	•	•
1151		H	H	H	H	H	H	H	H	H

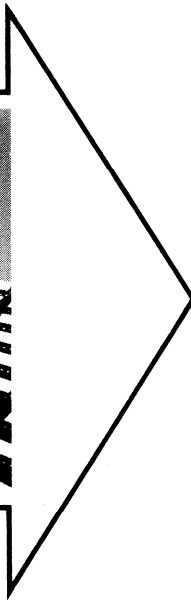
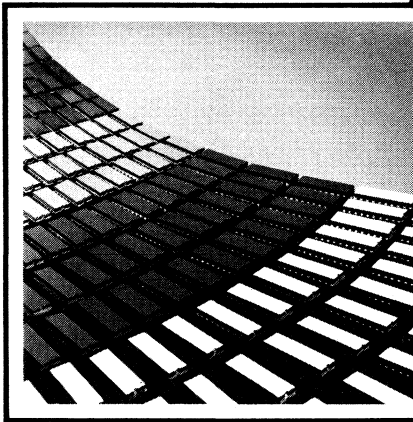
NOTE:
A high voltage on the data out lines is signified by an "H". A low voltage on the data out lines is signified by an "L". The word number assumes positive logic on the address pin so for example word 511 = HHHHHHHH.

CRT Character Display Block Diagram



Generation of the Character "\$" in a 7x9 Row Scan





Introduction	1
PROMS	2
ROMS	3
Character Generators	4
RAMS	5
Programmable Logic	6
LSI Logic	7
Arithmetic Elements	8
Interface	9
General Information	10
Representatives/Distributors	11

64-Bit (16 x 4) Random Access Memory 5560/6560, 5561/6561

Features/Benefits

- Advanced Schottky processing.
- Low input current (250 μ A maximum).
- Data outputs are off during a write cycle.
- Fully decoded and TTL compatible.
- Open collector or three state outputs.
- The 6560 is pin compatible with the 3101A.

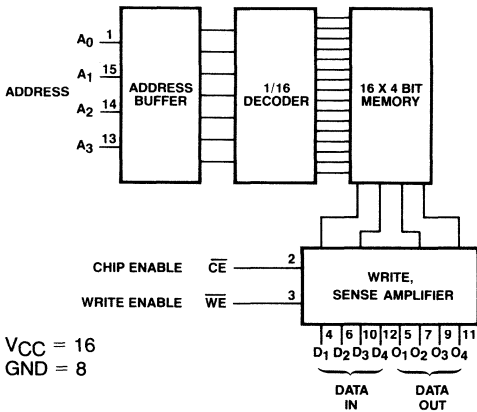
Applications

- Scratch pad registers for accumulators and buffer memories.
- Push down stacks.

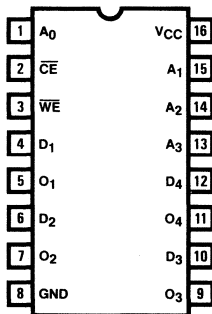
Selection Guide

Part Number	Package	Output	Temperature Range
6560	N16	OC	0° to +75°C
6561	N16	TS	0° to +75°C
5560	J16, F16	OC	-55°C to +125°C
5561	J16, F16	TS	-55°C to +125°C

Block Diagram



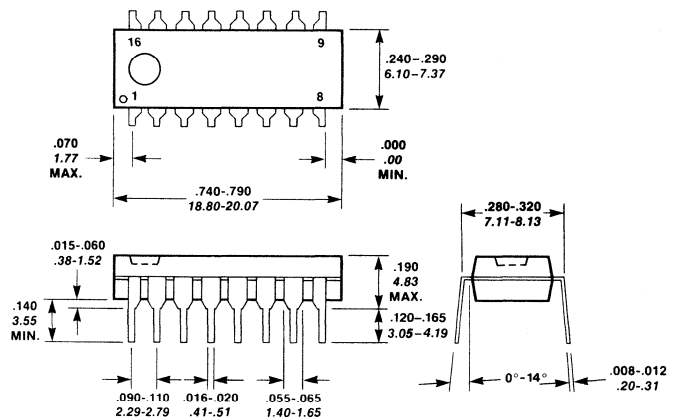
Pin Configuration



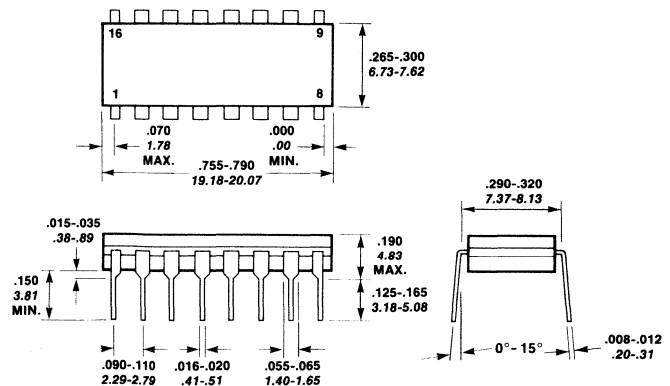
DATA IN = DATA OUT

Package Drawings

N16 Plastic DIP



J16 Ceramic DIP



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES.
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.

Absolute Maximum Ratings

Supply voltage V_{CC}	Operating -0.5V to 7V
Input voltage	-1.5V to 5.5V
Off-state output voltage	-1.5V to 5.5V
Storage temperature range	-65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.75	5.00	5.25	V
I_{OH}	High level output current			-3.2			-3.2	mA
I_{OL}	Low level output current			10			15	mA
T_A	Operating free air temperature	-55		125	0		75	°C

Electrical Characteristics

Over Recommended Operating Free Air Temperature Range

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
V_{IH}	High-level input voltage	$V_{CC} = 5.0V$	2			V	
V_{IL}	Low-level input voltage	$V_{CC} = 5.0V$			0.8	V	
V_{IC}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -5.0 \text{ mA}$			-1.0	V	
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2V,$ $V_{IL} = 0.8V$			0.5	V	
		$I_{OL} = 10 \text{ mA}$ $I_{OL} = 15 \text{ mA}$			0.5		
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5V$			1.0	mA	
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4V$			40	μA	
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.45V$			-250	μA	
C_I	Input capacitance	$V_{CC} = 5.0V, f = 1\text{MHz}$		$V_I = 2.0V$	7.0	pF	
C_O	Output capacitance	$T_A = 25^\circ C$		$V_O = 2.0V$	8.0		
I_{CC}	Supply current	$V_{CC} = 5.0V$ inputs		OC	70	105	mA
		Gnd and outputs open		TS	75	125	

OPEN COLLECTOR OUTPUT CURRENT

I_{CEX}	Output Leakage Current	$V_{CC} = \text{MAX}, V_O = 2.4V$			100	μA
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THREE STATE OUTPUT ONLY

V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2V,$ $V_{IL} = 0.8V, I_{OH} = \text{MAX}$	2.4			V
I_{OZH}	Off-state output current high-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2V,$ $V_O = 2.4V$			100	μA
I_{OZL}	Off-state output current low-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2V,$ $V_O = 0.5$			-100	μA
I_{OS}	Short-circuit output current	$V_{CC} = 5.0, V_O = 0V$	-20		-90	mA

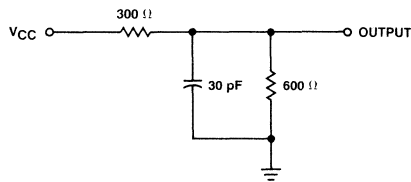
Switching Characteristics

With Standard Load (Fig. 1)

SYMBOL	PARAMETER	FIGURE	5560/5561		6560/6561		UNIT
			5.0V \pm 10%, MIN	-55 to 125°C MAX	5.0V \pm 5%, MIN	0 to 75°C MAX	
T _{AA}	Address access time	2	10	75	10	50	ns
T _{EA}	Enable access time	2	5.0	40	5.0	35	ns
T _{ER}	Enable recovery time	2	5.0	35	5.0	35	ns
T _{WP}	Write pulse width*	3	50		35		ns
T _{WH}	Write enable to output high time	3		50		35	ns
T _{DWO}	Data in and write enable overlap time	3	50		35		ns
T _{WSA}	Address to write enable set-up time	3	0		0		ns
T _{WHA}	Address to write enable hold time	3	0		0		ns
T _{WSCS}	Chip enable to write enable set-up time	3	10		10		ns
T _{WHCH}	Chip enable to write enable hold time	3	0		0		ns

*Write recovery time is less than T_{AA}**5561/6561 ONLY**

T _{ON}	Chip enable to low impedance delay		5		5		ns
T _{OFF}	Chip enable to high impedance delay			35		25	ns

5**Standard Test Circuit****Standard Load
(Commercial)**

Input Pulse Amplitude = 3.0V
 Input Rise and Fall Time
 5.0 ns From 1.0V to 2.0V
 Measurements Made at 1.50V

Figure 1

Waveforms

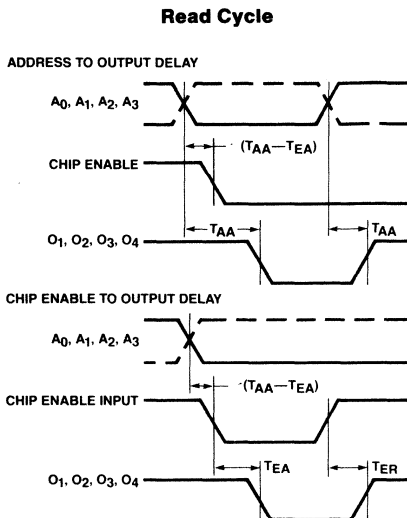


Figure 2

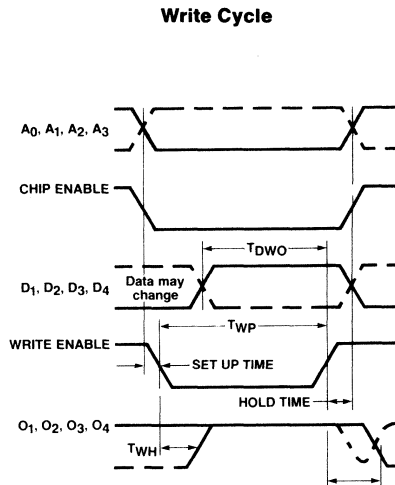


Figure 3

Functional Table

CHIP ENABLE	WRITE ENABLE	OPERATION	DATA OUTPUTS	
			5560/6560	5561/6561
LOW	LOW	WRITE	5560/6560	OFF
			5561/6561	HIGH IMPEDANCE STATE
LOW	HIGH	READ	COMPLEMENT OF WRITTEN DATA	
HIGH	DON'T CARE	HOLD	5560/6560	OFF
			5561/6561	HIGH IMPEDANCE STATE

Memory Operation

READ: The memory is addressed with the A_0 — A_3 inputs which selects one of the 16 words. The chip is enabled by making the chip enable LOW. If the chip enable is HIGH chip is disabled. If the write enable is HIGH and the chip is enabled the stored data is read out on the data out pin. The data read out is the **COMPLEMENT** of the data written in during the write cycle.

WRITE: The memory is addressed with the A_0 — A_3 inputs which selects one of the 16 4-bit words. The chip is enabled as in the read cycle. If the write enable is LOW the data on the data input pin is written into the addressed word. The data out pins of the memory during the write cycle will be kept OFF in the case of the 5560/6560 and in the third state (high impedance state) for the 5561/6561, by control of internal circuitry. Some memory devices may write in as fast as 10 ns so address and write enable timing must be carefully controlled, when the memory is operated with the enable activated throughout the cycle.

Memory Expansion Rules

- TO EXPAND THE NUMBER OF BITS IN THE WORD:**
Tie corresponding address pins together, tie write enable pins together, and bring data in and data out independently.
- TO EXPAND THE NUMBER OF WORDS:**
Tie corresponding address pins together, tie write enable pins and corresponding data in and data out pins together, and use the higher order system addresses in conjunction with the chip enable to pick one row of packages.

Low Power 64-Bit (16x4) Random Access Memory L5560/L6560, L5561/L6561

Features/Benefits

- Typical power dissipation of 125 mW.
- 100 n maximum access time over 0°C to 75°C and $\pm 5\%$ voltage variation (L6560/L6561).
- 120 ns maximum access time over -55°C to 125°C and $\pm 10\%$ voltage variation (L5560/L5561).
- Low input current (125 μ A maximum).
- Open collector or three-state outputs.

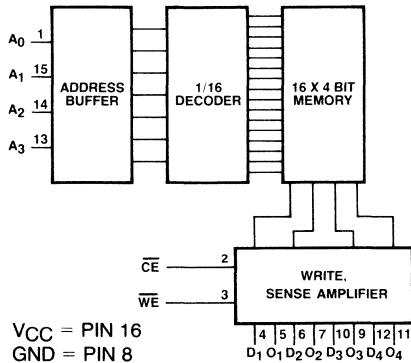
Selection Guide

PART NUMBER	PACKAGE	OUTPUT	TEMPERATURE RANGE
L6560	N16	OC	0° to +75°C
L6561	N16	TS	0° to +75°C
L5560	J16, F16	OC	-55°C to +125°C
L5561	J16, F16	TS	-55°C to +125°C

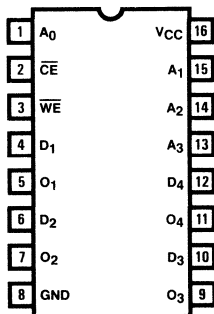
Applications

- Scratch pad registers for accumulators and buffer memories.
- Push down stacks.

Block Diagram



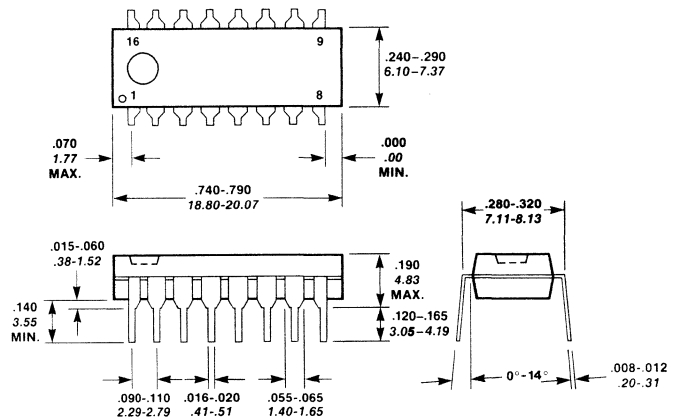
Pin Configuration



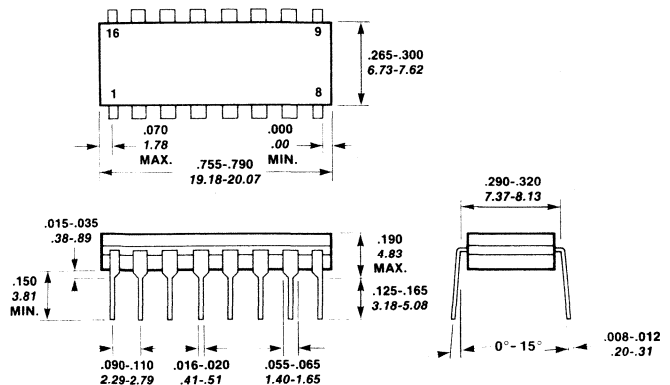
DATA IN = DATAOUT

Package Drawings

N16 Plastic DIP



J16 Ceramic DIP



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES.
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.

5

Absolute Maximum Ratings

Supply voltage V_{CC}	Operating -0.5V to 7V
Input voltage	-1.5V to 5.5V
Off-state output voltage	-1.5V to 5.5V
Storage temperature range	-65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.75	5.00	5.25	V
I_{OH}	High-level output current			-1.6			-1.6	mA
I_{OL}	Low-level output current			4.8			4.8	mA
T_A	Operating free air temperature	-55		125	0		75	°C

Electrical Characteristics

Over Recommended Operating Free Air Temperature Range

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	$V_{CC} = 5.0V$	2			V
V_{IL}	Low-level input voltage	$V_{CC} = 5.0V$			0.8	V
V_{IC}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -5.0 \text{ mA}$			-1.0	V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2V,$ $V_{IL} = 0.8V, I_{OL} = \text{MAX}$			0.5	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5V$			1.0	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4V$			40	μA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.45V$			-250	μA
C_I	Input capacitance	$V_{CC} = 5.0V, f = 1\text{MHz}$		7.0		pF
C_O	Output capacitance	$T_A = 25^\circ C$		8.0		
I_{CC}	Supply current	$V_{CC} = 5.0V$ inputs Gnd and outputs open	L6560, 61	25	48	mA
		L5560, 61	25	54		

OPEN COLLECTOR OUTPUT CURRENT

I_{CEX}	Output Leakage Current	$V_{CC} = \text{MAX}, V_O = 2.4V$	100	μA
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THREE STATE OUTPUT ONLY

V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2V,$ $V_{IL} = 0.8V, I_{OH} = \text{MAX}$	2.4		V
I_{OZH}	Off-state output current high-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2V,$ $V_O = 2.4V$		100	μA
I_{OZL}	Off-state output current low-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2V,$ $V_O = 0.5$		-100	μA
I_{OS}	Short-circuit output current	$V_{CC} = 5.0, V_O = 0V$	-20	-90	mA

Switching Characteristics

With Standard Load (Fig. 1)

SYMBOL	PARAMETER	FIGURE	L5560/L5561 5.0V ± 10%, -55 to 125°C		L6560/L6561 5.0V ± 5%, 0 to 75°C		UNIT
			MIN	MAX	MIN	MAX	
T _{AA}	Address access time	2	20	120	20	100	ns
T _{EA}	Enable access time	2	10	90	10	65	ns
T _{ER}	Enable recovery time	2	10	90	10	65	ns
T _{WP}	Write pulse width *	3	125		80		ns
T _{DWO}	Data in and write enable overlap time	3	125		80		ns
T _{WSA}	Address to write enable set-up time	3	0		0		ns
T _{WHA}	Address to write enable hold time	3	0		0		ns
T _{WSES}	Chip enable to write enable set-up time	3	20		20		ns
T _{WHCH}	Chip enable to write enable hold time	3	0		0		ns
T _{WH}	Write enable to output high	3	100		75		ns

*Write recovery time is less than T_{AA}

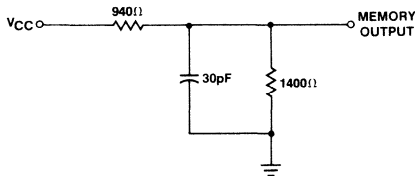
5561/6561 ONLY

T _{ON}	Chip enable to low impedance delay		5		5		ns
T _{OFF}	Chip enable to high impedance delay			75		55	ns

Standard Test Circuit

5

Standard Load



Input Pulse Amplitude = 3.0V
 Input Rise and Fall Time
 5.0 ns From 1.0V to 2.0V
 Measurements Made at 1.50V

Figure 1

Waveforms

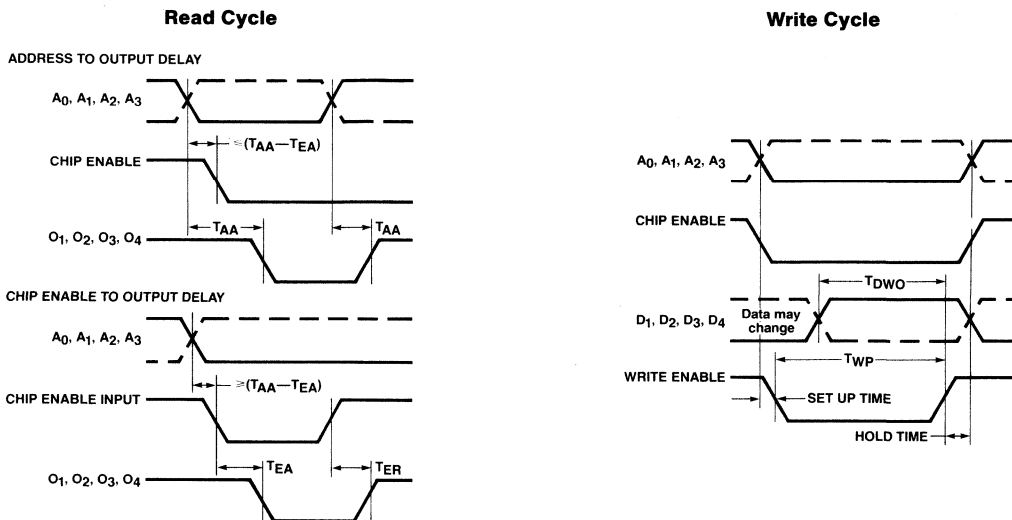


Figure 3

Functional Table

CHIP ENABLE	WRITE ENABLE	OPERATION	DATA OUTPUTS	
LOW	LOW	WRITE	L5560/L6560	OFF
			L5561/L6561	HIGH IMPEDANCE STATE
LOW	HIGH	READ	COMPLEMENT OF WRITTEN DATA	
HIGH	DON'T CARE	HOLD	L5560/L6560	OFF
			L5561/L6561	HIGH IMPEDANCE STATE

Memory Operation

READ: The memory is addressed with the A₀—A₃ inputs which selects one of the 16 words. The chip is enabled by making the chip enable LOW. If the chip enable is HIGH the chip is disabled. If the write enable is HIGH and the chip is enabled the stored data is read out on the data out pin. The data read out is the COMPLEMENT of the data written in during the write cycle.

WRITE: The memory is addressed with the A₀—A₃ inputs which selects one of the 16, 4-bit words. The chip is enabled as in the read cycle. If the write enable is LOW the data on the data input pin is written into the addressed word. The data out pins of the memory during the write cycle will be the complement of the data inputs for the L5560/L6560 (assuming a pullup resistor is attached) and in the third state (high impedance state) for the L5561/L6561. Some memory devices may write in as fast as 15 ns so address and write enable timing must be carefully controlled, when the memory is operated with the enable activated throughout the cycle.

Memory Expansion Rules

1. TO EXPAND THE NUMBER OF BITS IN THE WORD:
Tie corresponding address pins together, tie write enable pins together, and bring data in and data out independently.
2. TO EXPAND THE NUMBER OF WORDS:
Tie corresponding address pins together, tie write enable pins and corresponding data in and data out pins together, and use the higher order system addresses in conjunction with the chip enable to pick one row of packages.

64-bit (16x4) Edge Triggered Register 75S68 / 85S68

Features/Benefits

- On chip output register.
- Edge triggered write.
- High speed 30 ns typ.
- Three-state output.
- Both military (75S68) and commercial (85S68) operating temperature ranges.
- Optimized for register stack applications.
- Pin and performance compatible with the National part.
- 18-pin package.

Description

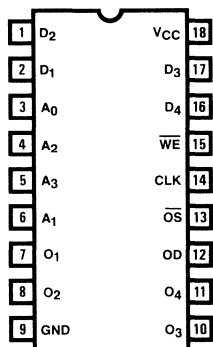
The 85S68 is an addressable "D" register file. Any of its 16 four-bit words may be asynchronously read or may be written into on the next clock transition. An input terminal is provided to enable or disable the synchronous writing of the input data into the location specified by the address terminals. An output disable terminal operates only as a three-state output control terminal. The addressable register data may be latched at the outputs and retained as long as the output store terminal is held in a low state. This memory storage condition is independent of the state of the output disable terminal.

All input terminals are high impedance at all times, and all outputs have low impedance active drive logic states and the high impedance three-state condition.

Applications

The 85S68 can enhance the dynamic performance of a TTL processor, since it may safely operate using single phase clocking instead of the multiphase clocking systems being used currently. This simple feature not only enhances the system's dynamic performance, since multiple levels of registers need not be activated, but also reduces component count by elimination of one set of buffer registers.

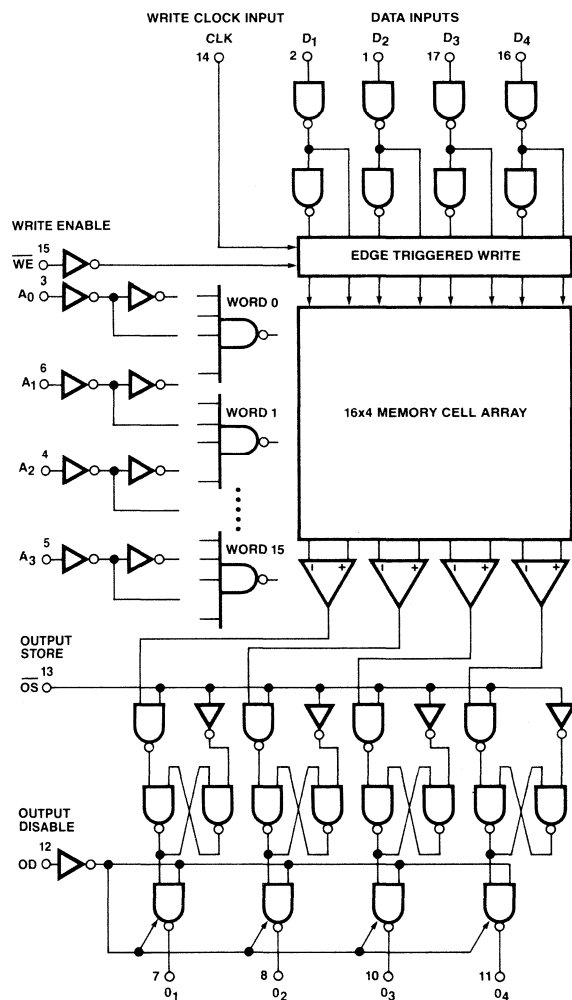
Pin Configuration



Selection Guide

PART NUMBER	PACKAGE	OUTPUT	TEMPERATURE RANGE
85S68	N16	TS	0° to +75°C
75S68	J16	TS	-55°C to +125°C

Logic Diagram



5

Absolute Maximum Ratings

Supply voltage V_{CC}	Operating -0.5V to 7V
Input voltage	-1.5V to 5.5V
Off-state output voltage	-1.5V to 5.5V
Storage temperature range	-65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.75	5.00	5.25	V
I_{OH}	High level output current			-5.2			-5.2	mA
I_{OL}	Low level output current			16			16	mA
T_A	Operating free air temperature	-55		125	0		75	°C

Electrical Characteristics**Over Recommended Operating Free Air Temperature Range**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IC}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18\text{mA}$			-1.2	V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V}$ $V_{IL} = 0.8\text{V}, I_{OL} = \text{MAX}$			0.50	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5\text{V}$			1.0	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}$ $V_I = 2.4\text{V}$	Clock input		50	μA
			All others		40	
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}$ $V_I = 0.5\text{V}$	Clock input		-500	μA
			All others		-250	
C_I	Input capacitance	$V_{CC} = 5.0\text{V}$ $V_I = 2.0\text{V}$		7.0		pF
C_O	Output capacitance	$f = 1\text{MHz}, T_A = 25^\circ\text{C}$ $V_O = 2.0\text{V}$		8.0		pF
I_{CC}	Supply current	$V_{CC} = \text{MAX}$		70	100	mA

THREE STATE OUTPUT

V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V}$ $V_{IL} = 0.8\text{V}, I_{OH} = \text{MAX}$	2.4			V
I_{OZH}	Off-state output current high-level voltage supplied	$V_{CC} = \text{MAX}, V_{IH} = 2\text{V}$ $V_O = 2.4\text{V}$			40	μA
I_{OZL}	Off-state output current low-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2\text{V}$ $V_O = 0.5\text{V}$			-40	μA
I_{OS}	Short-circuit output current	$V_{CC} = \text{MAX}, V_O = 0\text{V}$	-20		-55	mA

Switching Characteristics

Over Recommended Operating Range of T_A and V_{CC}

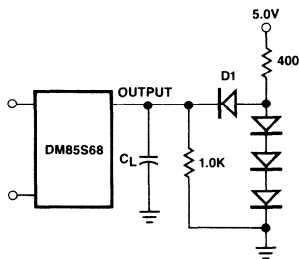
SYMBOL	PARAMETER	85S68			75S68			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{ZH}	Output enable to high level		20	35		20		ns
t_{ZL}	Output enable to low level		14	24		14		ns
t_{HZ}	Output disable time from high level		10	15		10		ns
t_{LZ}	Output disable time from low level		12	18		12		ns
t_{AA}	Access time	Address to output		30	40	30		ns
t_{DSA}		Output store to output		20	30	20		
t_{CA}		Clock to output		25	40	25		
t_{ASC}	Set-up time	Address to clock		15	5	5		ns
t_{DSC}		Data to clock		5	5	5		
t_{ASDS}		Address to output store		30	0	0		
t_{WESC}		Write enable set-up time		5	15	15		
t_{DSSC}		Store before write (t_{10})		10	0	0		
t_{AHC}	Hold time	Address from clock		10	5	5		ns
t_{DHC}		Data from clock		15	5	5		
t_{AHDS}		Address from output store		5	0	0		
t_{WEHC}		Write enable hold time		15	5	5		

Functional Table

OD	\overline{WE}	CLK	\overline{OS}	MODE	OUTPUTS
0	X	X	0	Output Store	Data From Last Addressed Location
X	0	\square	X	Write Data	Dependent on State of OD and \overline{OS}
0	X	X	1	Read Data	Data Stored in Addressed Location
1	X	X	0	Output Store	High Impedance State
1	X	X	1	Output Disable	High Impedance State

5

Test Circuit



$C_L = 5.0$ pF for t_{HZ} , t_{LZ}
 $C_L = 30$ pF for all others
 C_L includes probe and jig capacitance
 All diodes are 1N3064

Switching Waveforms

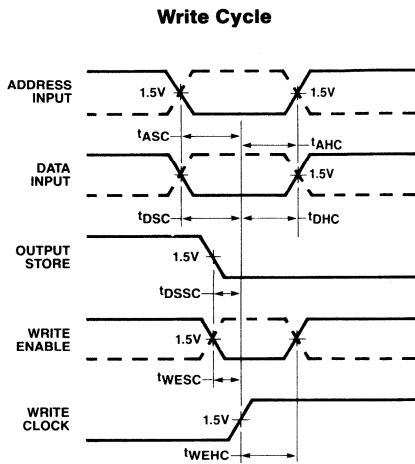


Figure 2. Clock Set-Up and Hold Time

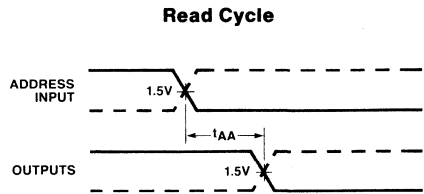


Figure 4. Address to Output Access Time

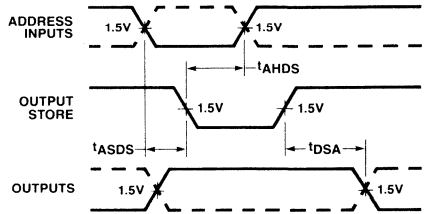


Figure 5. Output Store Access, Set-Up and Hold Time

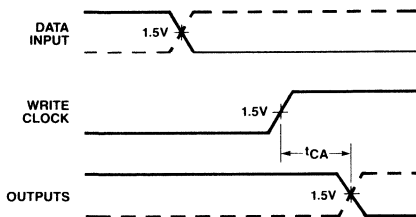


Figure 3. Clock to Output Access

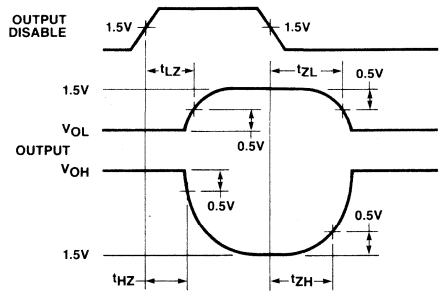


Figure 6. Output Enable to Disable Time

NOTE: Input waveforms supplied by pulse generator having the following characteristics: $V = 3.0V$, $t_R \leq 2.5ns$, $PRR \leq 1.0$ MHz and $Z_{OUT} = 50\Omega$.

64-Bit Random Access Memory (Non-Inverting)

29700, 29701

Features/Benefits

- Fully decoded 16-word x 4-bit Schottky technology high-speed RAM.
- Ultra fast access time typically 17ns.
- Non-inverting
- Available with three-state outputs (29701) or with open collector outputs (29700).
- Pin compatible with AMD's AM29700,01 respectively

Applications

- Scratch Pad registers for accumulators and buffer memories
- Push down stacks

Description

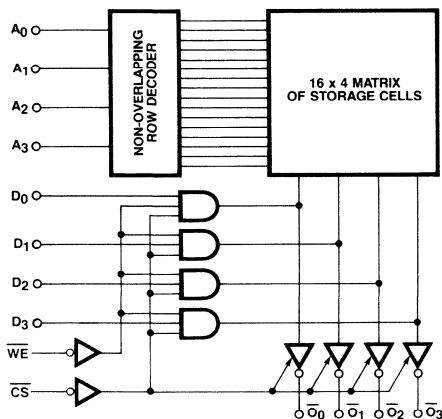
The 29700 and 29701 are 64-bit RAMs built using Schottky diode clamped transistors and are ideal for use in scratch pad and high-speed buffer memory applications. Each memory is organized as a fully decoded 16-word memory of 4 bits per word. Easy memory expansion is provided by an active LOW chip select (\overline{CS}) input and open collector OR tieable outputs (29700) or three-state outputs (29701). Chip selection for large memory systems can be controlled by active LOW output decoders.

An active LOW Write line \overline{WE} controls the writing/reading operation of the memory. When the chip select and write lines are LOW the information on the four data inputs D_0 to D_3 is written into the addressed memory word.

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the four outputs \overline{O}_0 to \overline{O}_3 .

During the writing operation or when the chip select line is HIGH the four outputs of the memory go to an inactive high impedance state.

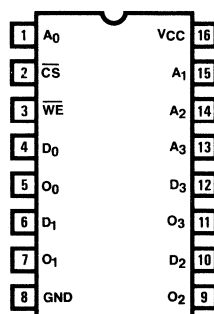
Block Diagram



Selection Guide

PART NUMBER	PACKAGE	OUTPUT	TEMPERATURE RANGE
29700NC	N16	OC	0°C to +75°C
29700JC	J16	OC	0°C to +75°C
29701NC	N16	TS	0°C to +75°C
29701JC	J16	TS	0°C to +75°C
29700JM	J16	OC	-55°C to +125°C
29700FM	F16	OC	-55°C to +125°C
29701JM	J16	TS	-55°C to +125°C
29701FM	F16	TS	-55°C to +125°C

Pin Configuration



Absolute Maximum Ratings

Supply voltage V_{CC}	Operating 7V
Input voltage	5.5V
Off-state output voltage	5.5V
Storage temperature range	-65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.75	5.00	5.25	V
I_{OH}	High level output current			-2.0			-5.2	mA
I_{OL}	Low level output current			16			20	mA
T_A	Operating free air temperature	-55		125	0		75	°C

Electrical Characteristics**Over Recommended Operating Free Air Temperature Range**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
V_{IC}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2	V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V},$ $V_{IL} = 0.8\text{V}$	$I_{OL} = 8 \text{ mA}$		0.45	V
			$I_{OL} = 10 \text{ mA}$		0.5	
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5\text{V}$			1.0	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4\text{V}$			10	μA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4\text{V}$			100	μA
C_I	Input Capacitance	$V_{CC} = 5.0\text{V}, f = 1 \text{ MHz}$ $T_A = 25^\circ\text{C}$	$V_I = 2.0\text{V}$		6	pF
C_O	Output Capacitance			$V_O = 2.0\text{V}$		8
I_{CC}	Supply current	$V_{CC} = \text{MAX}; \text{All inputs GND.}$			75 105	mA

OPEN COLLECTOR OUTPUT CURRENT

I_{CEX}	Output Leakage Current	$V_{CC} = \text{MAX}, V_O = 2.4\text{V}$			100	μA
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THREE STATE OUTPUT ONLY

V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V},$ $V_{IL} = 0.8\text{V}, I_{OH} = \text{MAX}$	2.4	3.6		V
I_{OZH}	Off-state output current high-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2\text{V},$ $V_O = 2.4\text{V}$			40	μA
I_{OZL}	Off-state output current low-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2\text{V},$ $V_O = 0.4\text{V}$			-40	μA
I_{OS}	Short-circuit output current	$V_{CC} = \text{MAX}$	-20	-45	-90	mA

Switching Characteristics Over Operating Range (Unless Otherwise Noted)

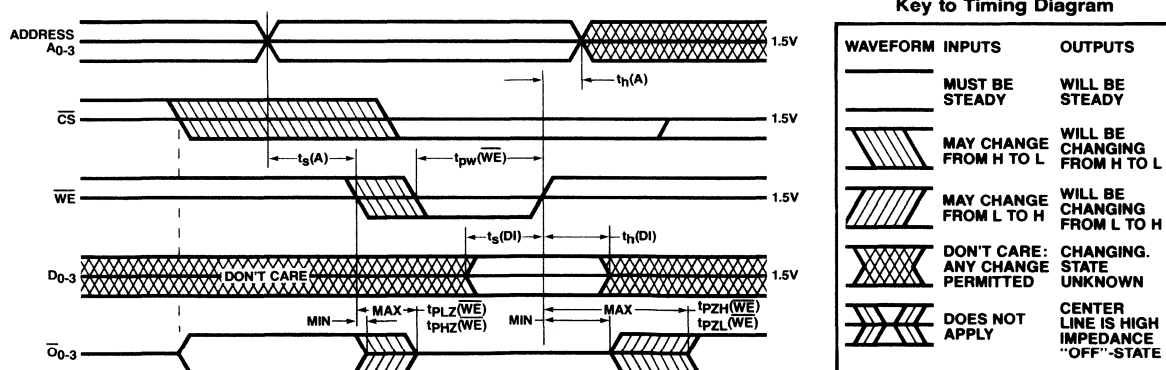
PARAMETERS	DESCRIPTION		A.C. TEST CONDITIONS	TYP	COM'L		MIL		UNITS
				(NOTE 1)	MIN	MAX	MIN	MAX	
t _{PLH} (A)	Delay from Address to Output	See Fig. 2	Fig. 3 test load (measured to output = 1.5V)	15	25	30	ns		
t _{PHL} (A)									
t _{PZH} (CS)	Delay from Chip Select (LOW) to Active Output and Correct Data	See Fig. 2		10	15	20	ns		
t _{PZL} (CS)									
t _{PZH} (WE)	Delay from Write Enable (HIGH) to Active Output and Correct Data (Write Recovery—See Note 2)	See Fig. 1		12	20	25	ns		
t _{PZL} (WE)									
t _s (A)	Set-up Time Address (Prior to Initiation of Write)	See Fig. 1		-6.0	0	0	ns		
t _h (A)	Hold Time Address (After Termination of Write)	See Fig. 1		-2.5	0	0	ns		
t _s (DI)	Set-up Time Data Input (Prior to Termination of Write)	See Fig. 1		9.0	20	25	ns		
t _h (DI)	Hold Time Data Input (After Termination of Write)	See Fig. 1		-4.0	0	0	ns		
t _{pw} (WE)	Min. Write Enable Pulse Width to Insure Write	See Fig. 1		10	20	25	ns		
t _{PHZ} (CS)	Delay from Chip Select (HIGH) to Inactive Output (HI-Z)	See Fig. 2		10	15	20	ns		
t _{PLZ} (CS)									
t _{PLZ} (WE)	Delay from Write Enable (LOW) to Inactive Output (HI-Z)	See Fig. 1	12	20	25	ns			
t _{PHZ} (WE)									

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.

2. Output is preconditioned to data in (non-inverted) during write to insure correct data is present on all outputs when write is terminated. (No write recovery glitch)

5

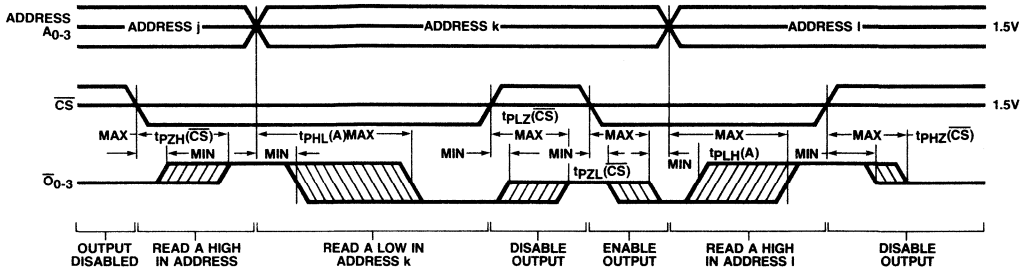
Switching Waveforms



Write Cycle Timing. The cycle is initiated by an address change. After t_s(A) min., the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, t_h(A) min. must be allowed before the address may be changed again. The output will be inactive (floating for the 27S03A) while the write enable is LOW.

Figure 1.

Switching Waveforms (Cont.)



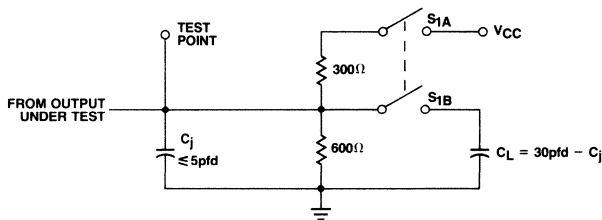
Switching delays from address and chip select inputs to the data output. For the 29701 disabled output is "OFF", represented by a single center line. For the 29700, a disabled output is HIGH.

Figure 2.

Test Load

Open Collector 29700

S₁ is closed for all A.C. tests. Note that t_{PHZ}(CS) and t_{PHZ}(WE) parameters do not apply to 29700 where disabled output is HIGH.

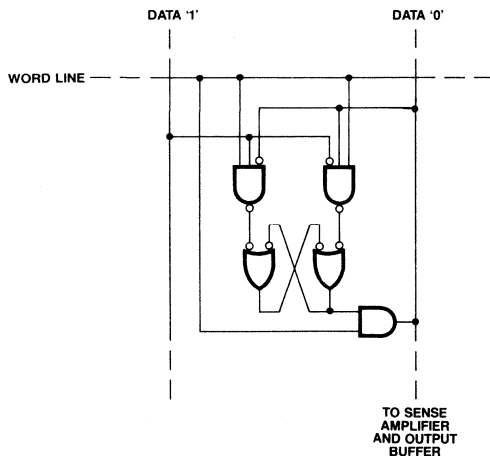


Three-State 29701

S₁ is closed for all A.C. tests except t_{PHZ}(CS) and t_{PHZ}(WE) where S₁ is open and jig capacitance (C_J) is ≤ 5pfd.

Figure 3.

Basic Memory Cell



Truth Table

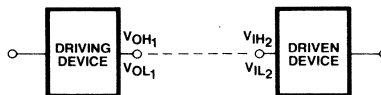
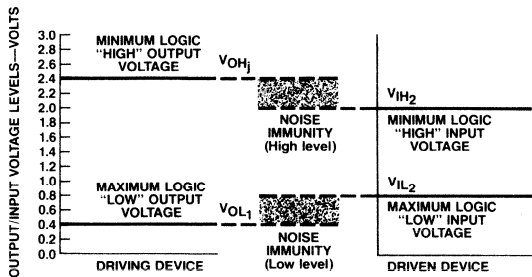
INPUTS			OUTPUTS	MODE
\overline{CS}	WE	D _i	O _i (t _n)	
H	L	L	Off	No Selection
H	L	H	Off	No Selection
H	H	X	Off	No Selection
L	L	L	Off	Write '0'
L	L	H	Off	Write '1'
L	H	X	D _i (t _{n-x})	Read

Note: The 29700 output is at a high impedance level at all times except when reading a LOW.

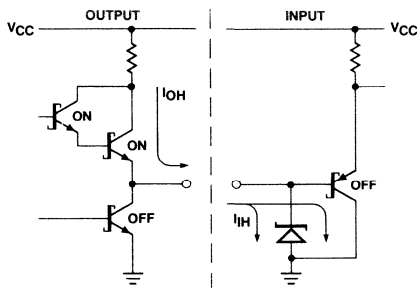
H = HIGH Voltage Level
 L = LOW Voltage Level
 OFF = HIGH Impedance

Input/Output Interface Conditions

Voltage Interface Conditions—LOW & HIGH

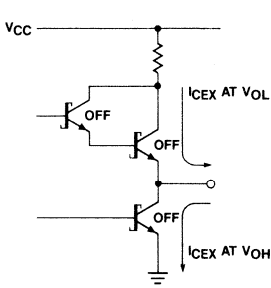


Current Conditions—HIGH State



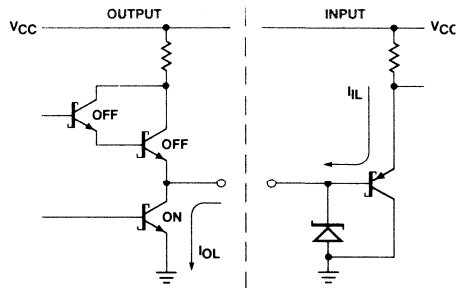
Note: 29700 open collector.

Current Conditions—OFF State



Note: 29700 open collector.

Current Conditions—LOW State



Loading Rules (In TTL Loads)

Notes

- The 29701 output has active circuitry for both logic levels and requires no external pull-up resistor.
- For a good DC noise margin with the 29700 a pull-up resistor can be used. Limits of R in kΩ are given by

$$\frac{V_{CC} - V_{OH \text{ required}}}{N I_{CEX} + N I_{IH}} > R_L > \frac{V_{CC} - V_{OL \text{ required}}}{I_{OL} - N I_{IL}}$$

Where n is number of OR tied outputs

N is the number of TTL units loads driven.

- Address and data lines can be interchanged within their respective groups for ease of P.C. layout without effecting device operation.
- Since for a given pattern on the address lines reading and writing are performed on the same actual memory word, the address lines can be driven by any mixture of assertion or negation of the variables making up the address field.

INPUT/OUTPUT	PIN NO.'S	INPUT LOADING	OUTPUT DRIVE (29701)	
			HIGH	LOW
A ₀	1	.25	—	—
CS	2	.25	—	—
WE	3	.25	—	—
D ₀	4	.25	—	—
O ₀	5	—	130	12.5
D ₁	6	.25	—	—
O ₁	7	—	130	12.5
GND	8	—	—	—
O ₂	9	—	130	12.5
D ₂	10	.25	—	—
O ₃	11	—	130	12.5
D ₃	12	.25	—	—
A ₃	13	.25	—	—
A ₂	14	.25	—	—
A ₁	15	.25	—	—
V _{CC}	16	—	—	—

A TTL unit load is -1.6mA at 0.4V and $40\mu\text{A}$ at 2.0V . The 29700 has open collector outputs; the output drive in the HIGH state is determined by an external pull-up resistor.

64-Bit Random Access Memory (Inverting)

29702, 29703

Features/Benefits

- Fully decoded 16-word x 4-bit Schottky technology high-speed RAM.
- Ultra fast access time typically 17ns.
- Non-Inverting outputs.
- Available with three-state outputs (29703) or with open collector outputs (29702).
- Pin compatible with AMD's Am29702,03 respectively.

Applications

- Scratch pad registers for accumulators and buffer memories
- Push down stacks

Functional Description

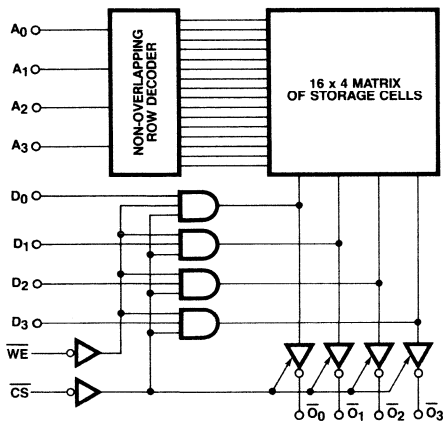
The 29702 and 29703 are 64-bit RAMs built using Schottky diode clamped transistors and are ideal for use in scratch pad and high-speed buffer memory applications. Each memory is organized as a fully decoded 16-word memory of 4 bits per word. Easy memory expansion is provided by an active LOW chip select (\overline{CS}) input and open collector OR tieable outputs (29702) or three-state outputs (29703). Chip selection for large memory systems can be controlled by active LOW output decoders.

An active LOW Write line \overline{WE} controls the writing/reading operation of the memory. When the chip select and write lines are LOW the information on the four data inputs D_0 to D_3 is written into the addressed memory word.

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the four inverting outputs \overline{O}_0 to \overline{O}_3 .

During the writing operation or when the chip select line is HIGH the four outputs of the memory go to an inactive high impedance state.

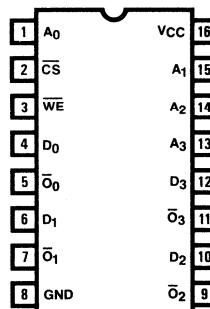
Block Diagram



Selection Guide

PART NUMBER	PACKAGE	OUTPUT	TEMPERATURE RANGE
29702NC	N16	OC	0°C to +75°C
29702JC	J16	OC	0°C to +75°C
29703NC	N16	TS	0°C to +75°C
29703JC	J16	TS	0°C to +75°C
29702JM	J16	OC	-55°C to +125°C
29702FM	F16	OC	-55°C to +125°C
29703JM	J16	TS	-55°C to +125°C
29703FM	F16	TS	-55°C to +125°C

Pin Configuration



Absolute Maximum Ratings

Supply voltage V_{CC}	Operating 7V
Input voltage	5.5V
Off-state output voltage	5.5V
Storage temperature range	-65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.75	5.00	5.25	V
I_{OH}	High level output current			-2.0			-5.2	mA
I_{OL}	Low level output current			16			20	mA
T_A	Operating free air temperature	-55		125	0		75	°C

Electrical Characteristics

Over Recommended Operating Free Air Temperature Range

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
V_{IC}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2	V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V},$ $V_{IL} = 0.8\text{V}$	$I_{OL} = 8 \text{ mA}$		0.45	V
			$I_{OL} = 10 \text{ mA}$		0.5	
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5\text{V}$			1.0	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4\text{V}$			10	μA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4\text{V}$			100	μA
C_I	Input Capacitance	$V_{CC} = 5.0\text{V}, f = 1 \text{ MHz}$ $T_A = 25^\circ\text{C}$	$V_I = 2.0\text{V}$		6	pF
C_O	Output Capacitance			$V_O = 2.0\text{V}$		8
I_{CC}	Supply current	$V_{CC} = \text{MAX}; \text{All inputs GND.}$			75 105	mA

OPEN COLLECTOR OUTPUT CURRENT

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CEX}	Output Leakage Current	$V_{CC} = \text{MAX}, V_O = 2.4\text{V}$			100	μA

THREE STATE OUTPUT ONLY

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V},$ $V_{IL} = 0.8\text{V}, I_{OH} = \text{MAX}$	2.4	3.6		V
I_{OZH}	Off-state output current high-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2\text{V},$ $V_O = 2.4\text{V}$			40	μA
I_{OZL}	Off-state output current low-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2\text{V},$ $V_O = 0.4\text{V}$			-40	μA
I_{OS}	Short-circuit output current	$V_{CC} = \text{MAX}$	-20	-45	-90	mA

Switching Characteristics Over Operating Range (Unless Otherwise Noted)

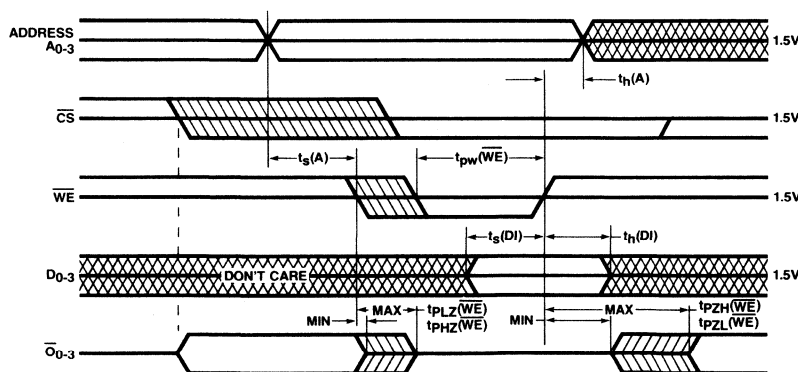
PARAMETERS	DESCRIPTION		A.C. TEST CONDITIONS	TYP	COM'L		MIL	UNITS
				(NOTE 1)	MIN	MAX	MIN	
t _{PLH} (A)	Delay from Address to Output	See Fig. 2	Fig. 3 test load (measured to output = 1.5V)	15	25	30	ns	
t _{PHL} (A)								
t _{PZH} (\overline{CS})	Delay from Chip Select (LOW) to Active Output and Correct Data	See Fig. 2		10	15	20	ns	
t _{PZL} (\overline{CS})								
t _{PZH} (\overline{WE})	Delay from Write Enable (HIGH) to Active Output and Correct Data (Write Recovery—See Note 2)	See Fig. 1		12	20	25	ns	
t _{PZL} (\overline{WE})								
t _s (A)	Set-up Time Address (Prior to Initiation of Write)	See Fig. 1		-6.0	0	0	ns	
t _h (A)	Hold Time Address (After Termination of Write)	See Fig. 1		-2.5	0	0	ns	
t _s (DI)	Set-up Time Data Input (Prior to Termination of Write)	See Fig. 1		9.0	20	25	ns	
t _h (DI)	Hold Time Data Input (After Termination of Write)	See Fig. 1		-4.0	0	0	ns	
t _{pw} (\overline{WE})	Min. Write Enable Pulse Width to Insure Write	See Fig. 1		10	20	25	ns	
t _{PHZ} (\overline{CS})	Delay from Chip Select (HIGH) to Inactive Output (HI-Z)	See Fig. 2		10	15	20	ns	
t _{PLZ} (\overline{CS})								
t _{PLZ} (\overline{WE})	Delay from Write Enable (LOW) to Inactive Output (HI-Z)	See Fig. 1	12	20	25	ns		
t _{PHZ} (\overline{WE})								

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.

2. Output is preconditioned to data in (non-inverted) during write to insure correct data is present on all outputs when write is terminated. (No write recovery glitch)



Switching Waveforms



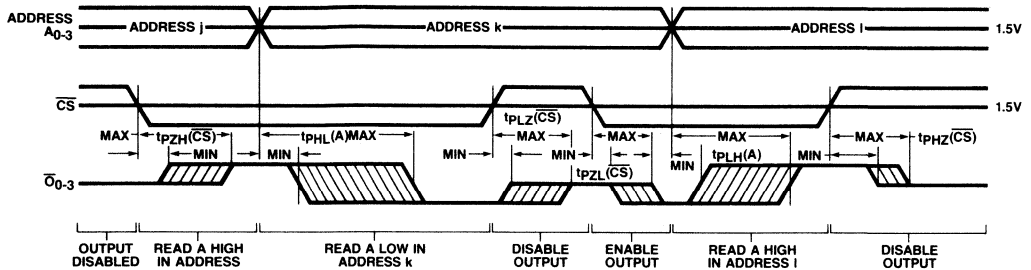
Key to Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
[Solid line]	MUST BE STEADY	WILL BE STEADY
[Diagonal lines /]	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
[Diagonal lines \]	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
[Cross-hatch]	DON'T CARE: ANY CHANGE PERMITTED	CHANGING. STATE UNKNOWN
[Diagonal lines X]	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF"-STATE

Write Cycle Timing. The cycle is initiated by an address change. After t_s(A) min., the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, t_h(A) min. must be allowed before the address may be changed again. The output will be inactive (floating for the 29703) while the write enable is LOW.

Figure 1.

Switching Waveforms (Cont.)



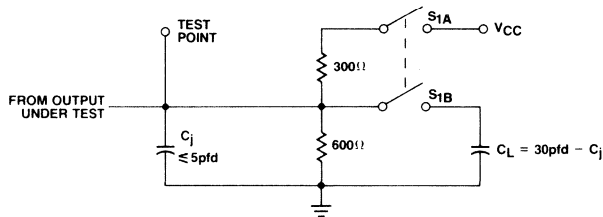
Switching delays from address and chip select inputs to the data output. For the 29703 disabled output is "OFF", represented by a single center line. For the 29702, a disabled output is HIGH.

Figure 2.

Open Collector 29702

S₁ is closed for all A.C. tests. Note that t_{PHZ}(CS) and t_{PHZ}(WE) parameters do not apply to 29702 where disabled output is HIGH.

Test Load

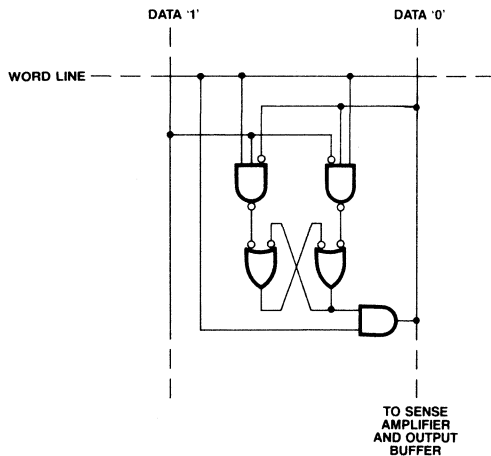


Three-State 29703

S₁ is closed for all A.C. tests except t_{PHZ}(CS) and t_{PHZ}(WE) where S₁ is open and jig capacitance (C_J) is ≤ 5pfd.

Figure 3.

Basic Memory Cell



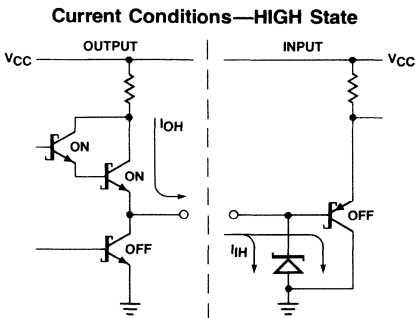
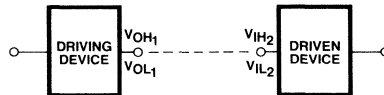
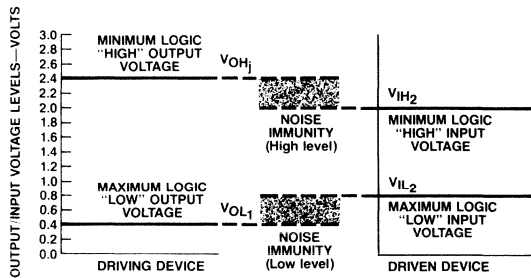
Truth Table

INPUTS			OUTPUTS	MODE
\overline{CS}	\overline{WE}	D _i	O _i (t _n)	
H	L	L	Off	No Selection
H	L	H	Off	No Selection
H	H	X	Off	No Selection
L	L	L	Off	Write '0'
L	L	H	Off	Write '1'
L	H	X	D _i (t _{n-x})	Read

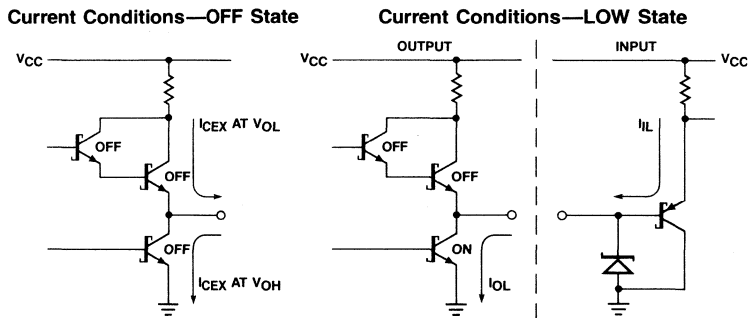
Note: The 29702 output is at a high impedance level at all times except when reading a LOW.

H = HIGH Voltage Level
 L = LOW Voltage Level
 OFF = HIGH Impedance

Input/Output Interface Conditions Voltage Interface Conditions—LOW & HIGH



Note: 29702 open collector.



Note: 29702 open collector.



Loading Rules (In TTL Loads)

INPUT/OUTPUT	PIN NO.'S	INPUT LOADING	OUTPUT DRIVE (29703)	
			HIGH	LOW
A ₀	1	.25	—	—
\overline{CS}	2	.25	—	—
\overline{WE}	3	.25	—	—
D ₀	4	.25	—	—
$\overline{O_0}$	5	—	130	12.5
D ₁	6	.25	—	—
$\overline{O_1}$	7	—	130	12.5
GND	8	—	—	—
$\overline{O_2}$	9	—	130	12.5
D ₂	10	.25	—	—
$\overline{O_3}$	11	—	130	12.5
D ₃	12	.25	—	—
A ₃	13	.25	—	—
A ₂	14	.25	—	—
A ₁	15	.25	—	—
V _{CC}	16	—	—	—

A TTL unit load is -1.6mA at 0.4V and $40\mu\text{A}$ at 2.0V . The 29702 has open collector outputs; the output drive in the HIGH state is determined by an external pull-up resistor.

Notes
1. The 29703 output has active circuitry for both logic levels and requires no external pull-up resistor.

2. For a good DC noise margin with the 29702 a pull-up resistor can be used. Limits of R in k Ω are given by

$$\frac{V_{CC} - V_{OH \text{ required}}}{nI_{CEX} + nI_{IH}} > R_L > \frac{V_{CC} - V_{OL \text{ required}}}{I_{OL} - nI_{IL}}$$

Where n is number of OR tied outputs
N is the number of TTL units loads driven.

3. Address and data lines can be interchanged within their respective groups for ease of P.C. layout without effecting device operation.

4. Since for a given pattern on the address lines reading and writing are performed on the same actual memory word, the address lines can be driven by any mixture of assertion or negation of the variables making up the address field.

Schottky 64-Bit Random Access Memory

27S02A, 27S03A

Features/Benefits

- Fully decoded 16-word x 4-bit Low power Schottky RAMS
- Ultra high speed: Address access time typically 15ns
- Low Power: I_{CC} typically 75mA
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Output preconditioned during write to eliminate write recovery glitch
- Available with three-state outputs (27S03A) or with open collector outputs (27S02A)
- Pin compatible replacements for 3101, 3101A, 74S289, 93403, 7489 and Am27S02A and for 74S189, DM8599 and Am27S03A

Applications

- Scratch pad registers for accumulators and buffer memories
- Push down stacks

Description

The 27S02A and 27S03A are 64-bit RAMs built using Schottky diode clamped transistors in conjunction with internal ECL circuitry and are ideal for use in scratch pad and high speed buffer

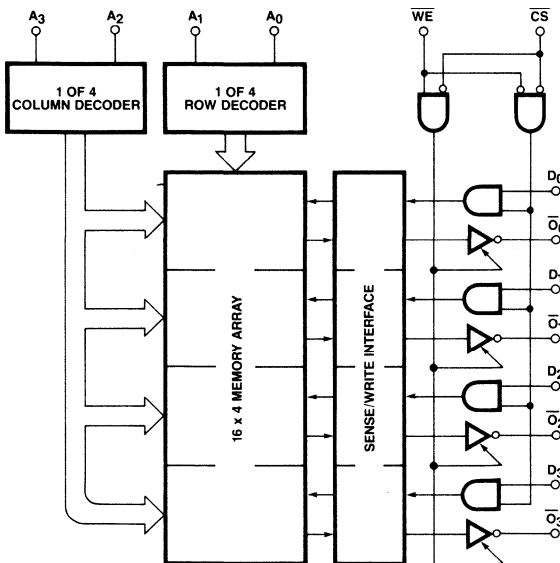
memory applications. Each memory is organized as a fully decoded 16-word memory of 4-bits per word. Easy memory expansion is provided by an active LOW chip select (\overline{CS}) input and open collector OR tieable outputs (27S02A) or three-state outputs (27S03A). Chip selection for large memory systems can be controlled by active LOW output decoders such as a 74S138.

An active LOW Write line (\overline{WE}) controls the writing/reading operation of the memory. When the chip select and write lines are LOW the information on the four data inputs D_0 to D_3 is written into the addressed memory word and preconditions the output circuitry so that true data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch".

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the four inverting outputs \overline{O}_0 to \overline{O}_3 .

During the writing operation or when the chip select line is HIGH the four outputs of the memory go to an inactive high impedance state.

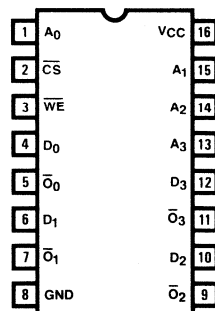
Block Diagram



Selection Guide

PART NUMBER	PACKAGE	OUTPUT	TEMPERATURE RANGE
27S02ANC	N16	OC	0°C to +75°C
27S02AJC	J16	OC	0°C to +75°C
27S03ANC	N16	TS	0°C to +75°C
27S03AJC	J16	TS	0°C to +75°C
27S02AJM	J16	OC	-55°C to +125°C
27S02AFM	F16	OC	-55°C to +125°C
27S03AJM	J16	TS	-55°C to +125°C
27S03AFM	F16	TS	-55°C to +125°C

Pin Configuration



Absolute Maximum Ratings

Supply voltage V_{CC}	Operating 7V
Input voltage	5.5V
Off-state output voltage	5.5V
Storage temperature range	-65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.75	5.00	5.25	V
I_{OH}	High level output current			-2.0			-5.2	mA
I_{OL}	Low level output current			8			10	mA
T_A	Operating free air temperature	-55		125	0		75	°C

Electrical Characteristics

Over Recommended Operating Free Air Temperature Range

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
V_{IC}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2	V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V}, V_{IL} = 0.8\text{V}$			0.45	V
					0.5	
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5\text{V}$			1.0	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4\text{V}$			10	μA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4\text{V}$			100	μA
C_i	Input Capacitance	$V_{CC} = 5.0\text{V}, f = 1 \text{ MHz}$		6		pF
C_o	Output Capacitance	$T_A = 25^\circ\text{C}$		8		pF
I_{CC}	Supply current	$V_{CC} = \text{MAX}; \text{All inputs GND.}$		75	105	mA

OPEN COLLECTOR OUTPUT CURRENT

I_{CEX}	Output Leakage Current	$V_{CC} = \text{MAX}, V_O = 2.4\text{V}$			100	μA
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THREE STATE OUTPUT ONLY

V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V}, V_{IL} = 0.8\text{V}, I_{OH} = \text{MAX}$	2.4	3.6		V
I_{OZH}	Off-state output current high-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2\text{V}, V_O = 2.4\text{V}$			40	μA
I_{OZL}	Off-state output current low-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2\text{V}, V_O = 0.4\text{V}$			-40	μA
I_{OS}	Short-circuit output current	$V_{CC} = \text{MAX}$	-20	-45	-90	mA

Switching Characteristics Over Operating Range (Unless Otherwise Noted)

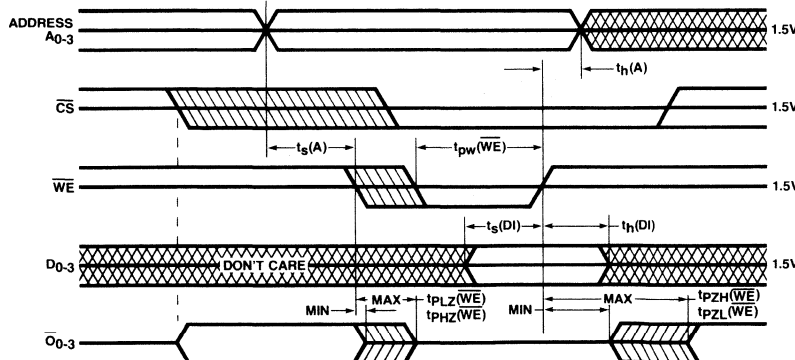
PARAMETERS	DESCRIPTION		A.C. TEST CONDITIONS	TYP (NOTE 1)	COM'L		MIL		UNITS
					MIN	MAX	MIN	MAX	
t _{PLH} (A)	Delay from Address to Output	See Fig. 2	Fig. 3 test load (measured to output = 1.5V)	15	25	30	ns		
t _{PHL} (A)									
t _{PZH} (CS)	Delay from Chip Select (LOW) to Active Output and Correct Data	See Fig. 2		10	15	20	ns		
t _{PZL} (CS)									
t _{PZH} (WE)	Delay from Write Enable (HIGH) to Active Output and Correct Data (Write Recovery—See Note 2)	See Fig. 1		12	20	25	ns		
t _{PZL} (WE)									
t _s (A)	Set-up Time Address (Prior to Initiation of Write)	See Fig. 1		-6.0	0	0	ns		
t _h (A)	Hold Time Address (After Termination of Write)	See Fig. 1		-2.5	0	0	ns		
t _s (DI)	Set-up Time Data Input (Prior to Termination of Write)	See Fig. 1		9.0	20	25	ns		
t _h (DI)	Hold Time Data Input (After Termination of Write)	See Fig. 1		-4.0	0	0	ns		
t _{pw} (WE)	Min. Write Enable Pulse Width to Insure Write	See Fig. 1	10	20	25	ns			
t _{PHZ} (CS)	Delay from Chip Select (HIGH) to Inactive Output (HI-Z)	See Fig. 2	10	15	20	ns			
t _{PLZ} (CS)									
t _{PLZ} (WE)	Delay from Write Enable (LOW) to Inactive Output (HI-Z)	See Fig. 1	12	20	25	ns			
t _{PHZ} (WE)									

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.

2. Output is preconditioned to data in (non-inverted) during write to insure correct data is present on all outputs when write is terminated. (No write recovery glitch)

5

Switching Waveforms



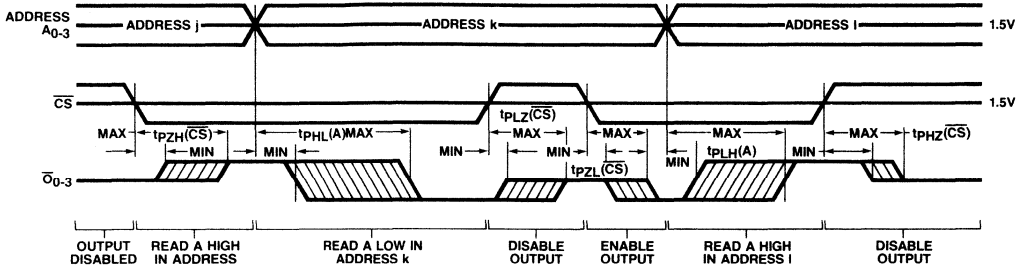
Key to Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
[Solid line]	MUST BE STEADY	WILL BE STEADY
[Diagonal lines /]	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
[Diagonal lines \]	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
[Cross-hatch]	DON'T CARE: ANY CHANGE PERMITTED	CHANGING. STATE UNKNOWN
[X-hatch]	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF"-STATE

Write Cycle Timing. The cycle is initiated by an address change. After t_s(A) min., the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, t_h(A) min. must be allowed before the address may be changed again. The output will be inactive (floating for the 27S03A) while the write enable is LOW.

Figure 1.

Switching Waveforms (Cont.)



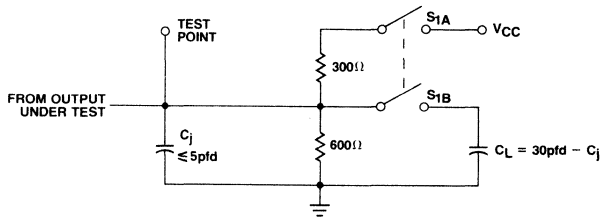
Switching delays from address and chip select inputs to the data output. For the 27S03A disabled output is "OFF", represented by a single center line. For the 27S02A, a disabled output is HIGH.

Figure 2.

Open Collector
27S02A

S₁ is closed for all A.C. tests. Note that t_{PHZ}(CS) and t_{PHZ}(WE) parameters do not apply to 27S02A where disabled output is HIGH.

Test Load

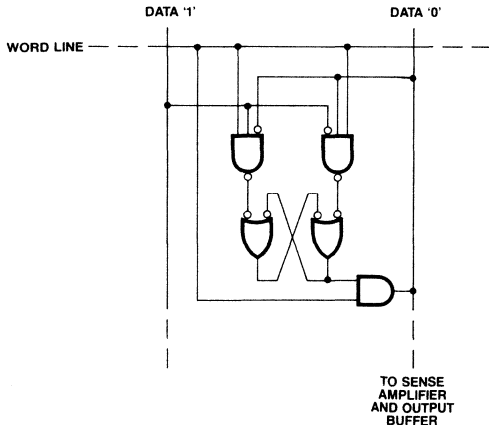


Three-State
27S03A

S₁ is closed for all A.C. tests except t_{PHZ}(CS) and t_{PHZ}(WE) where S₁ is open and jig capacitance (C_J) is ≤ 5pfd.

Figure 3.

Basic Memory Cell



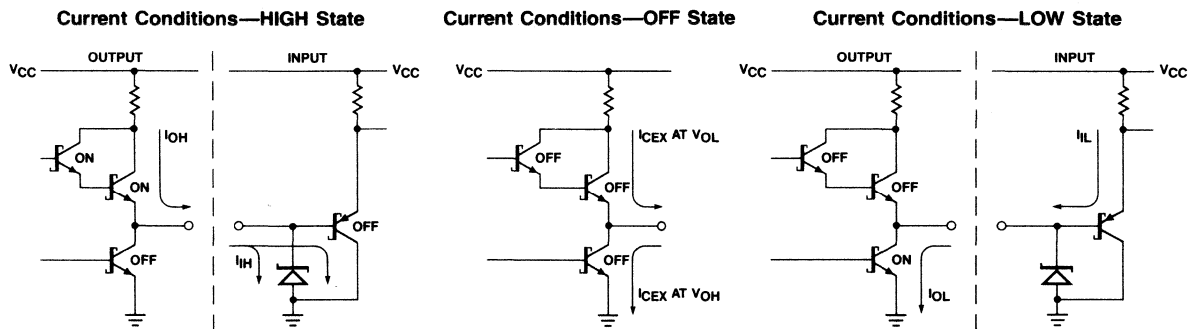
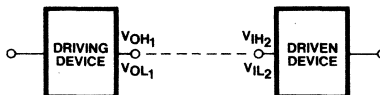
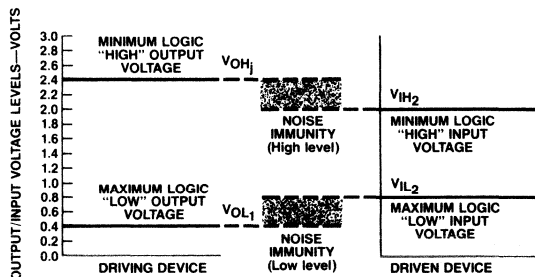
Truth Table

INPUTS			OUTPUTS	MODE
CS	WE	D _i	O _i (t _η)	
H	L	L	Off	No Selection
H	L	H	Off	No Selection
H	H	X	Off	No Selection
L	L	L	Off	Write '0'
L	L	H	Off	Write '1'
L	H	X	D _i (t _{η-x})	Read

Note: The 27S02A output is at a high impedance level at all times except when reading a LOW.

H = HIGH Voltage Level
L = LOW Voltage Level
OFF = HIGH Impedance

Input/Output Interface Conditions
Voltage Interface Conditions—LOW & HIGH



Note: 27LS02 open collector.

Note: 27S02A open collector.

5

Loading Rules (In TTL Loads)

INPUT/OUTPUT	PIN NO.'S	INPUT LOADING	OUTPUT DRIVE (27S03A)	
			HIGH	LOW
A ₀	1	.25	—	—
\overline{CS}	2	.25	—	—
\overline{WE}	3	.25	—	—
D ₀	4	.25	—	—
\overline{O}_0	5	—	130	12.5
D ₁	6	.25	—	—
\overline{O}_1	7	—	130	12.5
GND	8	—	—	—
\overline{O}_2	9	—	130	12.5
D ₂	10	.25	—	—
\overline{O}_3	11	—	130	12.5
D ₃	12	.25	—	—
A ₃	13	.25	—	—
A ₂	14	.25	—	—
A ₁	15	.25	—	—
VCC	16	—	—	—

Notes

1. The 27S03A output has active circuitry for both logic levels and requires no external pull-up resistor.

2. For a good DC noise margin with the 27S02A a pull-up resistor can be used. Limits of R in kΩ are given by

$$\frac{V_{CC} - V_{OH \text{ required}}}{N I_{CEX} + N I_{IH}} > R_L > \frac{V_{CC} - V_{OL \text{ required}}}{I_{OL} - N I_{IL}}$$

Where n is number of OR tied outputs

N is the number of TTL units loads driven.

3. Address and data lines can be interchanged within their respective groups for ease of P.C. layout without effecting device operation.

4. Since for a given pattern on the address lines reading and writing are performed on the same actual memory word, the address lines can be driven by any mixture of assertion or negation of the variables making up the address field.

A TTL unit load is -1.6mA at 0.4V and $40\mu\text{A}$ at 2.0V . The 27S02A has open collector outputs; the output drive in the HIGH state is determined by an external pull-up resistor.

Low Power Schottky 64-Bit Random Access Memory

27LS02, 27LS03

Features/Benefits

- Fully decoded 16-word x 4-bit Low power Schottky RAMS
- Ultra low power: I_{CC} typically 25mA
- High speed: Address access time typically 30ns
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Output preconditioned during write to eliminate the write recovery glitch
- Available with three-state outputs (27LS03) or with open collector outputs (27LS02)
- Pin compatible replacements for DM74L89A, DM74LS289, 7489 and AM27LS02, for DM86L99, DM74LS189, and Am27LS03.

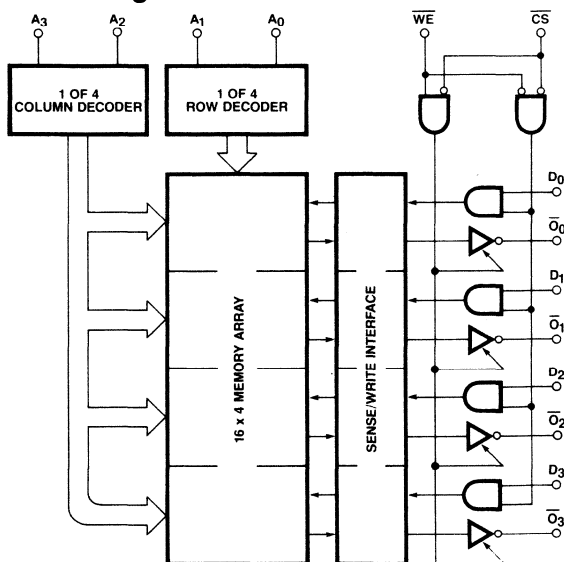
Applications

- Scratch pad registers for accumulators and buffer memories
- Push down stacks

Description

The 27LS02 and 27LS03 are 64-bit RAMs built using Schottky diode clamped transistors in conjunction with internal ECL circuitry and are ideal for use in scratch pad and high speed buffer

Block Diagram



memory applications where power is at a premium. Each memory is organized as a fully decoded 16-word memory of 4-bits per word. Easy memory expansion is provided by an active LOW chip select (\overline{CS}) input and open collector OR tieable outputs (27LS02) or three-state outputs (27LS03). Chip selection for large memory systems can be controlled by active LOW output decoders such as a 74LS138.

An active LOW Write line (\overline{WE}) controls the writing/reading operation of the memory. When the chip select and write lines are LOW, the information on the four data inputs D_0 to D_3 is written into the addressed memory word and preconditions the output circuitry so that true data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch".

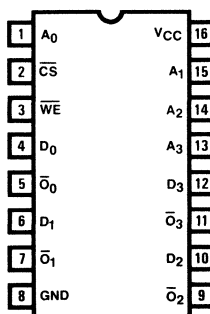
Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is readout on the four inverting outputs \overline{O}_0 to \overline{O}_3 .

During the writing operation or when the chip select line is HIGH the four outputs of the memory go to an inactive high impedance state.

Selection Guide

PART NUMBER	PACKAGE	OUTPUT	TEMPERATURE RANGE
27LS02ANC	N16	OC	0°C to +75°C
27LS02AJC	J16	OC	0°C to +75°C
27LS03ANC	N16	TS	0°C to +75°C
27LS03AJC	J16	TS	0°C to +75°C
27LS02AJM	J16	OC	-55°C to +125°C
27LS02AFM	F16	OC	-55°C to +125°C
27LS03AJM	J16	TS	-55°C to +125°C
27LS03AFM	F16	TS	-55°C to +125°C

Pin Configuration



Absolute Maximum Ratings

Supply voltage V_{CC}	Operating 7V
Input voltage	5.5V
Off-state output voltage	5.5V
Storage temperature range	-65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.75	5.00	5.25	V
I_{OH}	High level output current			-2.0			-5.2	mA
I_{OL}	Low level output current			8			10	mA
T_A	Operating free air temperature	-55		125	0		75	°C

Electrical Characteristics**Over Recommended Operating Free Air Temperature Range**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
V_{IC}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2	V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V},$ $V_{IL} = 0.8\text{V}$	$I_{OL} = 8 \text{ mA}$		0.45	V
			$I_{OL} = 10 \text{ mA}$		0.5	
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5\text{V}$			1.0	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4\text{V}$			10	μA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4\text{V}$			100	μA
C_I	Input Capacitance	$V_{CC} = 5.0\text{V}, f = 1 \text{ MHz}$		$V_I = 2.0\text{V}$	6	pF
C_O	Output Capacitance	$T_A = 25^\circ\text{C}$		$V_O = 2.0\text{V}$	8	pF
I_{CC}	Supply current	$V_{CC} = \text{MAX}; \text{All inputs GND.}$		25	38	mA

OPEN COLLECTOR OUTPUT CURRENT

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CEX}	Output Leakage Current	$V_{CC} = \text{MAX}, V_O = 2.4\text{V}$			100	μA

THREE STATE OUTPUT ONLY

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V},$ $V_{IL} = 0.8\text{V}, I_{OH} = \text{MAX}$	2.4	3.6		V
I_{OZH}	Off-state output current high-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2\text{V},$ $V_O = 2.4\text{V}$			40	μA
I_{OZL}	Off-state output current low-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2\text{V},$ $V_O = 0.4\text{V}$			-40	μA
I_{OS}	Short-circuit output current	$V_{CC} = \text{MAX}$	-20	-45	-90	mA

Switching Characteristics Over Operating Range (Unless Otherwise Noted)

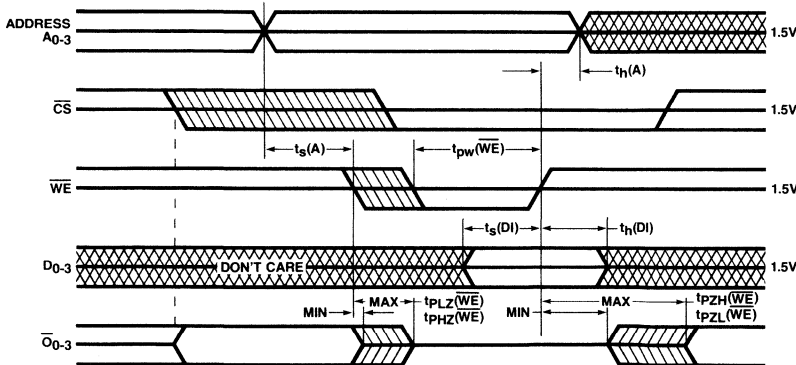
PARAMETERS	DESCRIPTION		A.C. TEST CONDITIONS	TYP (NOTE 1)	COM'L		UNITS
					MIN	MAX	
t _{PLH} (A)	Delay from Address to Output	See Fig. 2	Fig. 3 test load (measured to output = 1.5V)	30	55	65	ns
t _{PHL} (A)							
t _{PZH} (\overline{CS})	Delay from Chip Select (LOW) to Active Output and Correct Data	See Fig. 2		18	30	35	ns
t _{PZL} (\overline{CS})							
t _{PZH} (\overline{WE})	Delay from Write Enable (HIGH) to Active Output and Correct Data (Write Recovery—See Note 2)	See Fig. 1		18	30	35	ns
t _{PZL} (\overline{WE})							
t _s (A)	Set-up Time Address (Prior to Initiation of Write)	See Fig. 1		-17	0	0	ns
t _h (A)	Hold Time Address (After Termination of Write)	See Fig. 1		-6	0	0	ns
t _s (DI)	Set-up Time Data Input (Prior to Termination of Write)	See Fig. 1		16	45	55	ns
t _h (DI)	Hold Time Data Input (After Termination of Write)	See Fig. 1		-40	0	0	ns
t _{pw} (\overline{WE})	Min. Write Enable Pulse Width to Insure Write	See Fig. 1		20	45	55	ns
t _{PHZ} (\overline{CS})	Delay from Chip Select (HIGH) to Inactive Output (HI-Z)	See Fig. 2		18	30	35	ns
t _{PLZ} (\overline{CS})							
t _{PLZ} (\overline{WE})	Delay from Write Enable (LOW) to Inactive Output (HI-Z)	See Fig. 1	18	30	35	ns	
t _{PHZ} (\overline{WE})							

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.

2. Output is preconditioned to data in (non-inverted) during write to insure correct data is present on all outputs when write is terminated. (No write recovery glitch)

5

Switching Waveforms



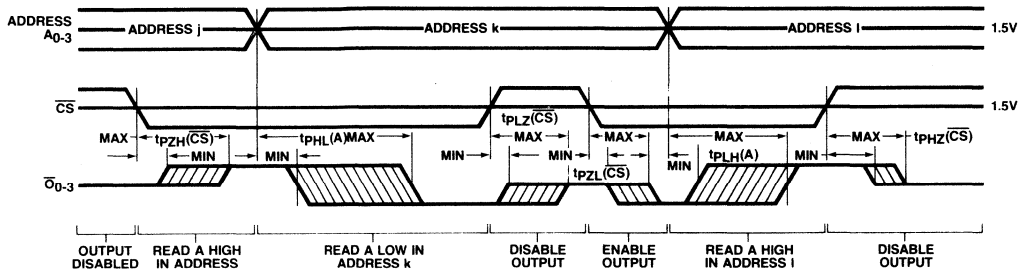
Key to Timing Diagram

WAVEFORM INPUTS	OUTPUTS	
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING. STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF"-STATE

Write Cycle Timing. The cycle is initiated by an address change. After t_s(A) min., the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, t_h(A) min. must be allowed before the address may be changed again. The output will be inactive (floating for the 27LS03) while the write enable is LOW.

Figure 1.

Switching Waveforms (Cont.)



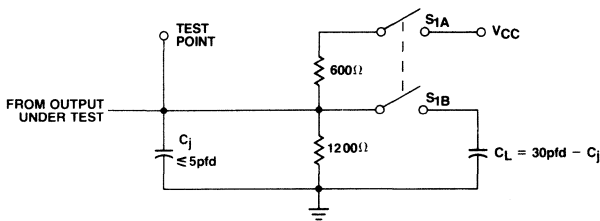
Switching delays from address and chip select inputs to the data output. For the 27LS03 disabled output is "OFF", represented by a single center line. For the 27LS02, a disabled output is HIGH.

Figure 2.

Open Collector 27LS02

S₁ is closed for all A.C. tests. Note that t_{PHZ}(CS) and t_{PHZ}(WE) parameters do not apply to 27LS02 where disabled output is HIGH.

Test Load

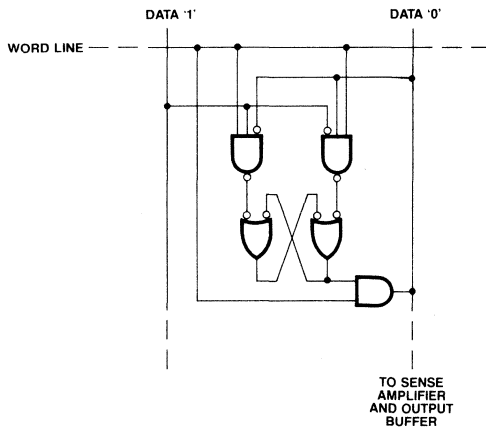


Three-State 27LS03

S₁ is closed for all A.C. tests except t_{PHZ}(CS) and t_{PHZ}(WE) where S₁ is open and jig capacitance (C_J) is ≤ 5pfd.

Figure 3.

Basic Memory Cell



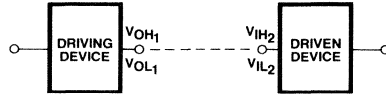
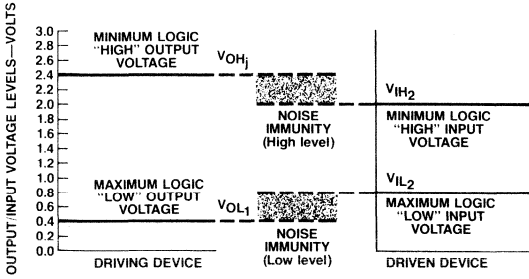
Truth Table

INPUTS			OUTPUTS	MODE
\overline{CS}	\overline{WE}	D _i	O _i (t _n)	
H	L	L	Off	No Selection
H	L	H	Off	No Selection
H	H	X	Off	No Selection
L	L	L	Off	Write '0'
L	L	H	Off	Write '1'
L	H	X	D _i (t _{n-x})	Read

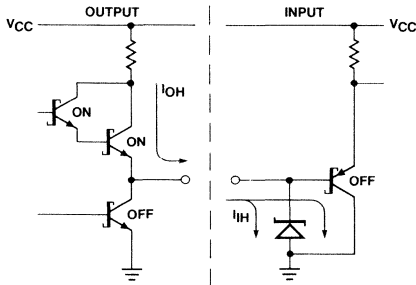
Note: The 27LS02 output is at a high impedance level at all times except when reading a LOW.

H = HIGH Voltage Level
 L = LOW Voltage Level
 OFF = HIGH Impedance

Input/Output Interface Conditions Voltage Interface Conditions—LOW & HIGH

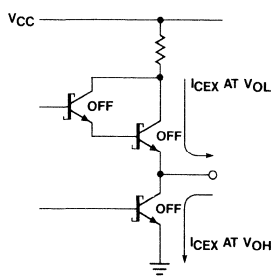


Current Conditions—HIGH State



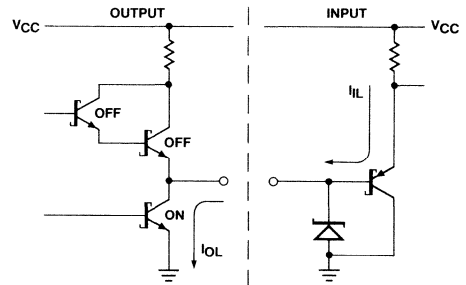
Note: 27LS02 open collector.

Current Conditions—OFF State



Note: 27LS02 open collector.

Current Conditions—LOW State



Loading Rules (In TTL Loads)

INPUT/OUTPUT	PIN NO.'S	INPUT LOADING	OUTPUT DRIVE (27LS03)	
			HIGH	LOW
A ₀	1	.25	—	—
\overline{CS}	2	.25	—	—
\overline{WE}	3	.25	—	—
D ₀	4	.25	—	—
O ₀	5	—	130	6.25
D ₁	6	.25	—	—
O ₁	7	—	130	6.25
GND	8	—	—	—
O ₂	9	—	130	6.25
D ₂	10	.25	—	—
O ₃	11	—	130	6.25
D ₃	12	.25	—	—
A ₃	13	.25	—	—
A ₂	14	.25	—	—
A ₁	15	.25	—	—
VCC	16	—	—	—

Notes

- The 27LS03 output has active circuitry for both logic levels and requires no external pull-up resistor.
- For a good DC noise margin with the 27LS02 a pull-up resistor can be used. Limits of R in kΩ are given by

$$\frac{V_{CC} - V_{OH} \text{ required}}{N I_{CEX} + N I_{IH}} > R_L > \frac{V_{CC} - V_{OL} \text{ required}}{I_{OL} - N I_{IL}}$$
 Where n is number of OR tied outputs
 N is the number of TTL units loads driven.
- Address and data lines can be interchanged within their respective groups for ease of P.C. layout without effecting device operation.
- Since for a given pattern on the address lines reading and writing are performed on the same actual memory word, the address lines can be driven by any mixture of assertion or negation of the variables making up the address field.

A TTL unit load is -1.6mA at 0.4V and $40\mu\text{A}$ at 2.0V. The 27LS02 has open collector outputs; the output drive in the HIGH state is determined by an external pull-up resistor.

256-Bit Bipolar (256x1) Random Access Memory

5530/6530, 5531/6531

Features/Benefits

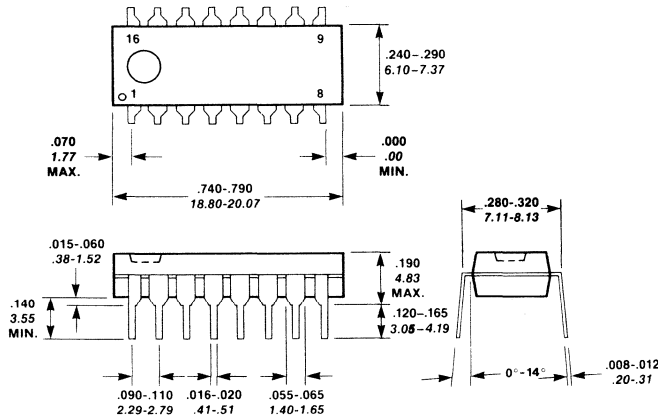
- 55 ns maximum access time over 0°C to 75°C and ±5% voltage variation (6530/6531).
- 70 ns maximum access time over -55°C to 125°C and ±10% voltage variation (5530/5531).
- Advanced Schottky processing.
- Low input current (250 μA maximum).
- The data stored is on the data out pin during a write cycle.
- Fully decoded with 3 chip enables.

Applications

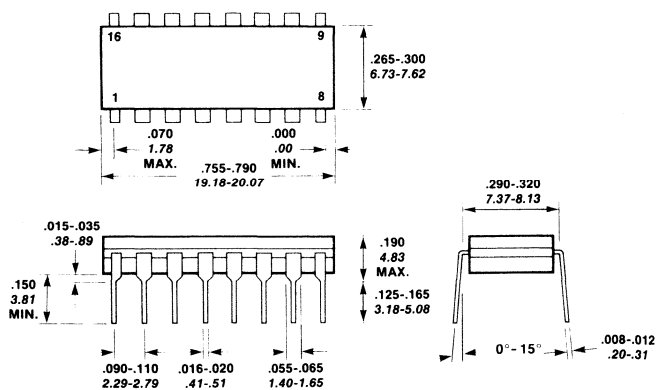
- Buffer memory.
- Cache memory.
- Writable control store.
- High speed main memory.
- Large scratch pad.

Package Drawings

N16 Plastic DIP



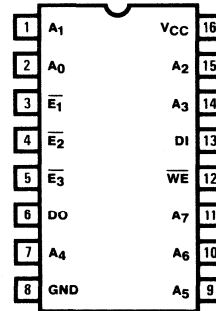
J16 Ceramic DIP



Selection Guide

Part Number	Package	Output	Temperature Range
6530	N16	OC	0° to +75°C
6531	N16	TS	0° to +75°C
5530	J16, F16	OC	-55°C to +125°C
5531	J16, F16	TS	-55°C to +125°C

Pin Configuration



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES.
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.

5

Absolute Maximum Ratings

Supply voltage V_{CC}	Operating -0.5V to 7V
Input voltage	-1.5V to 5.5V
Off-state output voltage	-1.5V to 5.5V
Storage temperature range	-65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.75	5.00	5.25	V
I_{OH}	High-level output current			-3.2			-3.2	mA
I_{OL}	Low-level output current			10			15	mA
T_A	Operating free air temperature	-55		125	0		75	°C

Electrical Characteristics

Over Recommended Operating Free Air Temperature Range

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	$V_{CC} = 5.0V$	2			V
V_{IL}	Low-level input voltage	$V_{CC} = 5.0V$			0.8	V
V_{IC}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -5.0 \text{ mA}$			-1.0	V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2V,$ $V_{IL} = 0.8V, I_{OL} = \text{MAX}$			0.5	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5V$			1.0	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4V$			40	μA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.45V$			-250	μA
C_I	Input capacitance	$V_{CC} = 5.0V, f = 1\text{MHz}$		7.0		pF
C_O	Output capacitance	$T_A = 25^\circ C$		8.0		
I_{CC}	Supply current	$V_{CC} = 5.0V,$ All inputs		6530, 31 5530, 31	95 130 95 135	mA

OPEN COLLECTOR OUTPUT CURRENT

I_{CEX}	Output Leakage Current	$V_{CC} = \text{MAX}, V_O = 2.4V$		100	μA
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THREE STATE OUTPUT ONLY

V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2V,$ $V_{IL} = 0.8V, I_{OH} = \text{MAX}$	2.4		V
I_{OZH}	Off-state output current high-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2V,$ $V_O = 2.4V$		100	μA
I_{OZL}	Off-state output current low-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2V,$ $V_O = 0.4V$		-100	μA
I_{OS}	Short-circuit output current	$V_{CC} = 5.0, V_O = 0V$	-20	-90	mA

Switching Characteristics
With Standard Load (Figure 1)

SYMBOL	PARAMETER	FIGURE	5530/5531 5.0V ±10%, -55 to 125°C		6530/6531 5.0V ±5%, 0 to 75°C		UNIT
			MIN	MAX	MIN	MAX	
T _A A	Address access time	2	20	70	20	55	ns
T _E A	Enable access time	2	5.0	45	5.0	35	ns
T _E R	Enable recovery time	2	5.0	35	5.0	35	ns
T _W P	Write pulse width *	3	70		50		ns
T _D W	Time input data appears at the output following a write command T _D W ₀ ≥ MIN	3		120		90	ns
T _D W ₀	Data in and write enable overlap time	3	65		45		ns
T _W SA	Address to write enable setup time	3	0		0		ns
T _W HA	Address to write enable hold time	3	0		0		ns
T _W SCS	Chip enable to write enable set-up time	3	10		10		ns
T _W HCH	Chip enable to write enable hold time	3	0		0		ns

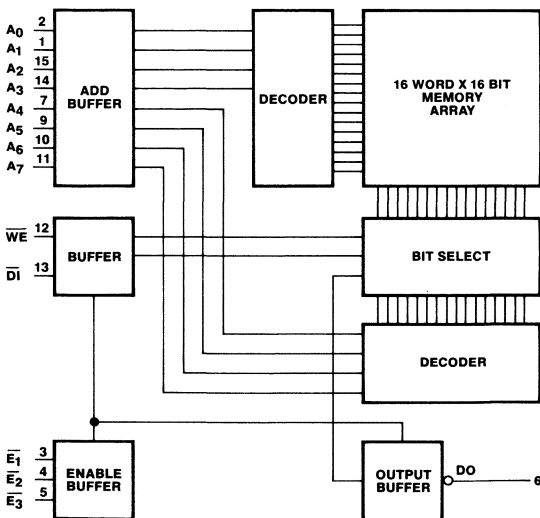
5531/6531 ONLY

T _{ON}	Chip enable to low impedance delay		0		0		ns
T _{OFF}	Chip enable to high impedance delay			25		25	ns

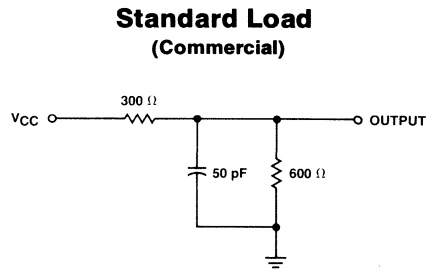
* Write recovery time is less than T_WA

5

Block Diagram



Standard Test Circuit



Input Pulse Amplitude = 3.0V
Input Rise and Fall Time
5.0 ns From 1.0V to 2.0V
Measurements Made at 1.50V

Figure 1.

Waveforms

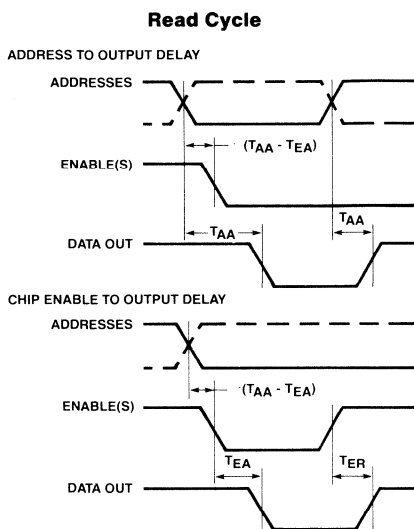


Figure 2.

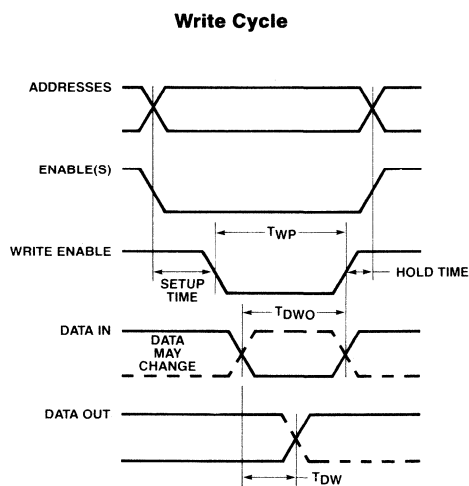


Figure 3.

Functional Table

CHIP SELECT	WRITE ENABLE	OPERATION	OUTPUT
ALL LOW	LOW	WRITE	COMPLEMENT OF DATA INPUT
ALL LOW	HIGH	READ	COMPLEMENT OF WRITTEN DATA
ONE OR MORE HIGH	DON'T CARE	HOLD	5531/6531 HIGH IMPEDANCE STATE 5530/6530 HIGH

Memory Operation

READ: The memory is addressed with the A_0 — A_7 inputs which selects one of the 256 words. The chip is enabled by making all chip enables low. If any chip enables are high the chip is disabled. If the write enable is HIGH and the chip is enabled the stored data is read out on the data out pin. The data read out is the COMPLEMENT of the data written in during the write cycle.

WRITE: The memory is addressed with the A_0 — A_7 inputs which selects one of the 256 words. The chip is enabled as in the read cycle. If the write enable is LOW the data on the data input pin is written into the addressed word. The data out of the memory during the write cycle is the complement of the data written in. This allows checking of the stored data during the write cycle.

Some memory devices may write in as fast as 10 ns so address and write enable timing must be carefully controlled, when the memory is operated with the enables activated throughout the cycle.

Memory Expansion Rules

1. TO EXPAND THE NUMBER OF BITS IN THE WORD:
Tie corresponding address pins together, tie write enable pins together, and bring data in and data out independently.
2. TO EXPAND THE NUMBER OF WORDS:
Tie corresponding address pins together, tie write enable pins and corresponding data in and data out pins together, and use the higher order system addresses in conjunction with the chip enable to pick one row of packages.

Low Power 256-BIT Bipolar (256 x 1) Random Access Memory L5530/L6530, L5531/L6531

Features/Benefits

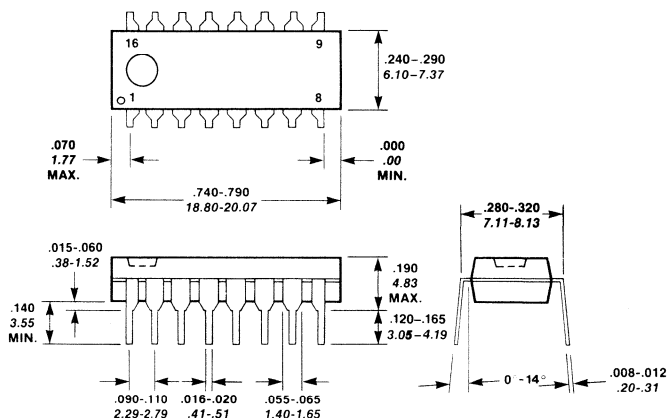
- Typical power dissipation of 275 mW.
- 115 ns maximum access time over 0°C to 75°C and ±5% voltage variation (L6530/L6531).
- 130 ns maximum access time over -55°C to 125°C and ±10% voltage variation (L5530/L5531).
- Advanced Schottky processing.
- Low input current (125 μA maximum).
- The data stored is on the data out pin during a write cycle.
- Fully decoded with 3 chip enables.

Selection Guide

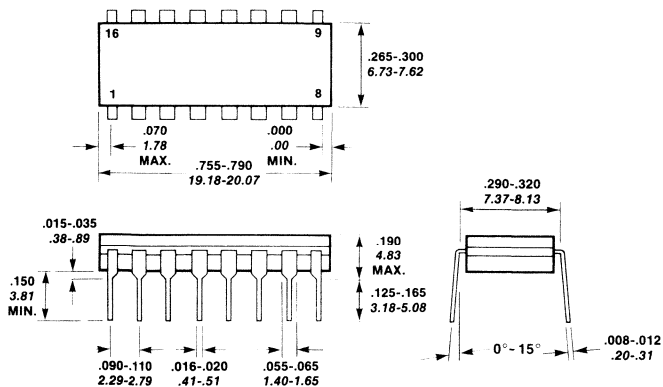
Part Number	Package	Output	Temperature Range
L6530	N16	OC	0° to +75°C
L6531	N16	TS	0° to +75°C
L5530	J16, F16	OC	-55°C to +125°C
L5531	J16, F16	TS	-55°C to +125°C

Package Drawings

N16 Plastic DIP



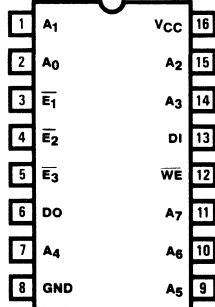
J16 Ceramic DIP



Applications

- Buffer memory.
- Cache memory.
- Writable control store.
- High speed main memory.
- Large scratch pad.

Pin Configuration



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES.
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.

5

Absolute Maximum Ratings

Supply voltage V_{CC}	Operating -0.5V to 7V
Input voltage	-1.5V to 5.5V
Off-state output voltage	-1.5V to 5.5V
Storage temperature range	-65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.75	5.00	5.25	V
I_{OH}	High-level output current			-3.2			-3.2	mA
I_{OL}	Low-level output current			10			15	mA
T_A	Operating free air temperature	-55		125	0		75	°C

Electrical Characteristics**Over Recommended Operating Free Air Temperature Range**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	$V_{CC} = 5.0V$	2			V
V_{IL}	Low-level input voltage	$V_{CC} = 5.0V$			0.8	V
V_{IC}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -5.0 \text{ mA}$			-1.0	V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2V,$ $V_{IL} = 0.8V, I_{OL} = \text{MAX}$			0.5	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5V$			1.0	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4V$			40	μA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.45V$			-250	μA
C_I	Input capacitance	$V_{CC} = 5.0V, f = 1 \text{ MHz}$		7.0		pF
C_O	Output capacitance	$T_A = 25^\circ C$		8.0		
I_{CC}	Supply current	$V_{CC} = \text{MAX}, \text{All inputs at}$ $2.4V, \text{all Outputs, open}$		55	85	mA
		L6530/31 L5530/31		55	100	

OPEN COLLECTOR OUTPUT CURRENT

I_{CEX}	Output Leakage Current	$V_{CC} = \text{MAX}, V_O = 2.4V$			100	μA
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THREE STATE OUTPUT ONLY

V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2V,$ $V_{IL} = 0.8V, I_{OH} = \text{MAX}$	2.4			V
I_{OZH}	Off-state output current high-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2V,$ $V_O = 2.4V$			100	μA
I_{OZL}	Off-state output current low-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2V,$ $V_O = 0.5V$			-100	μA
I_{OS}	Short-circuit output current	$V_{CC} = 5.0, V_O = 0V$	-20		-90	mA

Switching Characteristics
With Standard Load (Figure 1)

SYMBOL	PARAMETER	FIGURE	L5530/L5531		L6530/L6531		UNIT
			5.0V ±10%, -55 to 125°C MIN	MAX	5.0V ±5%, 0 to 75°C MIN	MAX	
TAA	Address access time	2	20	130	20	115	ns
TEA	Enable access time	2	5.0	80	5.0	60	ns
TER	Enable recovery time	2	5.0	85	5.0	60	ns
TWP	Write pulse width*	3	100		85		ns
TD AND TDW	Time input data appears at the output following a write command $T_{DWO} \geq MIN$	3		130		110	ns
T _{DWO}	Data in and write enable overlap time	3	100		85		ns
T _{WSA}	Address to write enable setup time	3	0		0		ns
T _{WHA}	Address to write enable hold time	3	0		0		ns
T _{WSCS}	Chip enable to write enable set-up time	3	10		10		ns
T _{WHCH}	Chip enable to write enable hold time	3	0		0		ns

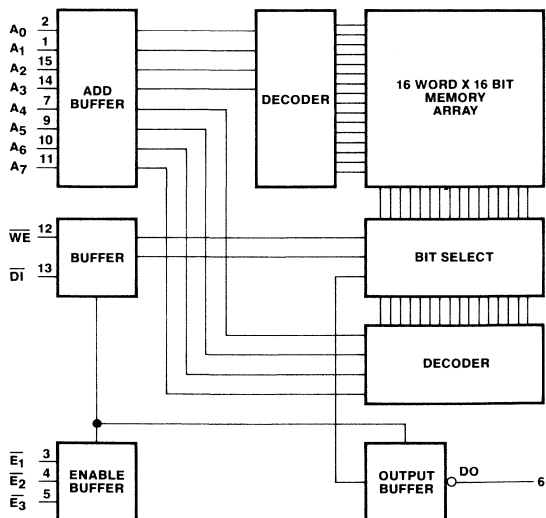
L5531/L6531 ONLY

T _{ON}	Chip enable to low impedance delay		0		0		ns
T _{OFF}	Chip enable to high impedance delay			80		55	ns

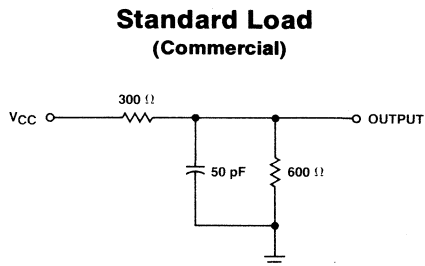
* Write recovery time is less than TWA

5

Block Diagram



Standard Test Circuit



Input Pulse Amplitude = 3.0V
Input Rise and Fall Time
5.0 ns From 1.0V to 2.0V
Measurements Made at 1.50V

Figure 1

Waveforms

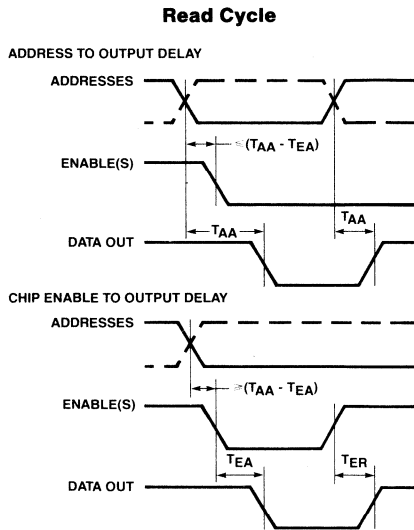


Figure 2

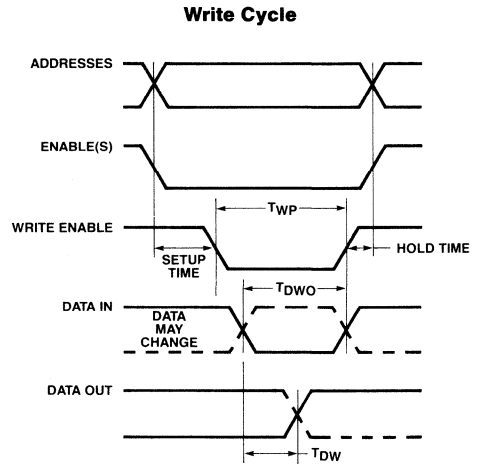


Figure 3

Functional Table

CHIP SELECT	WRITE ENABLE	OPERATION	OUTPUT	
ALL LOW	LOW	WRITE	COMPLEMENT OF DATA INPUT	
ALL LOW	HIGH	READ	COMPLEMENT OF WRITTEN DATA	
ONE OR MORE HIGH	DON'T CARE	HOLD	L5531/L6531	HIGH IMPEDANCE STATE
			L5530/L6530	OFF

Memory Operation

READ: The memory is addressed with the A_0 — A_7 inputs which selects one of the 256 words. The chip is enabled by making all chip enables low. If any chip enables are high the chip is disabled. If the write enable is HIGH and the chip is enabled the stored data is read out on the data out pin. The data read out is the COMPLEMENT of the data written in during the write cycle.

WRITE: The memory is addressed with the A_0 — A_7 inputs which selects one of the 256 words. The chip is enabled as in the read cycle. If the write enable is LOW the data on the data input pin is written into the addressed word. The data out of the memory during the write cycle is the complement of the data written in. This allows checking of the stored data during the write cycle. **Some memory devices may write in as fast as 10 ns** so address and write enable timing must be carefully controlled, when the memory is operated with the enables activated throughout the cycle.

Memory Expansion Rules

- TO EXPAND THE NUMBER OF BITS IN THE WORD:**
Tie corresponding address pins together, tie write enable pins together, and bring data in and data out independently.
- TO EXPAND THE NUMBER OF WORDS:**
Tie corresponding address pins together, tie write enable pins and corresponding data in and data out pins together, and use the higher order system addresses in conjunction with the chip enable to pick one row of packages.

First-In First-Out (FIFO) 64x4 Serial Memory

57401/67401

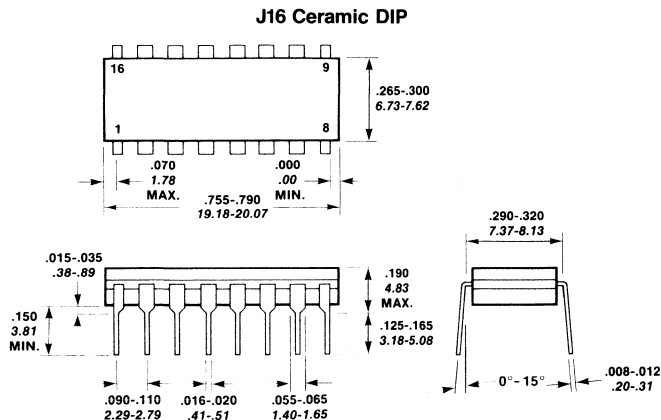
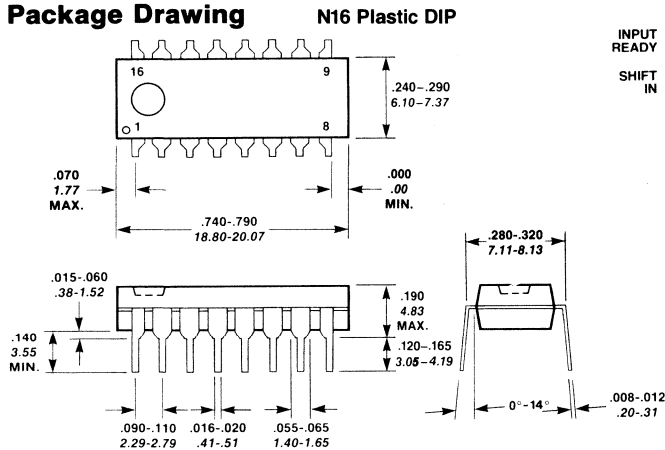
Features/Benefits

- 12 MHz shift in, shift out typical rates
- Advanced Schottky bipolar processing
- TTL inputs and outputs
- Readily expandable in word and bit dimensions
- Asynchronous or synchronous operation
- Pin compatible with Fairchild's F3341 MOS FIFO and ten times as fast

Description

The 57401 is an expandable "fall-through" high speed First-In First-Out (FIFO) memory organized 64 words by 4-bit. A 12 MHz data rate allows usage in high speed tape or disc controllers and communication buffer applications. The 67401 is specified over the commercial operating range 0 -75°C and the 57401 is specified over the military operating of -55°C to +125°C.

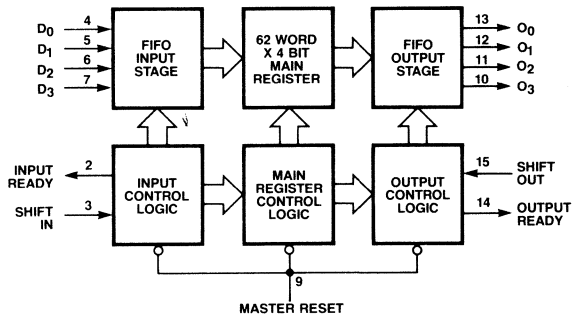
Package Drawing



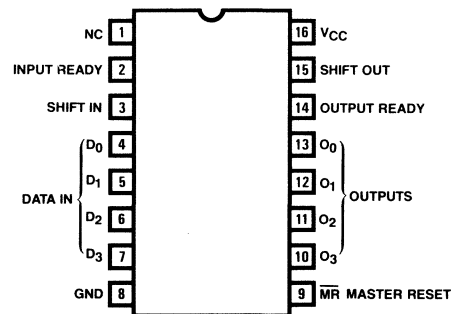
Selection Guide

PART NUMBER	PACKAGE	TEMPERATURE RANGE
57401	J16	Military
67401	J/N16	Commercial

Block Diagram



Pin Configuration



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES.
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.

Absolute Maximum Ratings

Supply voltage V_{CC}	Operating 7V/12V
Input voltage	5.5V/12V
Off-state output voltage	5.5V/12V
Storage temperature range	-65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.75	5.00	5.25	V
I_{OH}	High-level output current			0.9			0.9	mA
I_{OL}	Low-level output current			8			8	mA
T_A	Operating free air temperature	-55		125	0		75	°C

Electrical Characteristics

Over Recommended Operating Free Air Temperature

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IC}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18\text{mA}$			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V}$ $V_{IL} = 0.8\text{V}, I_{OH} = \text{MAX}$	2.4			V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V}$ $V_{IL} = 0.8\text{V}, I_{OL} = \text{MAX}$			0.5	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5\text{V}$			1	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4\text{V}$			50	μA
I_{IL1}	Low-level input current inputs $D_0 - D_3, MR$	$V_{CC} = \text{MAX}, V_F = 0.45\text{V}$			-0.8	mA
I_{IL2}	Low-level input current inputs S_1, S_0	$V_{CC} = \text{MAX}, V_F = 0.45\text{V}$			-1.6	mA
I_{OS}	Short-circuit output current	$V_{CC} = 6\text{V}, V_O = .5\text{V}$	-20		-90	mA
C_I	Input capacitance	$V_{CC} = 5.0\text{V}$		7		pF
C_O	Output capacitance	$f = 1\text{MHz}, T_A = 25^\circ\text{C}$		8		
I_{CC}	Supply current	$V_{CC} = \text{MAX}^1$		111	150	mA

NOTE: 1. I_{CC} measured with worst case sequence; FIFO reset, one shift-in cycle with data inputs held low, measure I_{CC} with all inputs held low.

Switching Characteristics

See Figure 1

SYMBOL	PARAMETER	FIGURE	57401—MILITARY 5 ± 10%, -55°C to +125°C			67401—COMMERCIAL 5 ± 5%, 0°C to 70°C		
			MIN	MAX	UNIT	MIN	MAX	UNIT
t _{IN}	Shift in Clock Rate	1	7		MHz	10		MHz
t _{SIH}	Shift in High Time	1	45		ns	35		ns
t _{SIL}	Shift in Low Time	1	45		ns	35		ns
t _{IRL}	Input Ready ON Delay	1		60	ns		45	ns
t _{IRH}	Input Ready OFF Delay	1		60	ns		45	ns
t _{IDS}	Input Data Set Up	1	10		ns	5		ns
t _{IDH}	Input Data Hold Time	1	55		ns	45		ns
f _{OUT}	Shift Out Clock Rate	2	7		MHz	10		MHz
t _{SOH}	Shift Out High Time	2	45		ns	35		ns
t _{SOL}	Shift Out Low Time	2	45		ns	35		ns
t _{ORL}	Output Ready ON Delay	2		65	ns		55	ns
t _{ORH}	Output Ready OFF Delay	2		65	ns		55	ns
t _{ODH}	Output Data Hold Time	2	10		ns	10		ns
t _{ODS}	Output Data Delay	2		65	ns		55	ns
t _{PT}	Data Throughput Time	Note 1		4.0	μs		3.0	μs
t _{MRW}	Master Reset Pulse	Note 2	30		ns	25		ns
t _{MRORL}	Master Reset to OR Low	5		65	ns		55	ns
t _{MRIRH}	Master Reset to IR High	5		45	ns		35	ns
t _{MRS}	Master Reset to SI	5	45		ns	35		ns
t _{IPH}	Input Ready Pulse High	4	45		ns	35		ns
t _{IPL}	Input Ready Pulse Low	6	45		ns	35		ns
t _{OPH}	Output Ready Pulse High	3	45		ns	35		ns
t _{OPL}	Output Ready Pulse Low	7	45		ns	35		ns

NOTES: 1. This parameter defines total time from the time data is present at D₀-D₃ to the time it is available at O₀-O₃ with FIFO initially empty and total time from the time data is extracted from O₀-O₃ to IR High with FIFO initially full.
2. Master Reset clears the 57401/67401 to the all cells empty state.

Functional Description

Data Input

Data is entered into the FIFO on D₀-D₃ inputs. To enter data the Input Ready (IR) output should be HIGH, indicating that the first location is ready to accept data. Data then present at the four data inputs is entered into the first location when the Shift In (SI) is brought HIGH. A SI HIGH signal causes the RI to go LOW. Data remains at the first location until SI is brought LOW. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. If the memory is full, IR will remain LOW.

Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the

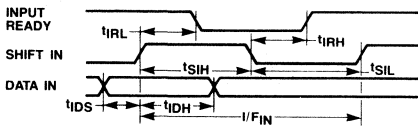
end of the device while empty locations will "bubble" to the front. t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device.

Data Output

Data is read from the O₀-O₃ outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the memory is emptied, OR stays LOW.

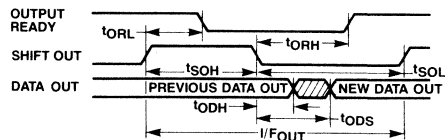
Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

Timing Diagrams



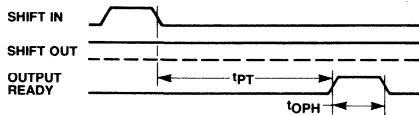
1. Input data must remain stable during t_{IDS} and t_{IDH} .
2. Input Ready HIGH indicates that space is available and a Shift In pulse may be applied. Input Ready LOW indicates that the FIFO is full or that a previous Shift In operation is not complete. Shift In pulses applied while Input Ready is LOW will be ignored.
3. The rise of Input Ready indicates that the data at the D0-D3 inputs has been accepted and that the input stage is empty.

Figure 1. FIFO Input Timing



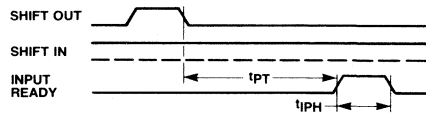
1. Output data will be stable at the rise of Output Ready.
2. Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied. Output Ready LOW indicates that the FIFO is empty or that a previous Shift Out operation is still in progress. Shift Out pulses applied while Shift Out Ready is LOW will be ignored.
3. The rise of Output Ready indicates that new data has been loaded into the output stage.

Figure 2. FIFO Output Timing



1. FIFO initially empty.
2. Shift Out held high (as shown).

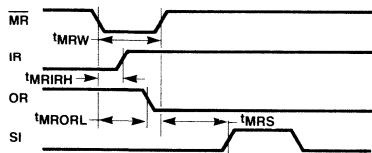
Figure 3. t_{OPH} Specification



1. FIFO initially full.
2. Shift In held high (as shown).

Figure 4. t_{IPH} Specification

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1. FIFO initially full

Figure 5. FIFO Master Reset Timing

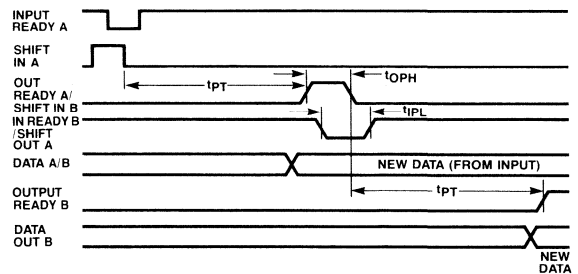
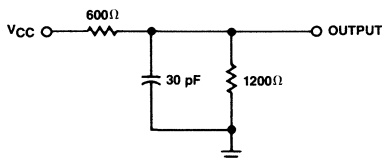


Figure 6. FIFO/FIFO Communication: Empty/Input Timing

Standard Test Circuit



Input Pulse Amplitude = 3.0V
 Input Rise and Fall Time = 5.0 ns from 1.0V to 2.0V
 Measurements made at 1.50V

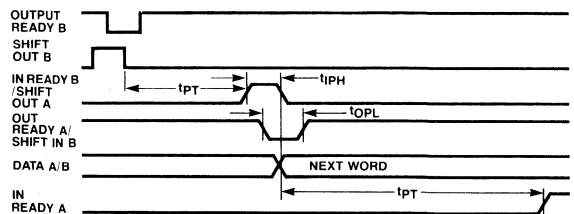


Figure 7. FIFO/FIFO Communication: Full/Output Timing

Expansion

FIFOs can be connected serially to form larger effective FIFOs: i.e., two 64 x 4 FIFOs can be connected to form a 128 x 4 FIFO, as shown in Figure 8. This is done by connecting the data outputs of the input side FIFO, A, to the data inputs of the output side FIFO, B, and Output Ready and Shift Out Pins of the input FIFO, A, to the Shift In and Input Ready pins of the output FIFO, B, respectively.

If both FIFOs are empty, the Input Ready/Shift Out pins between the FIFOs will be HIGH and the Output Ready/Shift In pins between the FIFOs will be LOW. If the Shift In pin of FIFO A is clocked, the data will propagate to the output. This will set the output full indicator, causing the Output Ready/Shift In combination to rise temporarily. However, since the Input Ready/Shift Out combination is HIGH this enables the Shift Out clock and the full indicator is reset immediately after the rise of Output Ready/Shift In. The result in a positive going pulse on the Output Ready/Shift In line which is t_{OPH} , Output Pulse High (empty), as shown in Figure 6. The FIFO chip is designed such that the pulse is greater than the minimum Shift In High time, t_{SIH} . The leading edge (LOW to HIGH) of this Output Ready pulse indicates that the new word is available at FIFO A's output. This LOW to HIGH transition on FIFO B's Shift In causes FIFO B to load the data from FIFO A into B's first (input) word. FIFO B responds by taking the Input Ready/Shift Out combination LOW. The trailing edge, HIGH to LOW transition of Output Ready/Shift In Pulse allows the word in FIFO B to propagate on to its output. Once propagation has begun, FIFO B will again raise Input Pulse Low (empty). The FIFO is designed such that this pulse is greater than the minimum Shift Out Low time, t_{SOL} .

Chip-to-chip communication for the case of two connected FIFOs, both full, with an empty location bubbling from the output to the input is similar to the both-empty case described above. When both FIFO A and B are full, Input Ready/Shift Out is LOW and Output Ready/Shift In is HIGH. When an empty location bubbles from the output of FIFO B to its input, Input Ready/Shift will temporarily go HIGH. Since Output Ready/Shift In is

already HIGH, the Shift In clock is enabled and Input Ready/Shift Out will immediately go LOW. The result is a pulse on the Input Ready/Shift Out line which is t_{IPH} , Input Pulse High (full). The FIFO is designed such that this pulse is greater than the minimum Shift Out High time, t_{SOH} . The leading edge of this pulse will cause FIFO A to load new data at its outputs, and the trailing edge will cause the newly created empty location to bubble through FIFO A. The rise of the Input Ready/Shift Out pulse will cause Output Ready/Shift In to go LOW. Output Ready/Shift In will go HIGH again when new data has been loaded into FIFO A's output. This creates a negative pulse on the Output Ready/Shift In line which is t_{OPL} , Output Pulse Low (full). The FIFO is designed such that t_{OPL} is greater than the minimum Shift Out Low time.

Word Length Expansion

Expansion of the FIFO to a longer word length is accomplished as shown in Figures 9 and 10. Careful attention must be paid to the generation of composite Input Ready and Output Ready signals. Because of device-to-device variation the Shift In (SI) to Input Ready (IR) delays will be different on the input FIFOs. If a simple scheme such as shown in Figure 9 is used, then this variation must be allowed for, since composite Input Ready will go LOW as soon as the fastest IR goes LOW, but Shift In cannot go LOW until all three IRs for the input FIFOs are LOW. The user must provide sufficient delay to insure this.

Figure 9 shows one way to eliminate any potential timing problems. The gates and flip-flops are used to generate a Shift In or Shift Out pulse independent of the Shift In or Shift Out signal. The gating insures that Shift In does not go HIGH until all IRs are HIGH and does not go LOW until they are all LOW. The output gating operates in the same way. The only restriction on Shift In and Shift Out are that they must be long enough to clock the flip-flop and that they must occur after the composite Input Ready or Output Ready signal.

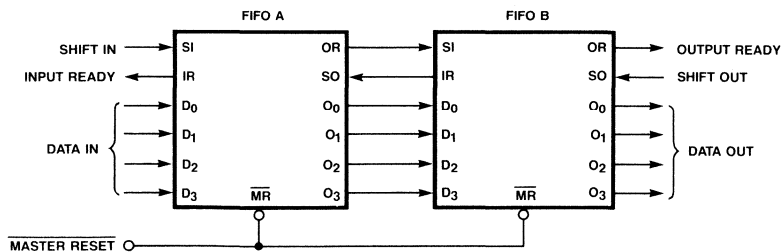


Figure 8. 128 x 4 FIFO

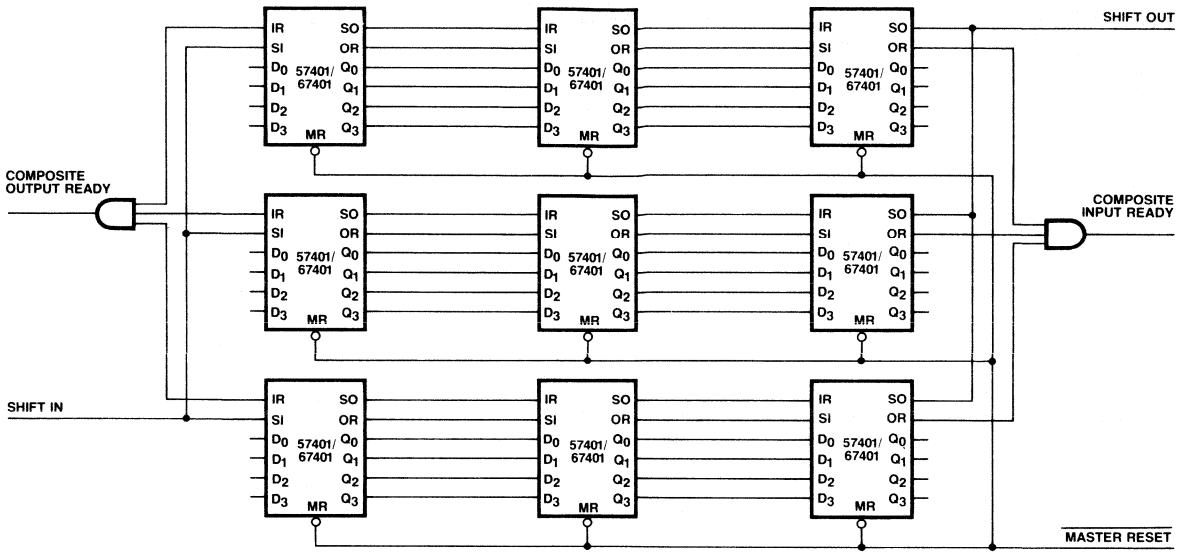


Figure 9. 192 x 12 FIFO—Unlatched Control Lines

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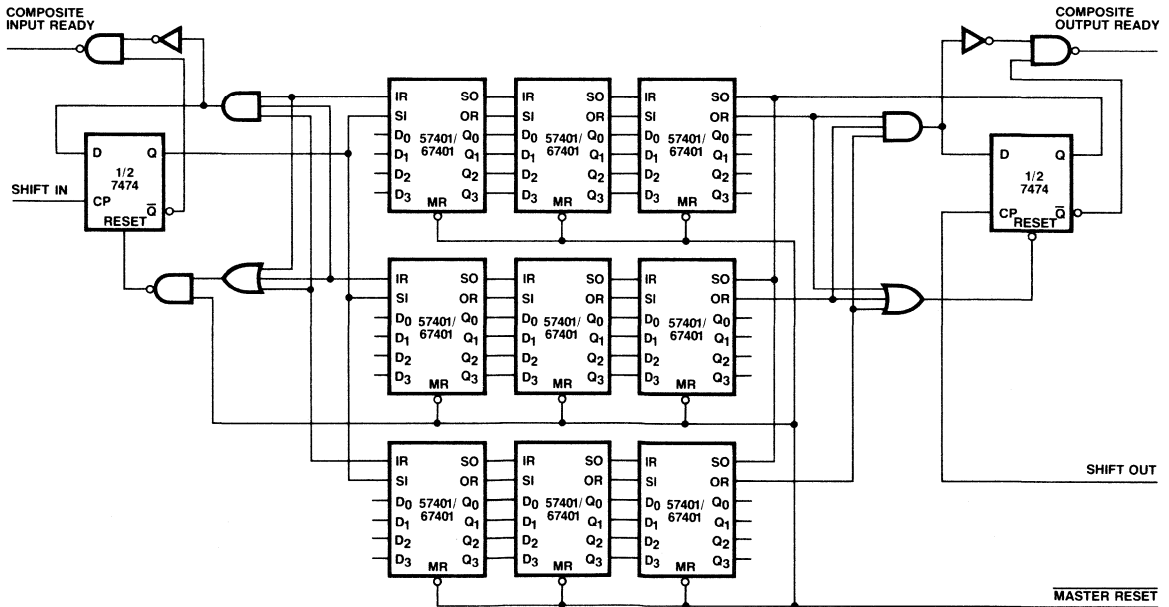


Figure 10. 192 x 12 FIFO—Latched Control Lines

PRELIMINARY
NOTE: THIS DATA
SPECIFICATIONS ARE SUBJECT TO CHANGE
WITHOUT NOTICE

First-In First-Out (FIFOs) 64x4, 64x5 Serial Memories 57401A/67401A, 57402A/67402A

Features/Benefits

- 15 MHz shift in, shift out typical rates
- Advanced Schottky bipolar processing
- TTL inputs and outputs
- Readily expandable in word and bit dimensions
- Asynchronous or synchronous operation
- 64x4 FIFO pin compatible with Fairchild's F3341 MOS FIFO and ten times as fast
- 4 & 5-bit organizations for 9 bit expansion
- Master reset clears outputs to zero state

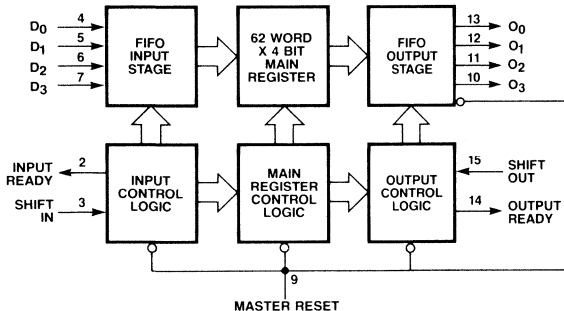
Description

The 57401A/402A are expandable "fall-through" high speed First-In First-Out (FIFO) memories. The 57401A is organized 64 words by 4-bits. The 57402A is organized 64 words by 5-bits. A 15 MHz data rate allows usage in high speed tape or disc controllers and communication buffer applications. The 67401A/67402A is specified over the commercial operating range 0–75°C and the 57401A/57402A is specified over the military operating range of –55°C to +125°C.

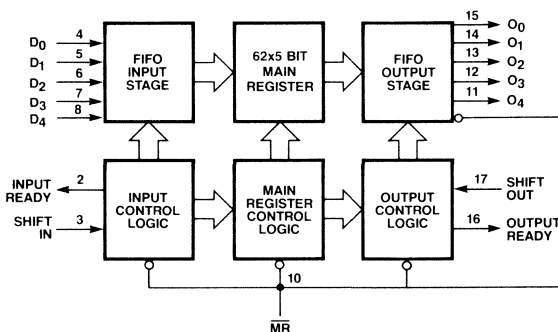
Selection Guide

PART NUMBER	PACKAGE	TEMPERATURE RANGE
57401A	J16	Military
67401A	J/N16	Commercial
57402A	J18	Military
67402A	J/N18	Commercial

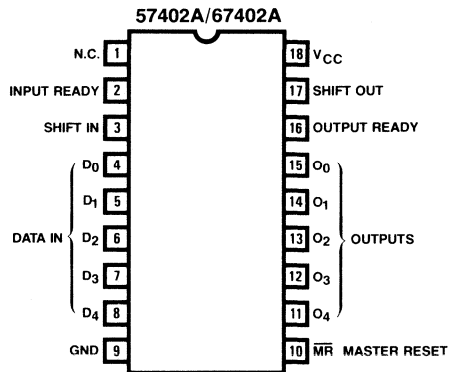
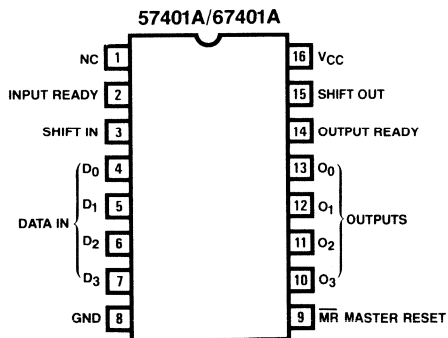
Block Diagram 57401A/67401A 64x4



Block Diagram 57402A/67402A 64x5



Pin Configuration



Absolute Maximum Ratings

Supply voltage V_{CC}	Operating 7V
Input voltage	5.5V
Off-state output voltage	5.5V
Storage temperature range	-65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.75	5.00	5.25	V
I_{OH}	High-level output current			0.9			0.9	mA
I_{OL}	Low-level output current			8			8	mA
T_A	Operating free air temperature	-55		125	0		75	°C

Electrical Characteristics

Over Recommended Operating Free Air Temperature

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IC}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18\text{mA}$			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V}$ $V_{IL} = 0.8\text{V}, I_{OH} = \text{MAX}$	2.4			V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V}$ $V_{IL} = 0.8\text{V}, I_{OL} = \text{MAX}$			0.5	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5\text{V}$			1	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4\text{V}$			50	μA
I_{IL1}	Low-level input current inputs $D_0 - D_3, MR$	$V_{CC} = \text{MAX}, V_F = 0.45\text{V}$			-0.8	mA
I_{IL2}	Low-level input current inputs $S1, S0$	$V_{CC} = \text{MAX}, V_F = 0.45\text{V}$			-1.6	mA
I_{OS}	Short-circuit output current	$V_{CC} = \text{MAX}, V_O = .5\text{V}$	-20		-90	mA
C_I	Input capacitance	$V_{CC} = 5.0\text{V}$		7		pF
C_O	Output capacitance	$f = 1\text{MHz}, T_A = 25^\circ\text{C}$		8		
I_{CC}	Supply current 57401A/67401A	$V_{CC} = \text{MAX}^1$		111	150	mA
I_{CC}	Supply current 57402A/67402A	$V_{CC} = \text{MAX}^1$		119	160	mA

NOTE: 1. I_{CC} measured with worst case sequence; FIFO reset, one shift-in cycle with data inputs held low, measure I_{CC} with all inputs held low.

5

Switching Characteristics

See Figure 1

SYMBOL	PARAMETER	FIGURE	57401A/57402A—MILITARY 5 ± 10%, -55°C to +125°C				67401A/67402A—COMM 5 ± 5%, 0°C to 70°C			
			MIN	TYP ³	MAX	UNIT	MIN	TYP ³	MAX	UNIT
f _{IN}	Shift in Clock Rate	1	15			MHz	15			MHz
t _{SIH}	Shift in High Time	1	18			ns	18			ns
t _{SIL}	Shift in Low Time	1	18			ns	18			ns
t _{IRL}	Input Ready ON Delay	1	30			ns	30			ns
t _{IRH}	Input Ready OFF Delay	1	30			ns	30			ns
t _{IDS}	Input Data Set Up	1	5			ns	5			ns
t _{IDH}	Input Data Hold Time	1	12			ns	12			ns
f _{OUT}	Shift Out Clock Rate	2	15			MHz	15			MHz
t _{SOH}	Shift Out High Time	2	18			ns	18			ns
t _{SOL}	Shift Out Low Time	2	18			ns	18			ns
t _{ORL}	Output Ready ON Delay	2	24			ns	24			ns
t _{ORH}	Output Ready OFF Delay	2	24			ns	24			ns
t _{ODH}	Output Data Hold Time	2	25			ns	25			ns
t _{ODS}	Output Data Delay	2	35			ns	35			ns
t _{PT}	Data Throughput Time	Note 1	2.0			μs	2.0			μs
t _{MRW}	Master Reset Pulse	Note 2	15			ns	15			ns
t _{MRORL}	Master Reset to OR Low	5	30			ns	30			ns
t _{MRIRH}	Master Reset to IR High	5	30			ns	30			ns
t _{MRS}	Master Reset to SI	5	20			ns	20			ns
t _{IPH}	Input Ready Pulse High	4	35			ns	35			ns
t _{IPL}	Input Ready Pulse Low	6	35			ns	35			ns
t _{OPH}	Output Ready Pulse High	3	35			ns	35			ns
t _{OPL}	Output Ready Pulse Low	7	35			ns	35			ns

- NOTES: 1. This parameter defines total time from the time data is present at Dn to the time it is available at On with FIFO initially empty and total time from the time data is extracted from Dn to IR High with FIFO initially full.
 2. Master Reset clears the FIFO to the all cells empty state and resets outputs On to zero state.
 3. Typical values @ 5.0V V_{CC} and 25°C.

Functional Description

Data Input

Data is entered into the FIFO on Dn inputs. To enter data the Input Ready (IR) output should be HIGH, indicating that the first location is ready to accept data. Data then present at the data inputs is entered into the first location when the Shift In (SI) is brought HIGH. A SI HIGH signal causes the RI to go LOW. Data remains at the first location until SI is brought LOW. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. If the memory is full, it will remain LOW.

Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the

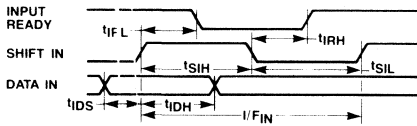
end of the device while empty locations will "bubble" to the front. t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device.

Data Output

Data is read from the On outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the memory is emptied, OR stays LOW.

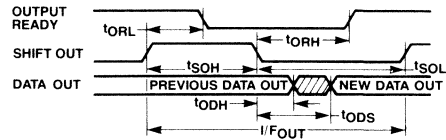
Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

Timing Diagrams



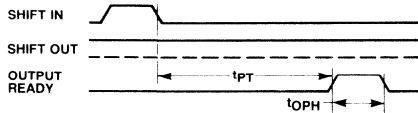
1. Input data must remain stable during t_{IDS} and t_{IDH} .
2. Input Ready HIGH indicates that space is available and a Shift In pulse may be applied. Input Ready LOW indicates that the FIFO is full or that a previous Shift In operation is not complete. Shift In pulses applied while Input Ready is LOW will be ignored.
3. The rise of Input Ready indicates that the data at the Dn inputs has been accepted and that the input stage is empty.

Figure 1. FIFO Input Timing



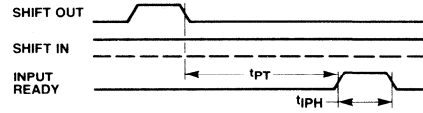
1. Output data will be stable at the rise of Output Ready.
2. Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied. Output Ready LOW indicates that the FIFO is empty or that a previous Shift Out operation is still in progress. Shift Out pulses applied while Shift Out Ready is LOW will be ignored.
3. The rise of Output Ready indicates that new data has been loaded into the output stage.

Figure 2. FIFO Output Timing



1. FIFO initially empty.
2. Shift Out held high (as shown).

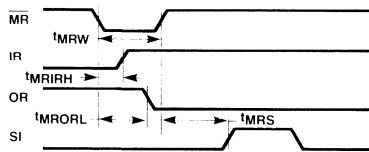
Figure 3. t_{OPH} Specification



1. FIFO initially full.
2. Shift In held high (as shown).

Figure 4. t_{IPH} Specification

5



1. FIFO initially full

Figure 5. FIFO Master Reset Timing

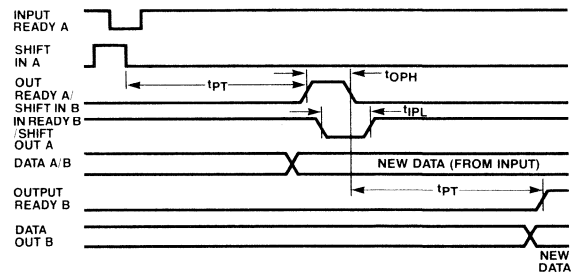
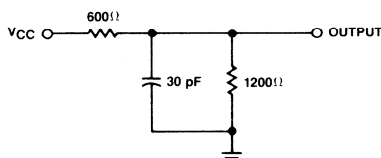


Figure 6. FIFO/FIFO Communication: Empty/Input Timing

Standard Test Circuit



Input Pulse Amplitude = 2.5V
 Input Rise and Fall Time = 5.0 ns from 1.0V to 2.0V
 Measurements made at 1.50V

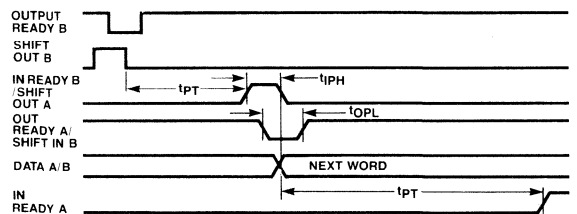
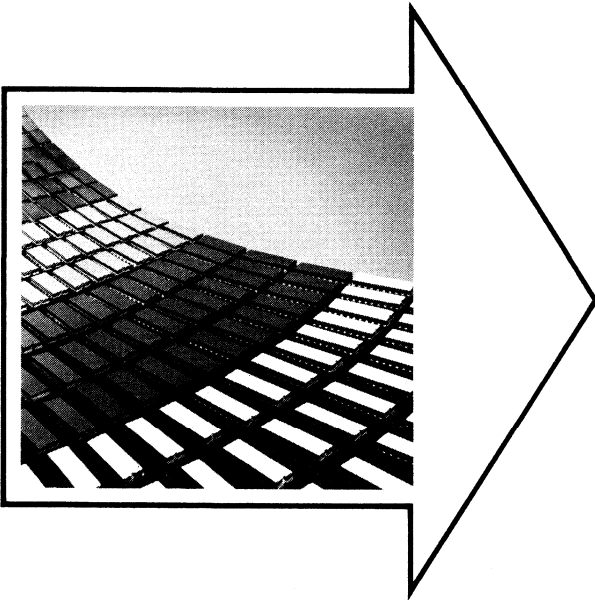


Figure 7. FIFO/FIFO Communication: Full/Output Timing



Introduction	1
PROMS	2
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Programmable Array Logic Family

PAL Series 20 Data Sheet

Patent Allowed

Features/Benefits

- Programmable replacement for conventional TTL logic.
- Reduces IC inventories substantially and simplifies their control.
- Reduces chip count by 4 to 1.
- Expedites and simplifies prototyping and board layout.
- Saves space with 20-pin Skinny DIP packages.
- High speed: 25ns typical propagation delay.
- Programmed on standard PROM programmers.
- Programmable three-state outputs.
- Special feature reduces possibility of copying by competitors.

Description

The PAL family utilizes an advanced Schottky TTL process and the Bipolar PROM fusible link technology to provide user programmable logic for replacing conventional SSI/MSI gates and flip-flops at reduced chip count.

The family lets the systems engineer "design his own chip" by blowing fusible links to configure AND and OR gates to perform his desired logic function. Complex interconnections which previously required time-consuming layout are thus "lifted" from PC board etch and placed on silicon where they can be easily modified during prototype check-out or production.

The PAL transfer function is the familiar sum of products. Like the PROM, the PAL has a single array of fusible links. Unlike the PROM, the PAL is a programmable AND array driving a fixed OR array (the PROM is a fixed AND array driving a programmable OR array). In addition the PAL provides these options:

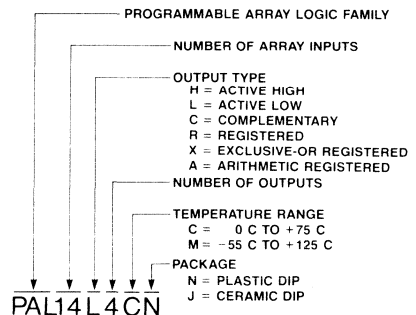
- Variable input/output pin ratio
- Programmable three-state outputs
- Registers with feedback
- Arithmetic capability

Unused inputs are tied directly to V_{CC} or GND. Product terms with all fuses blown assume the logical high state, and product terms connected to both true and complement of any single input assume the logical low state. Registers consist of D type flip-flops which are loaded on the low to high transition of the clock. All registers are designed to power up to logical high state at the output pin. PAL Logic Diagrams are shown with all fuses blown, enabling the designer use of the diagrams as coding sheets. 8½ x 11 Logic Diagrams are available on request.

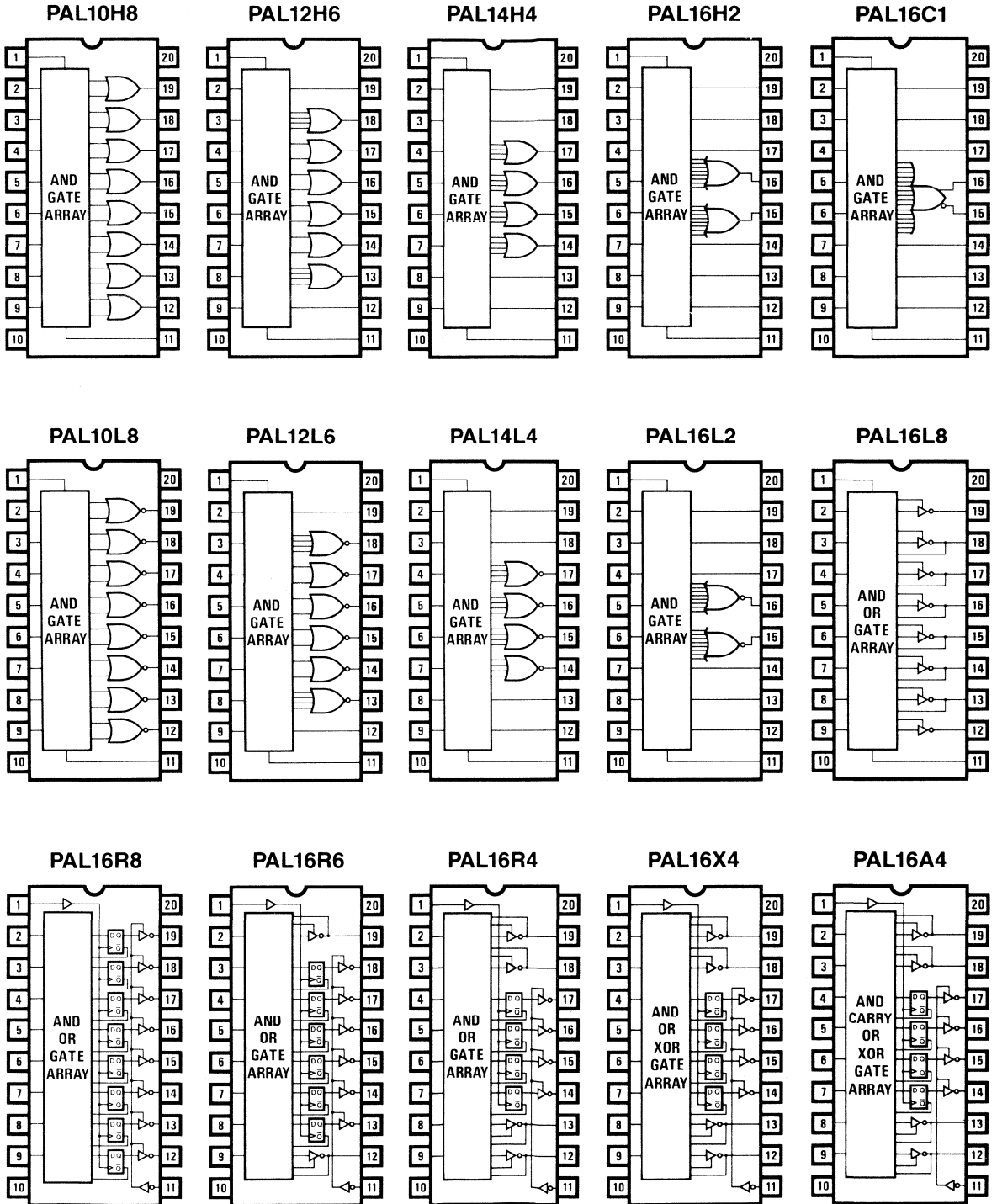
The entire PAL family is programmed on inexpensive conventional PROM programmers with appropriate personality and socket adapter cards. Once the PAL is programmed and verified, two additional fuses may be blown to defeat verification. This feature gives the user a proprietary circuit which is very difficult to copy.

PART NUMBER	DESCRIPTION
PAL10H8	OCTAL 10 INPUT AND-OR GATE ARRAY
PAL12H6	HEX 12 INPUT AND-OR GATE ARRAY
PAL14H4	QUAD 14 INPUT AND-OR GATE ARRAY
PAL16H2	DUAL 16 INPUT AND-OR GATE ARRAY
PAL16C1	16 INPUT AND-OR/AND-OR-INVERT GATE ARRAY
PAL10L8	OCTAL 10 INPUT AND-OR-INVERT GATE ARRAY
PAL12L6	HEX 12 INPUT AND-OR-INVERT GATE ARRAY
PAL14L4	QUAD 14 INPUT AND-OR-INVERT GATE ARRAY
PAL16L2	DUAL 16 INPUT AND-OR-INVERT GATE ARRAY
PAL16L8	OCTAL 16 INPUT AND-OR-INVERT GATE ARRAY
PAL16R8	OCTAL 16 INPUT REGISTERED AND-OR GATE ARRAY
PAL16R6	HEX 16 INPUT REGISTERED AND-OR GATE ARRAY
PAL16R4	QUAD 16 INPUT REGISTERED AND-OR GATE ARRAY
PAL16X4	QUAD 16 INPUT REGISTERED AND-OR-XOR GATE ARRAY
PAL16A4	QUAD 16 INPUT REGISTERED AND-CARRY-OR-XOR GATE ARRAY

Ordering Information



PAL Logic Symbols



6

PRELIMINARY
DATA

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	7V	12V
Input voltage	5.5V	12V
Off-state output voltage	5.5V	12V
Storage temperature range	-65°C to	150°C

10H8, 12H6, 14H4, 16H2, 16C1, 10L8, 12L6, 14L4, 16L2

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.75	5.00	5.25	V
I_{OH}	High-level output current			-2.0			-3.2	mA
I_{OL}	Low-level output current			8			8	mA
T_A	Operating free air temperature	-55		125	0		75	°C

Electrical Characteristics

Over Recommended Operating Temperature Range

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IC}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2V,$ $V_{IL} = 0.8V, I_{OH} = \text{MAX}$	2.4			V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2V,$ $V_{IL} = 0.8V, I_{OL} = \text{MAX}$			0.5	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5V$			1.0	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4V$			25	μA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4V$			-250	μA
I_{OS}	Short-circuit output current	$V_{CC} = \text{MAX}$	-30		-130	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}$		55	90	mA

Switching Characteristics

Over Recommended Ranges of Temperature and V_{CC}

SYMBOL	PARAMETER	TEST CONDITIONS ^{††} $R_L = 2.0 \text{ K}\Omega$	MILITARY $T_A = -55^\circ \text{ to } +125^\circ \text{C}$ $V_{CC} = 5.0V \pm 10\%$			COMMERCIAL $T_A = 0^\circ \text{ to } 75^\circ \text{C}$ $V_{CC} = 5.0V \pm 5\%$			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	From any input to any output	$C_L = 15\text{pF}$		45			40		ns

^{††} See Standard Test Load and Definition of Waveforms, page 10-4

PAL Series 20

16L8, 16R8, 16R6, 16R4, 16X4[†], 16A4[†]

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5.0	5.5	4.75	5.00	5.25	V
I _{OH}	High-level output current			-2.0			3.2	mA
I _{OL}	Low-level output current			12			24	mA
T _A	Operating free air temperature	-55		125*	0		75	C

Electrical Characteristics

Over Recommended Operating Temperature Range

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{IH}	High-level input voltage		2			V
V _{IL}	Low-level input voltage				0.8	V
V _{IC}	Input clamp voltage	V _{CC} = MIN, I _i = -18mA			-1.5	V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IH} = 2V, V _{IL} = 0.8V, I _{OH} = MAX	2.4			V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2V, V _{IL} = 0.8V, I _{OL} = MAX			0.5	V
I _{OZH}	Off-state output current high-level voltage applied	V _{CC} = MAX, V _{IH} = 2V, V _O = 2.4V, V _{IL} = 0.8V			100	μA
I _{OZL}	Off-state output current low-level voltage applied	V _{CC} = MAX, V _{IH} = 2V, V _O = 0.4V, V _{IL} = 0.8V			-100	μA
I _i	Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V			1.0	mA
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.4V			25	μA
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.4V			-250	μA
I _{OS}	Short-circuit output current	V _{CC} = MAX,	-30		-130	mA
I _{CC}	Supply Current	16L8		140	210 [†]	mA
		16R4, 16R6, 16R8		150	225 [†]	
		16X4, 16A4		160		

6

Switching Characteristics

Over Recommended Ranges of Temperature and V_{CC}

SYMBOL	PARAMETER	TEST CONDITIONS ^{††} R _L = 667 Ω	MILITARY T _A = -55° to +125°C V _{CC} = 5.0V ± 10%			COMMERCIAL T _A = -0° to +75°C V _{CC} = 5.0V ± 5%			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t _{PD}	Input to output	C _L = 45pF	25	45		25	40	ns	
t _{PD}	Clock to output		15	25		15	25	ns	
t _{PZX}	Pin 11 to output enable		15	25		15	25	ns	
t _{PXZ}	Pin 11 to output disable	C _L = 5pF	15	25		15	25	ns	
t _{PZX}	Input to output enable	C _L = 45pF	25	45		25	40	ns	
t _{PXZ}	Input to output disable	C _L = 5pF	25	45		25	40	ns	
t _w	Width of clock	High	25			25		ns	
		Low	25			25			
t _{su}	Setup time	16R8, 16R6, 16R4	45			40		ns	
		16X4, 16A4							
t _h	Hold time		0	-15		0	-15	ns	

*Operating Case Temperature only, T_C = 125°C

[†]I_{CC} = MAX at minimum temperature

^{††} See Standard Test Load and Definition of Waveforms, page 10-4

† PRELIMINARY

Programming

PAL fuses are programmed using a low-voltage linear-select procedure which is common to all 15 PAL types. The array is divided into two groups, products 0 thru 31 and products 32 thru 63, for which pin identifications are shown in Figure 1. To program a particular fuse, both an input line and a product line are selected according to the following procedure:

- Step 1 Raise Output Disable, OD, to V_{IHH}
- Step 2 Select an input line by specifying $I_0, I_1, I_2, I_3, I_4, I_5, I_6, I_7$ and L/R as shown in Table 1
- Step 3 Select a product line by specifying A_0, A_1 and A_2 one-of-eight select as shown in Table 2
- Step 4 Raise V_{CC} (pin 20) to V_{IHH}
- Step 5 Program the fuse by pulsing the output pins, O, of the selected product group to V_{IHH} as shown in Table 2.
- Step 6 Lower V_{CC} (pin 20) to 6.0 V
- Step 7 Pulse the CLOCK pin and verify the output pin, O, to be Low for active Low PAL types or High for active High PAL types.
- Step 8 Lower V_{CC} (pin 20) to 4.2 V and repeat step 7
- Step 9 Should the output not verify, repeat steps 1 thru 8 up to five (5) times.

This procedure is repeated for all fuses to be blown (see programming waveforms).

To prevent further verification, two last fuses may be blown by raising pin 1 and pin 11 to VP. V_{CC} is not required during this operation.

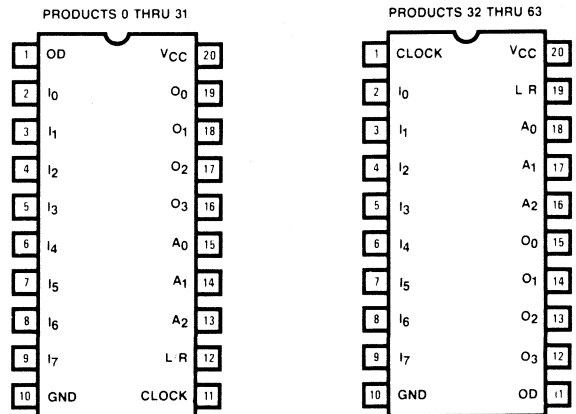
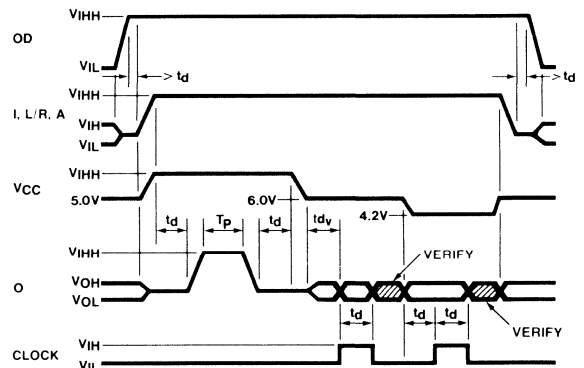


Figure 1 Pin Identification

Programming Waveforms



Programming Parameters

$T_A = 25^\circ C$

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	TYP	MAX	
V_{IHH}	Program-level input voltage	10.5	11	11.5	V
I_{IHH}	Program-level input current	Output Program Pulse			mA
		OD, L/R			
		All Other Inputs			
I_{CCH}	Program Supply Current			400	mA
T_P	Program Pulse Width	10		50	μS
t_d	Delay time	100			ns
	Program Pulse duty cycle			25	%
V_P	Program/Verify-Protect-input voltage		20		V
I_P	Program/Verify-Protect-input current			400	mA
t_{dv}	Delay Time to Verify	100			μS

Voltage Legend

- L = Low-level input voltage, V_{IL}
- H = High-level input voltage, V_{IH}
- HH = High-level program voltage, V_{IHH}
- Z = High impedance (e.g. 10 K Ω to +5.0 V)

INPUT LINE NUMBER	PIN IDENTIFICATION								
	I7	I6	I5	I4	I3	I2	I1	I0	L/R
0	HH	HH	HH	HH	HH	HH	HH	L	L
1	HH	HH	HH	HH	HH	HH	HH	H	L
2	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	L	HH	L
5	HH	HH	HH	HH	HH	HH	H	HH	L
6	HH	HH	HH	HH	HH	HH	L	HH	HH
7	HH	HH	HH	HH	HH	HH	H	HH	HH
8	HH	HH	HH	HH	HH	L	HH	HH	L
9	HH	HH	HH	HH	HH	H	HH	HH	L
10	HH	HH	HH	HH	HH	L	HH	HH	HH
11	HH	HH	HH	HH	HH	H	HH	HH	HH
12	HH	HH	HH	HH	L	HH	HH	HH	L
13	HH	HH	HH	HH	H	HH	HH	HH	L
14	HH	HH	HH	HH	L	HH	HH	HH	HH
15	HH	HH	HH	HH	H	HH	HH	HH	HH
16	HH	HH	HH	L	HH	HH	HH	HH	L
17	HH	HH	HH	H	HH	HH	HH	HH	L
18	HH	HH	HH	L	HH	HH	HH	HH	HH
19	HH	HH	HH	H	HH	HH	HH	HH	HH
20	HH	HH	L	HH	HH	HH	HH	HH	L
21	HH	HH	H	HH	HH	HH	HH	HH	L
22	HH	HH	L	HH	HH	HH	HH	HH	HH
23	HH	HH	H	HH	HH	HH	HH	HH	HH
24	HH	L	HH	HH	HH	HH	HH	HH	L
25	HH	H	HH	HH	HH	HH	HH	HH	L
26	HH	L	HH	HH	HH	HH	HH	HH	HH
27	HH	H	HH	HH	HH	HH	HH	HH	HH
28	L	HH	HH	HH	HH	HH	HH	HH	L
29	H	HH	HH	HH	HH	HH	HH	HH	L
30	L	HH	HH	HH	HH	HH	HH	HH	HH
31	H	HH	HH	HH	HH	HH	HH	HH	HH

Table 1 Input Line Select

PRODUCT LINE NUMBER	PIN IDENTIFICATION						
	O3	O2	O1	O0	A2	A1	A0
0, 32	Z	Z	Z	HH	Z	Z	Z
1, 33	Z	Z	Z	HH	Z	Z	HH
2, 34	Z	Z	Z	HH	Z	HH	Z
3, 35	Z	Z	Z	HH	Z	HH	HH
4, 36	Z	Z	Z	HH	HH	Z	Z
5, 37	Z	Z	Z	HH	HH	Z	HH
6, 38	Z	Z	Z	HH	HH	HH	Z
7, 39	Z	Z	Z	HH	HH	HH	HH
8, 40	Z	Z	HH	Z	Z	Z	Z
9, 41	Z	Z	HH	Z	Z	Z	HH
10, 42	Z	Z	HH	Z	Z	HH	Z
11, 43	Z	Z	HH	Z	Z	HH	HH
12, 44	Z	Z	HH	Z	HH	Z	Z
13, 45	Z	Z	HH	Z	HH	Z	HH
14, 46	Z	Z	HH	Z	HH	HH	Z
15, 47	Z	Z	HH	Z	HH	HH	HH
16, 48	Z	HH	Z	Z	Z	Z	Z
17, 49	Z	HH	Z	Z	Z	Z	HH
18, 50	Z	HH	Z	Z	Z	HH	Z
19, 51	Z	HH	Z	Z	Z	HH	HH
20, 52	Z	HH	Z	Z	HH	Z	Z
21, 53	Z	HH	Z	Z	HH	Z	HH
22, 54	Z	HH	Z	Z	HH	HH	Z
23, 55	Z	HH	Z	Z	HH	HH	HH
24, 56	HH	Z	Z	Z	Z	Z	Z
25, 57	HH	Z	Z	Z	Z	Z	HH
26, 58	HH	Z	Z	Z	Z	HH	Z
27, 59	HH	Z	Z	Z	Z	HH	HH
28, 60	HH	Z	Z	Z	HH	Z	Z
29, 61	HH	Z	Z	Z	HH	Z	HH
30, 62	HH	Z	Z	Z	HH	HH	Z
31, 63	HH	Z	Z	Z	HH	HH	HH

Table 2 Product Line Select

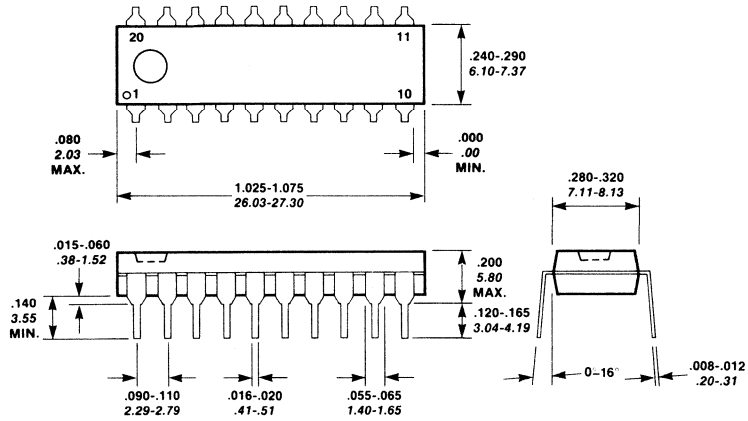
Approved Programmers:

- Data I/O models 5 or 9
- Programming card set: 909-1427
- Socket adapters: VOH-PAL: 715-1428-1
- Socket adapters: VOL-PAL: 715-1428-2
- Socket adapters: COMPL-PAL: 715-1428-3

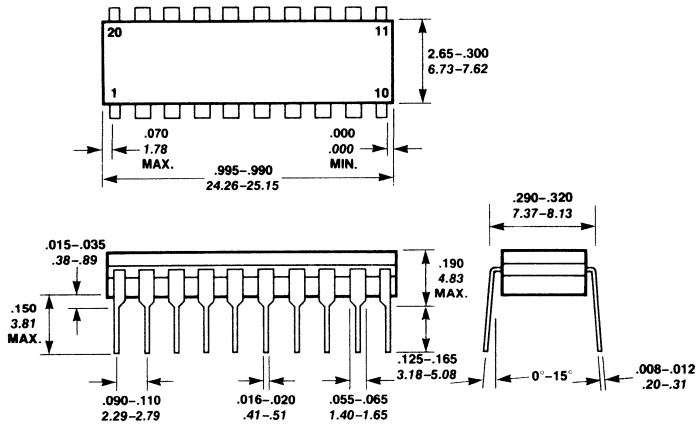
Package Drawings

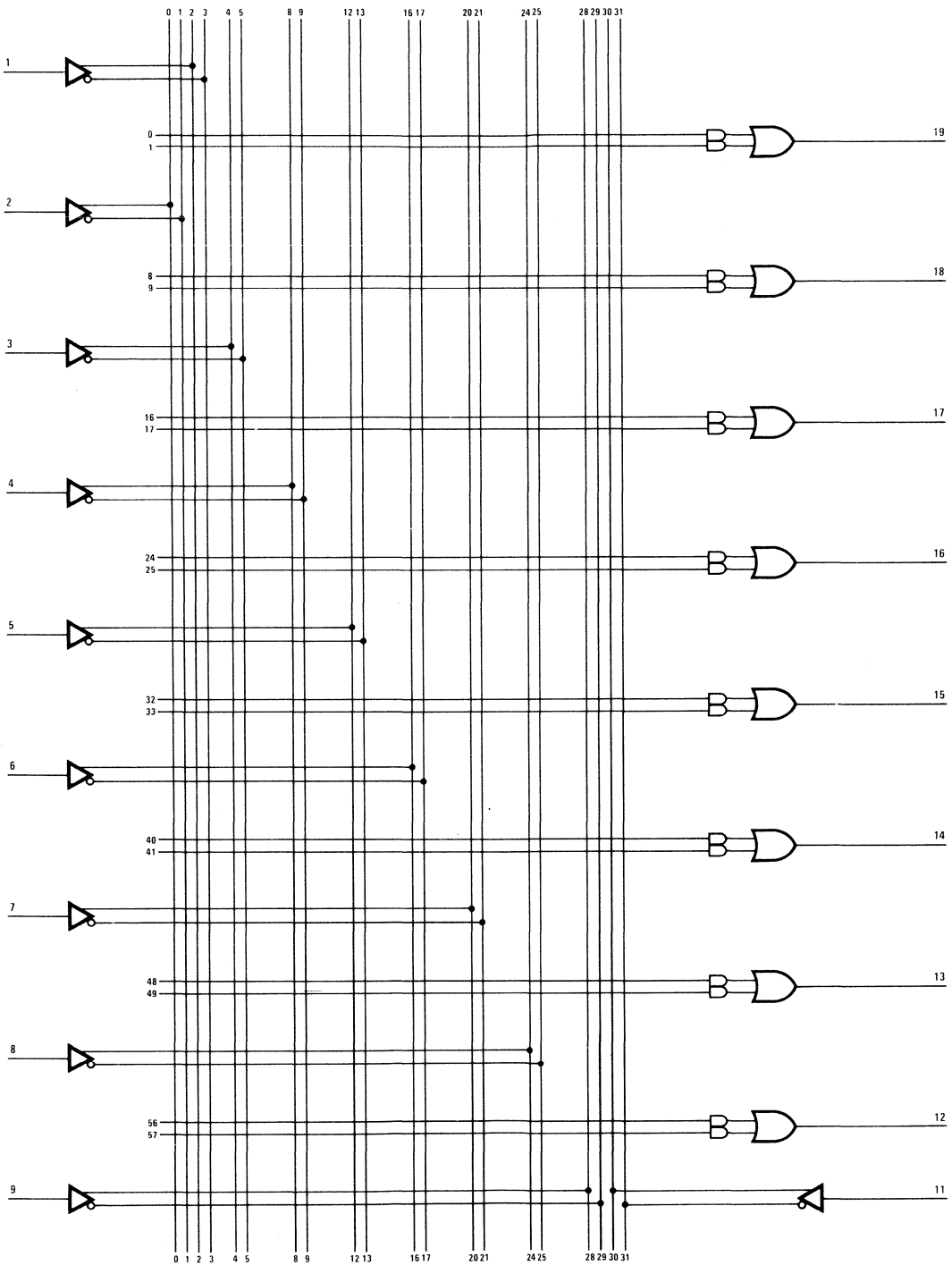
UNLESS OTHERWISE SPECIFIED:
 ALL DIMENSIONS MIN.-MAX. IN INCHES.
 ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.

N20 Plastic Dip

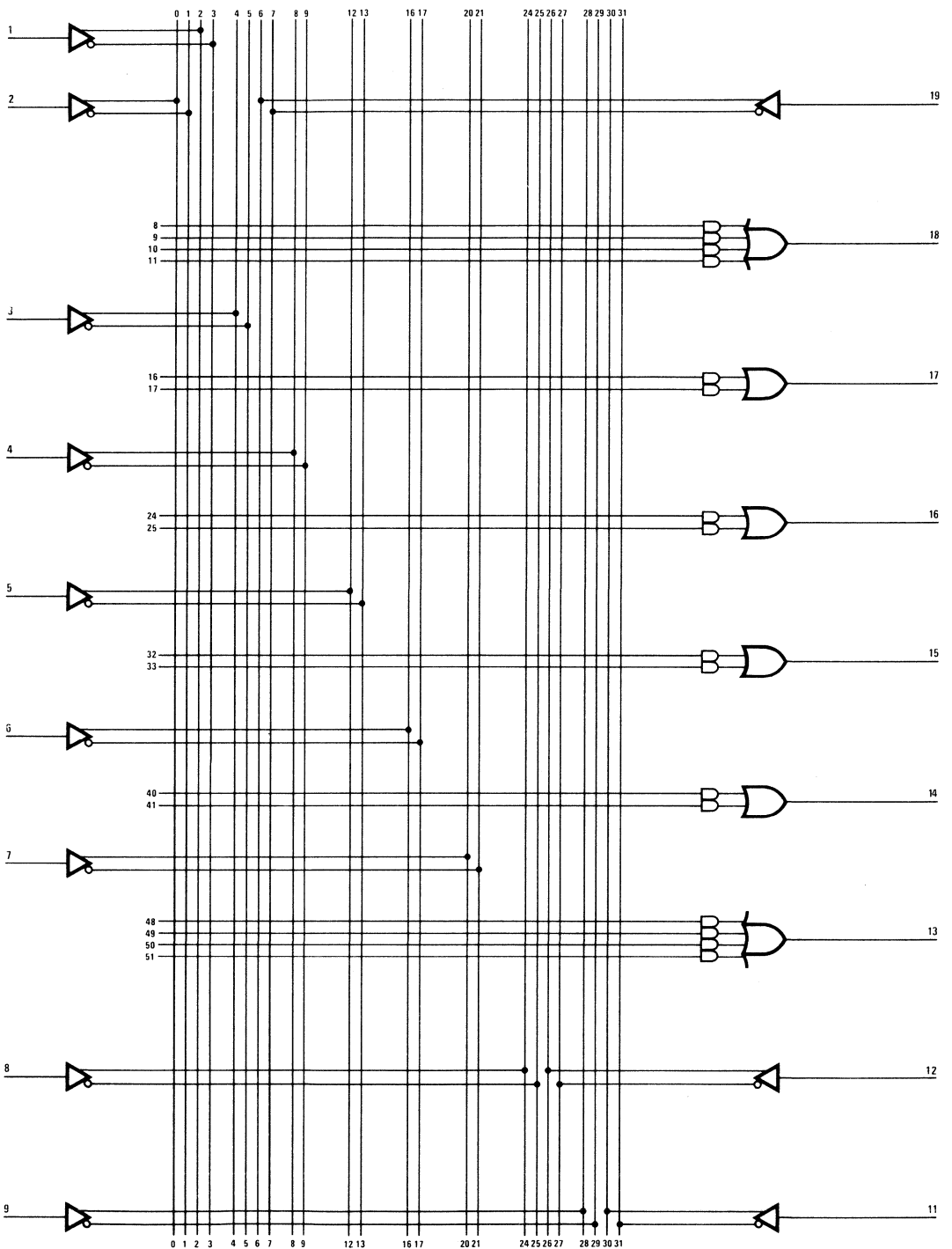


J20 Ceramic Dip

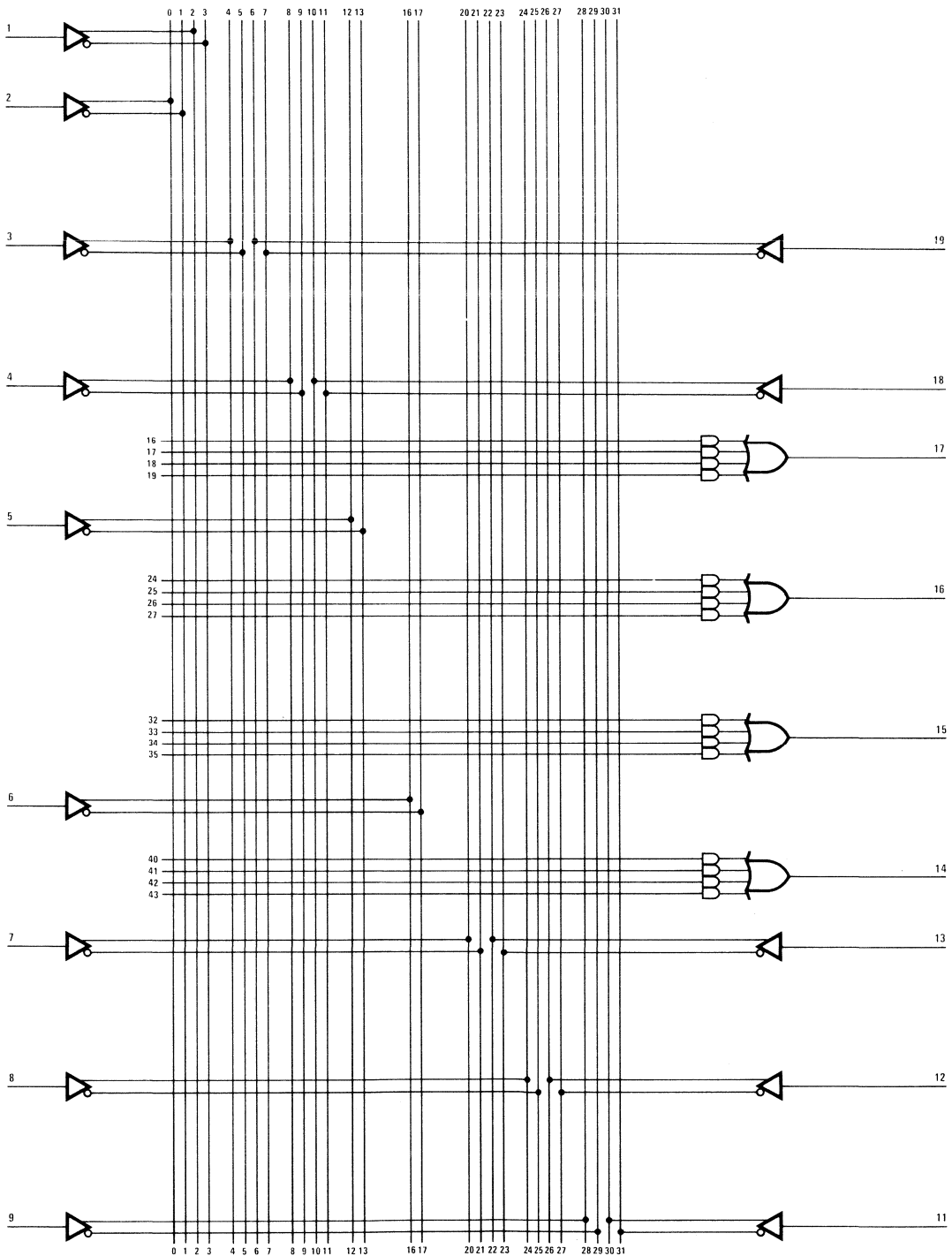




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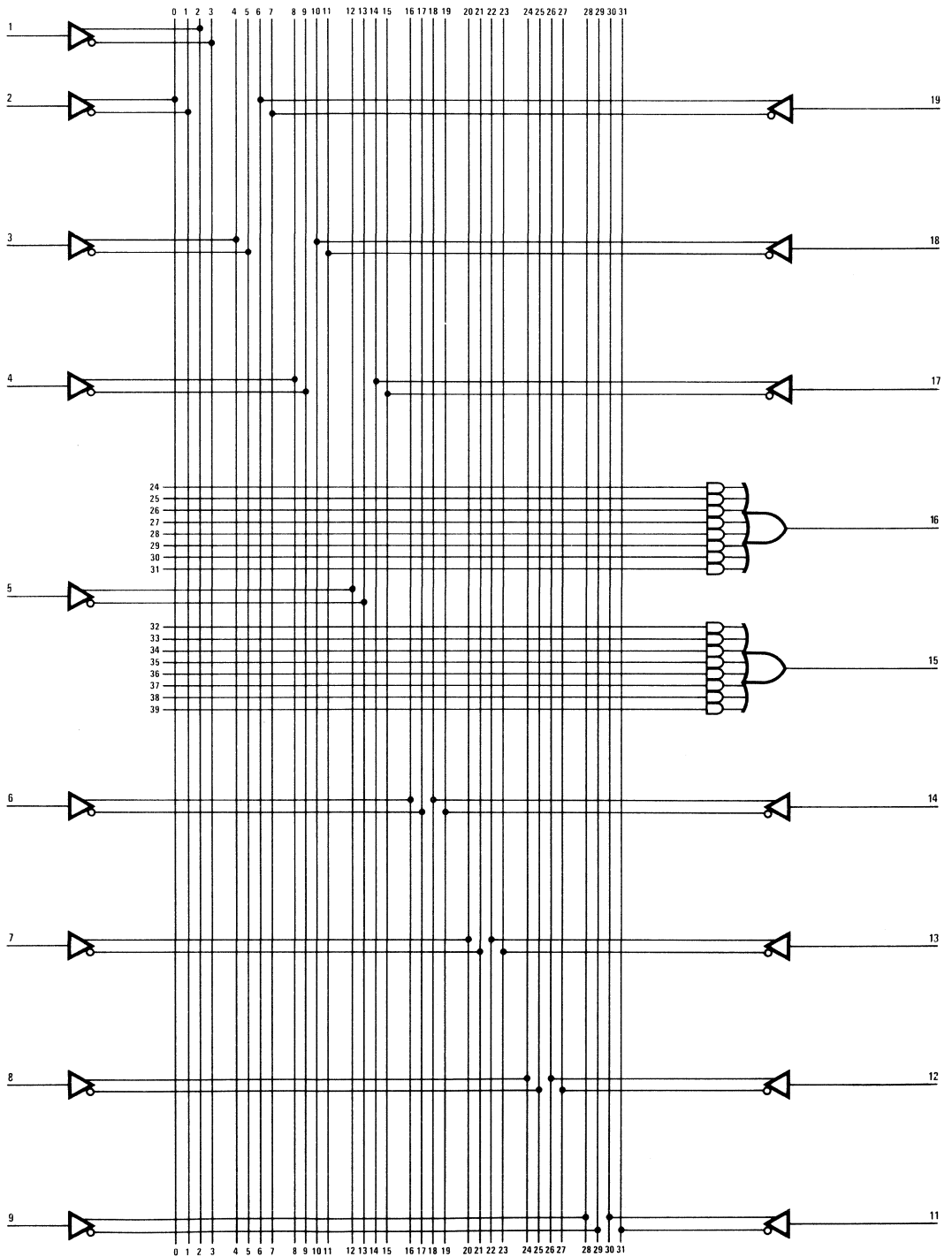


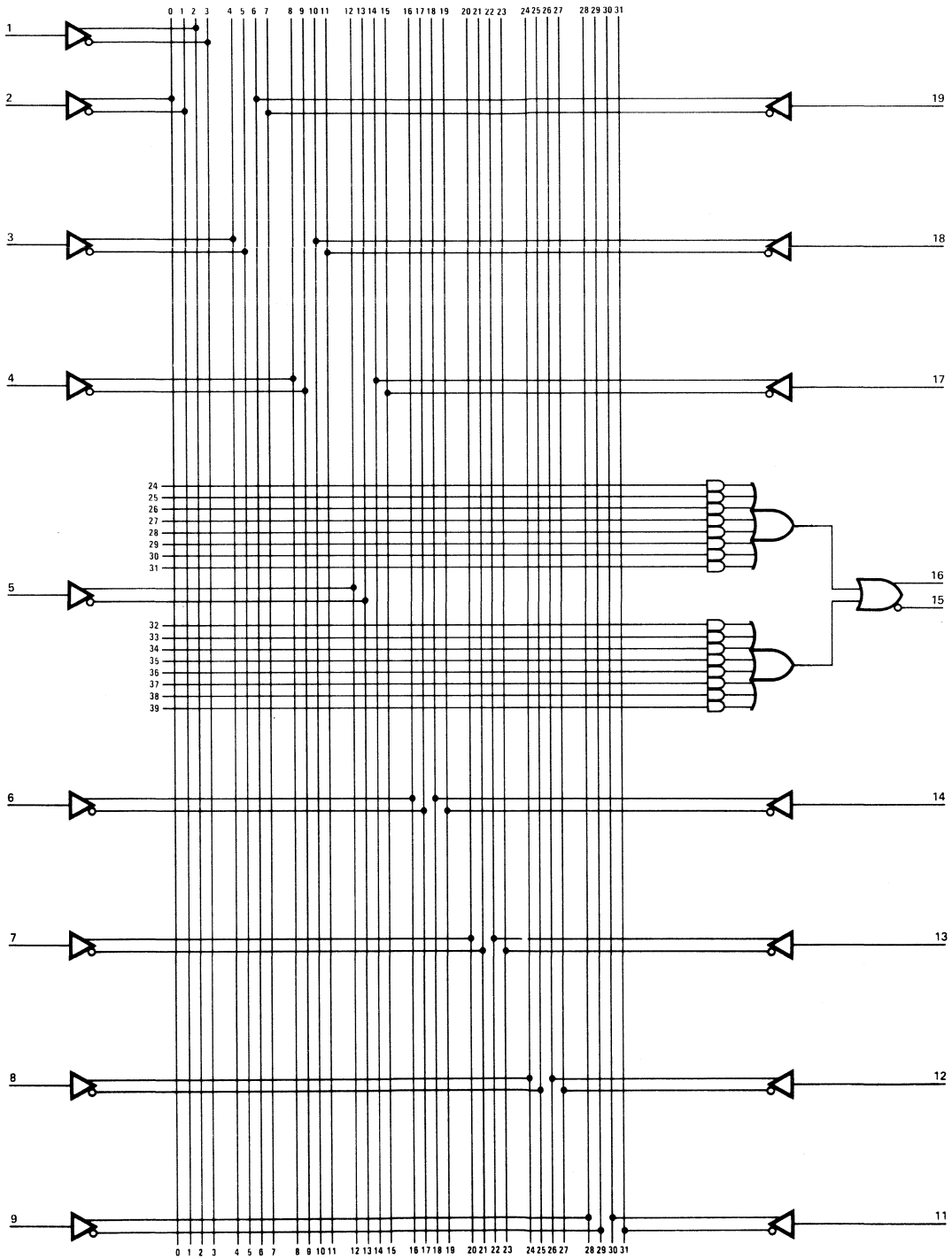
Logic Diagram PAL14H4



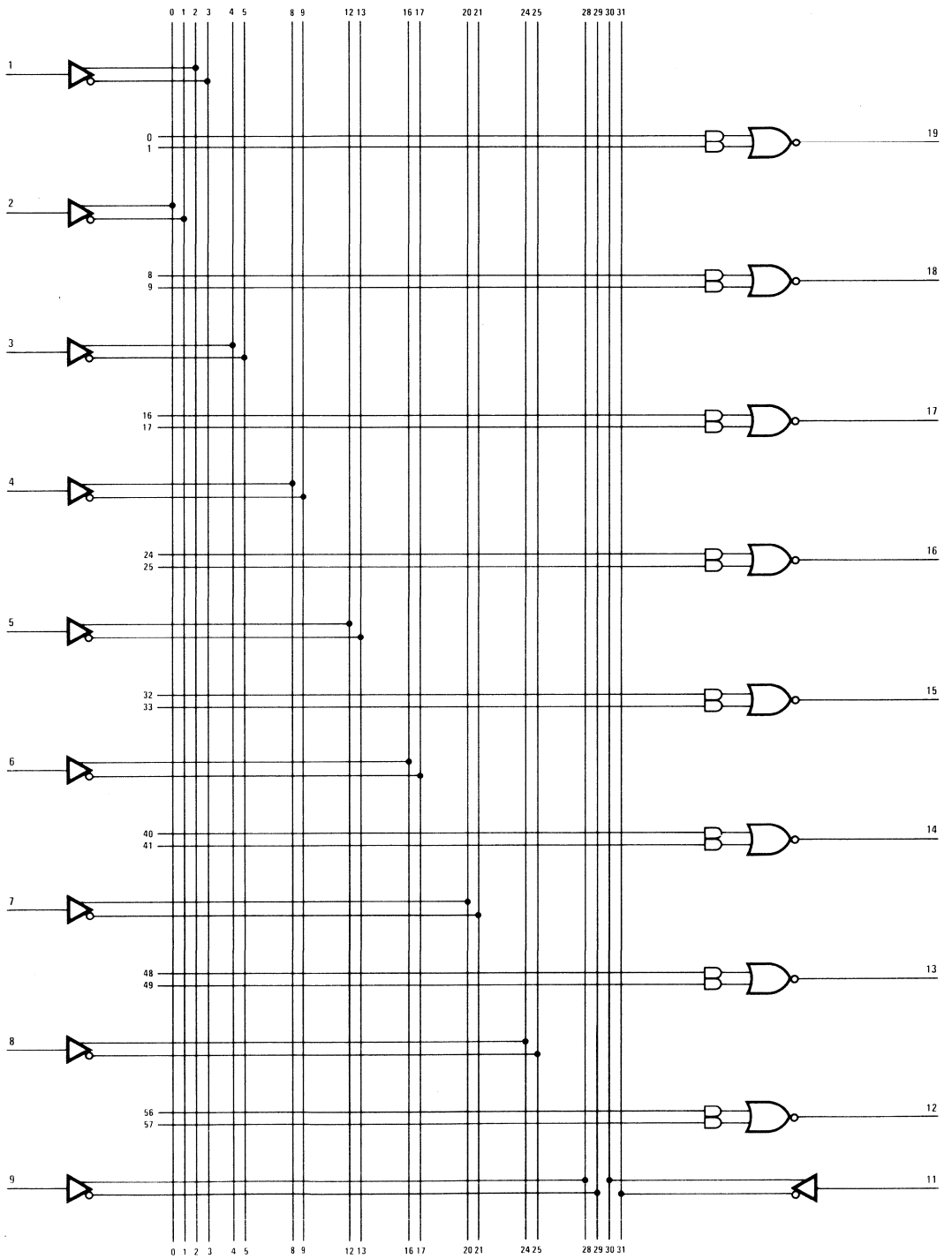
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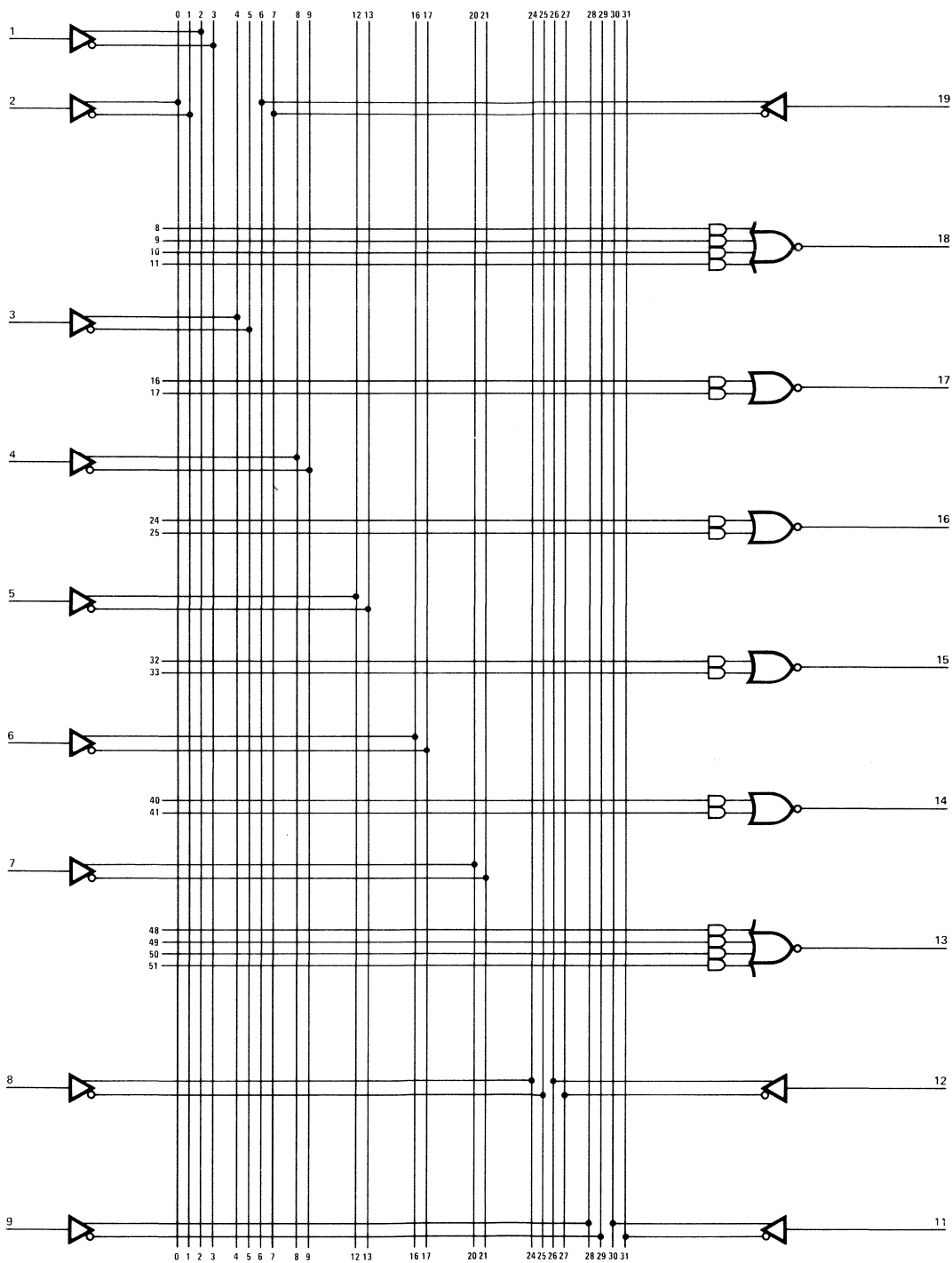
Logic Diagram PAL16H2



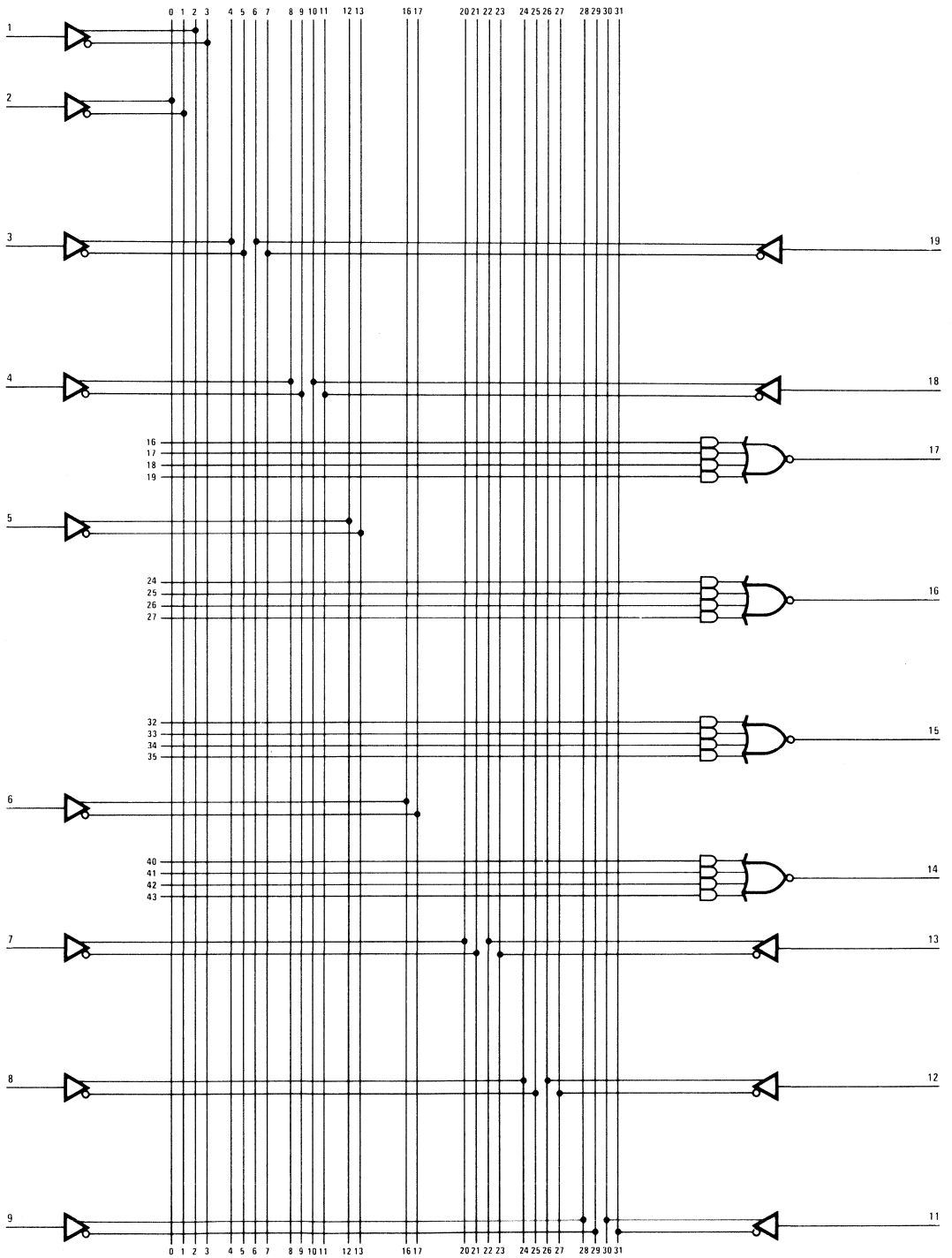


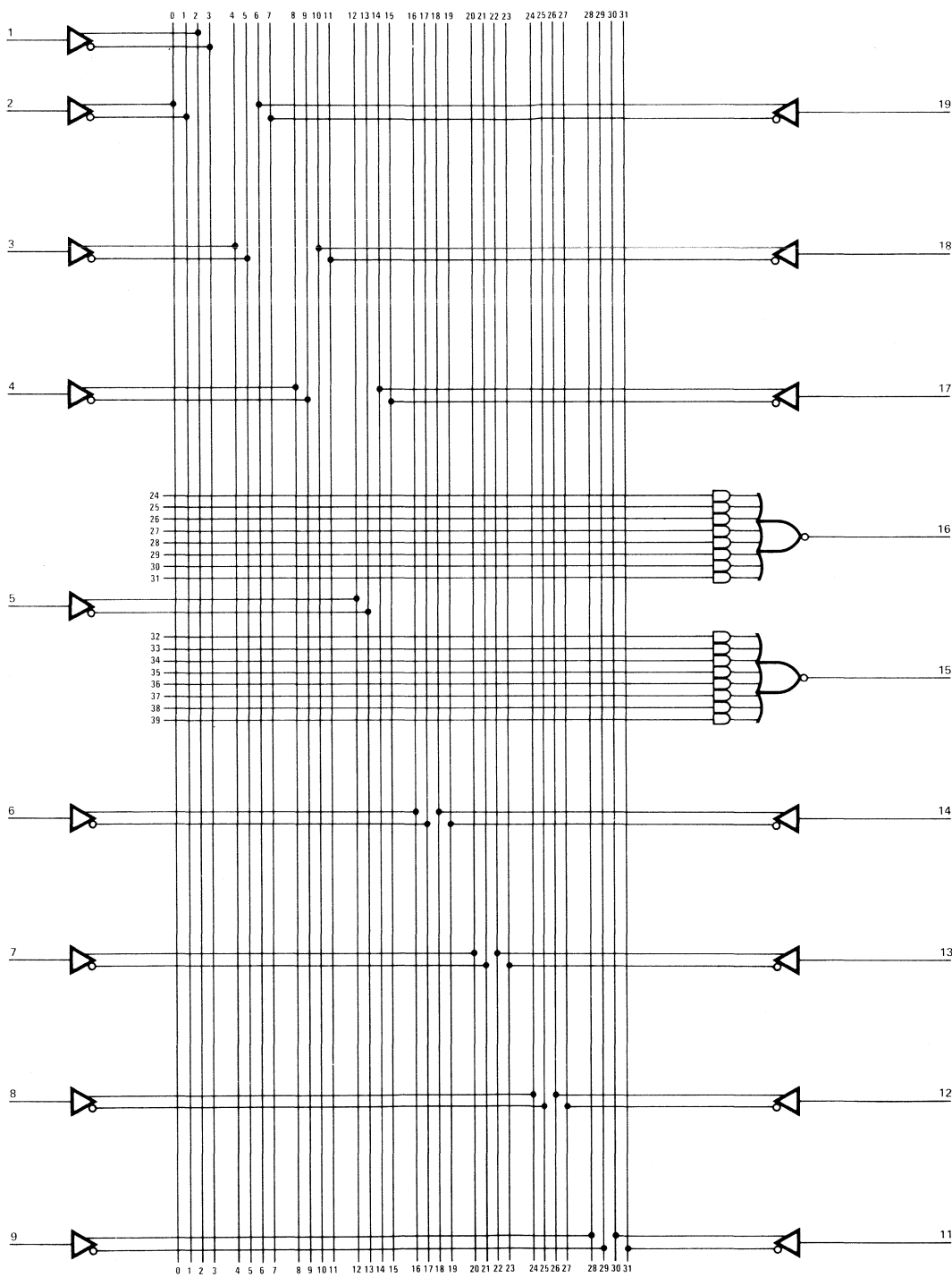
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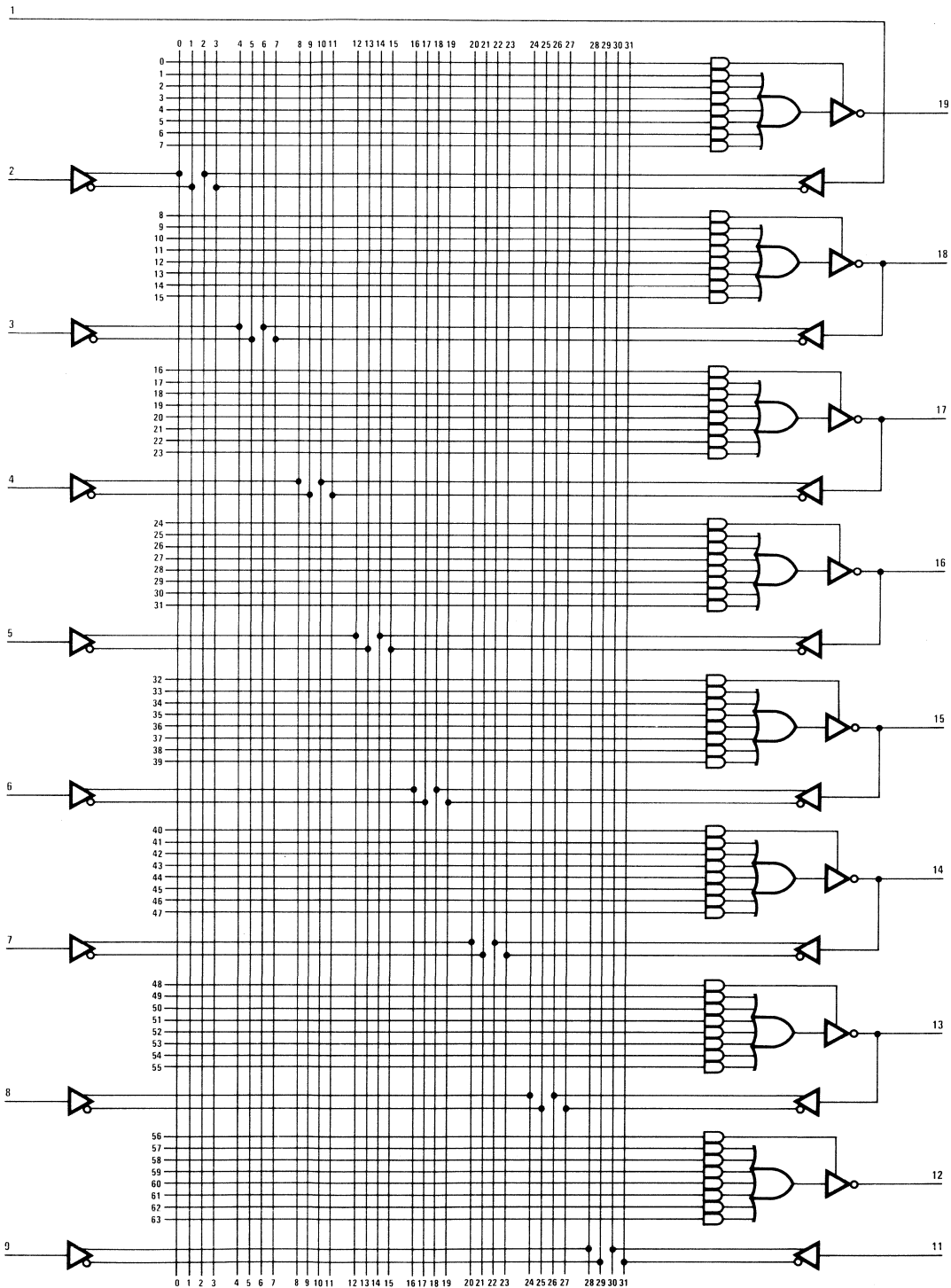
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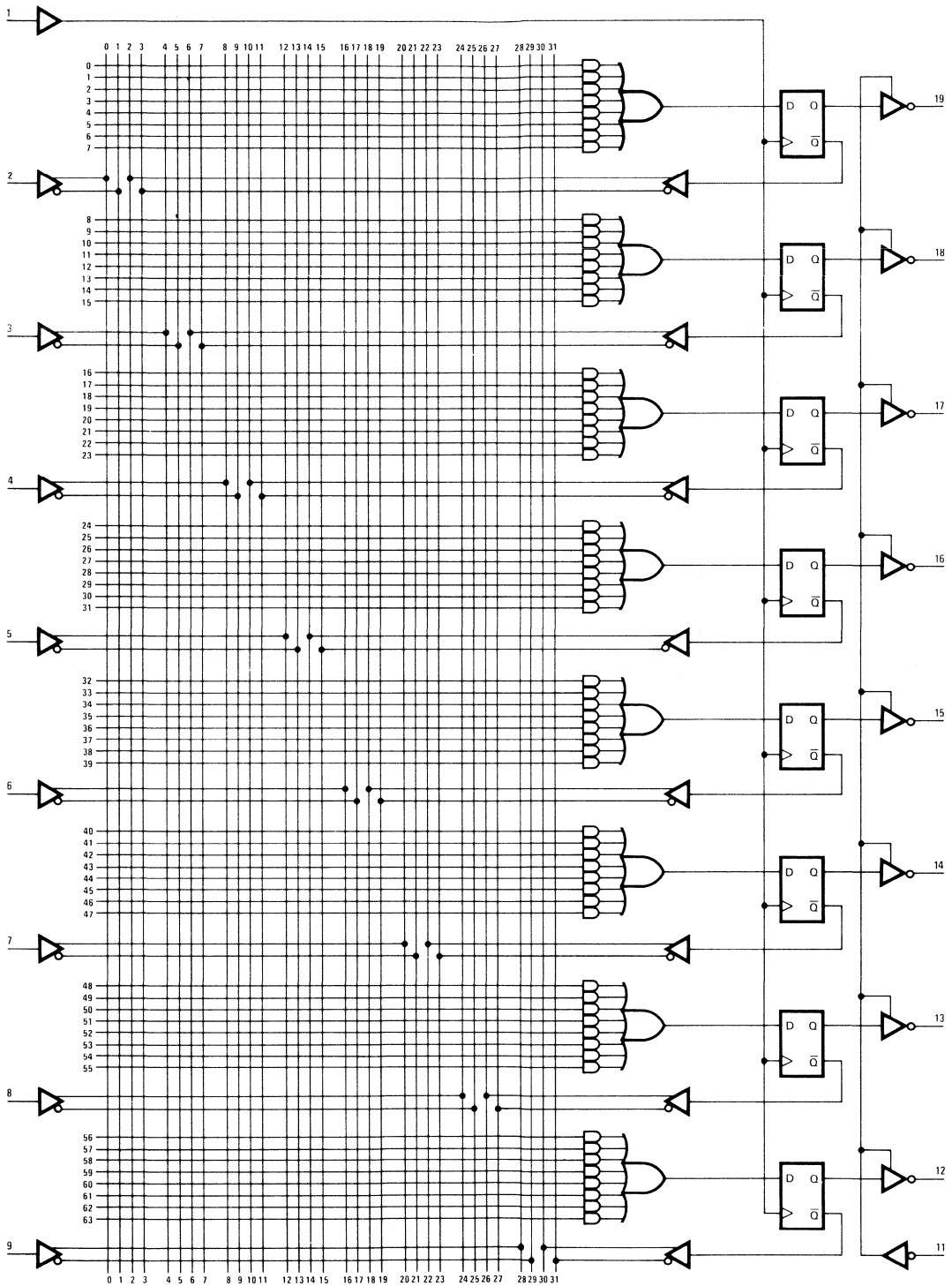


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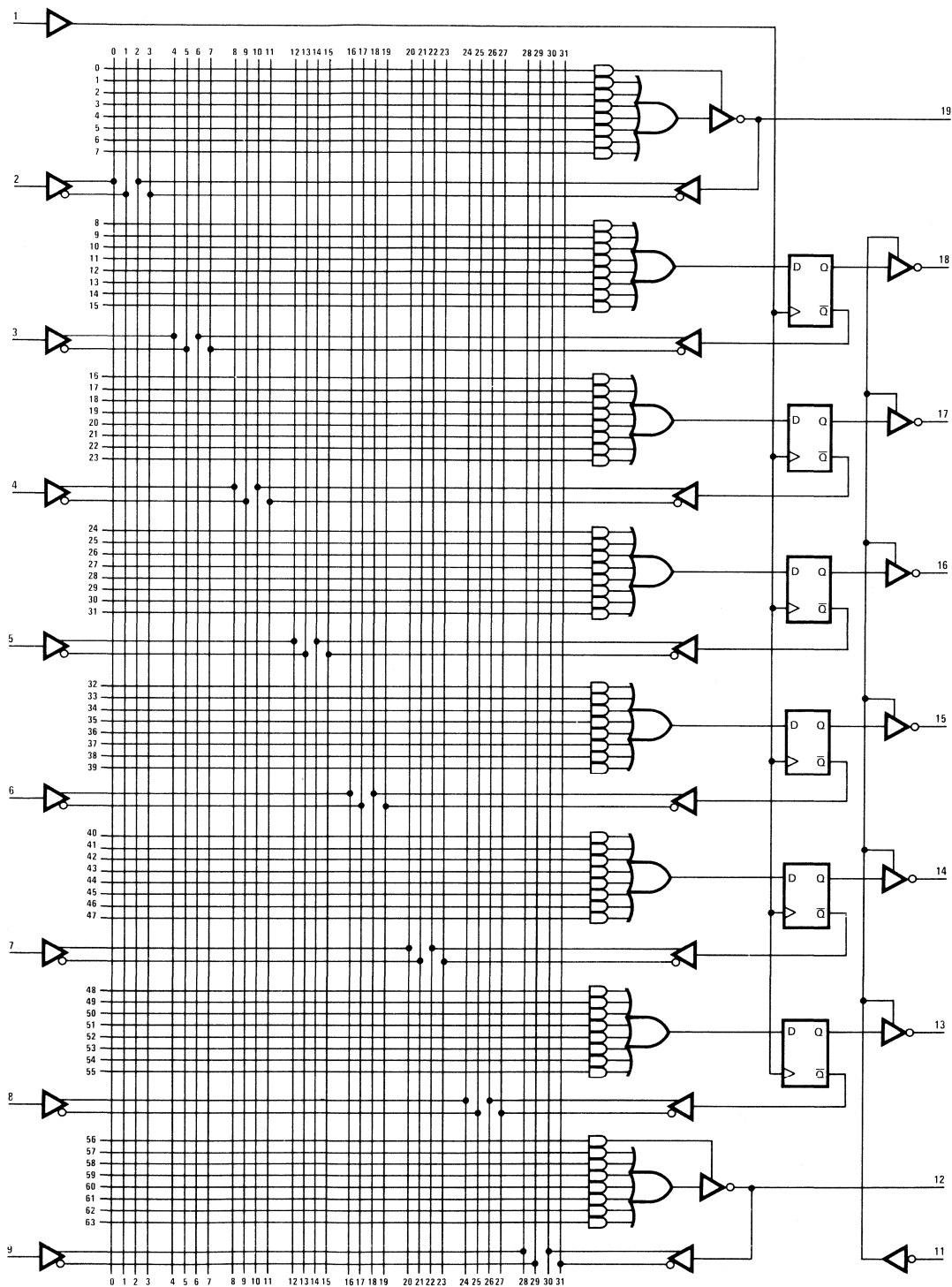
Logic Diagram PAL16L8



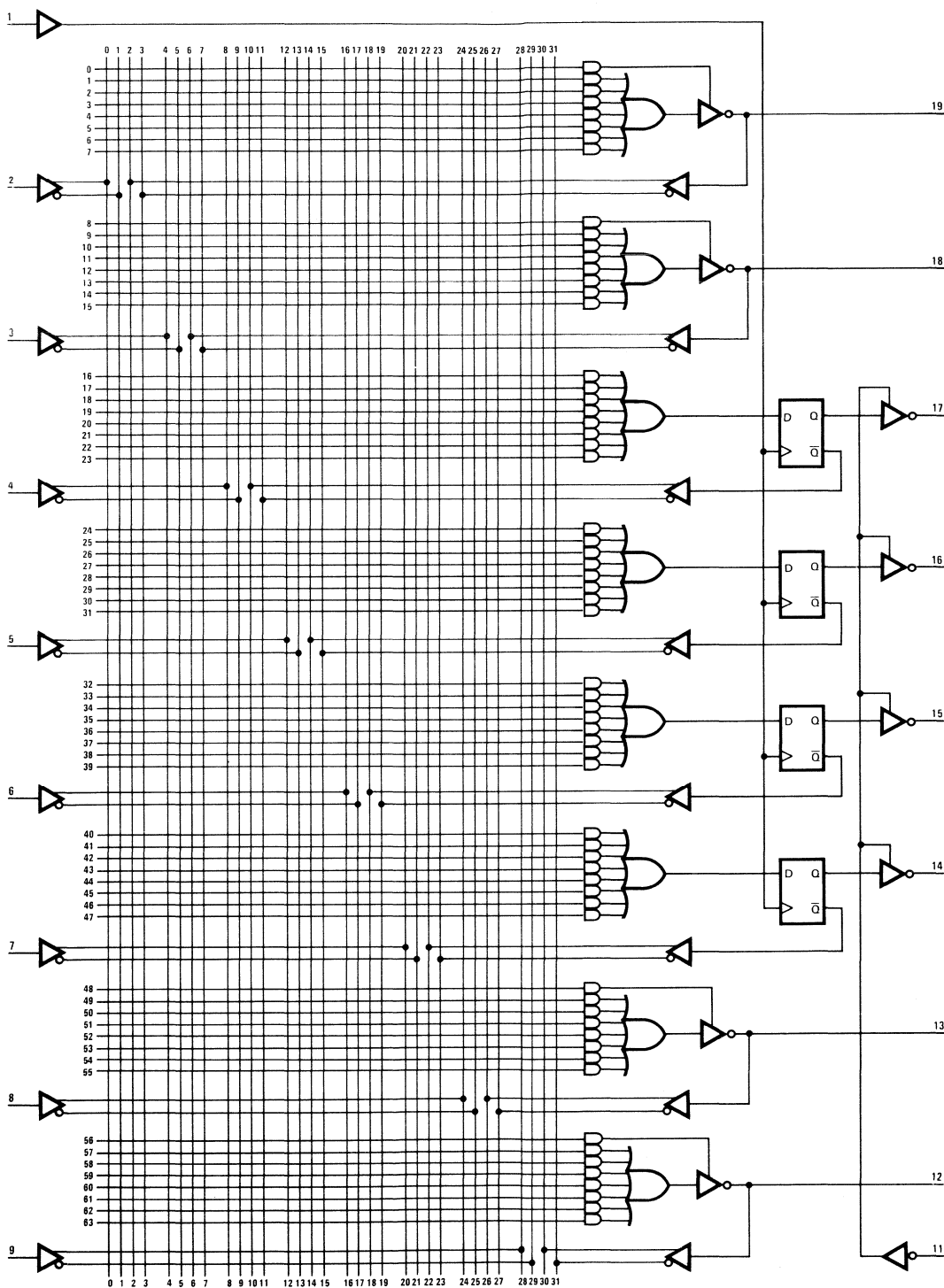
Logic Diagram PAL16R8



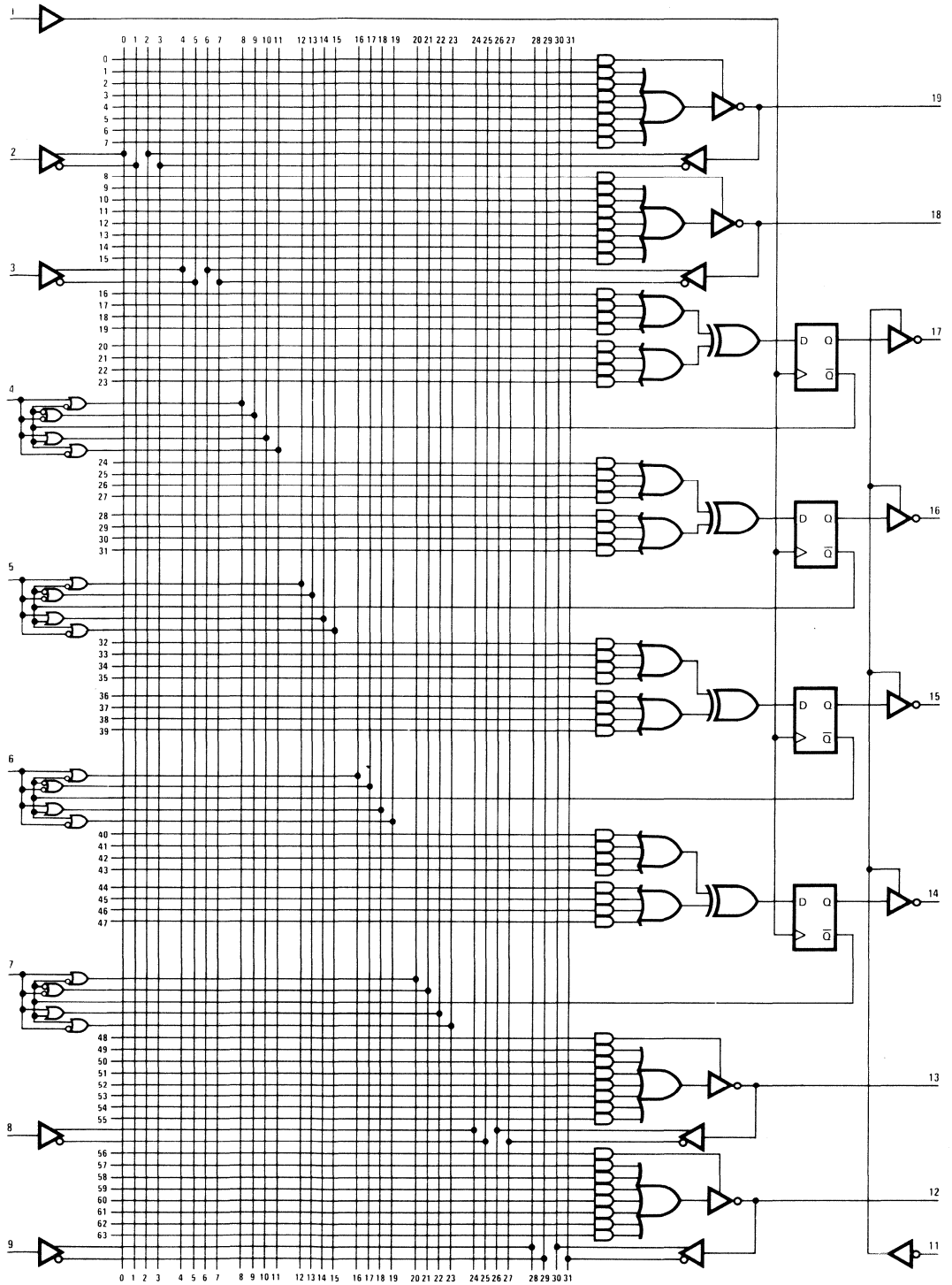
Logic Diagram PAL16R6



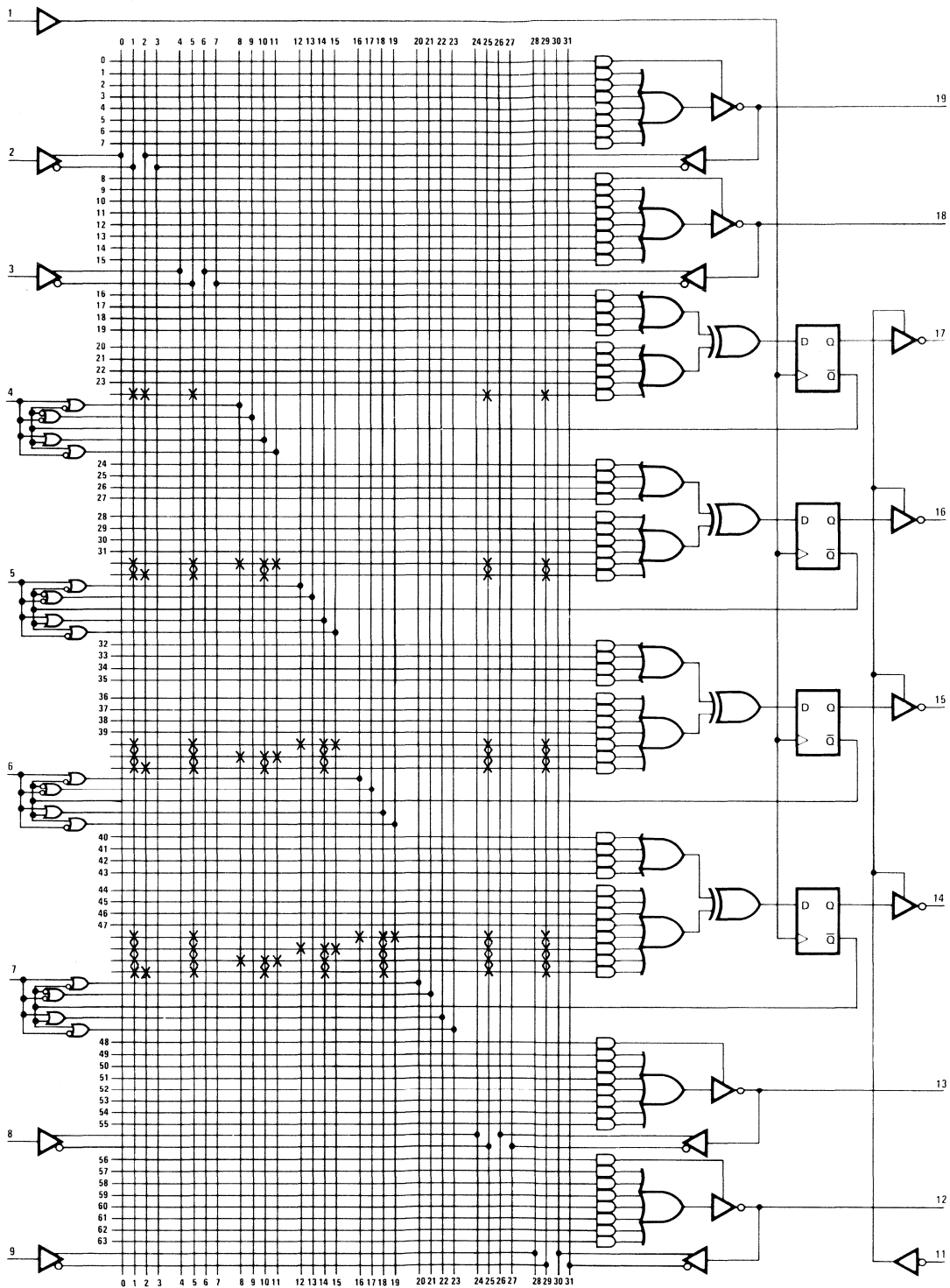
Logic Diagram PAL16R4



Logic Diagram PAL16X4



Logic Diagram PAL16A4



6

Ten Input, Quad 8 to 1 Programmable Multiplexer PMUX 29693

Features/Benefits

- Electrically programmable inputs
- Equivalent to four 74LS151, 8-to-1-line multiplexers
- Space saving 20 pin package
- Buffered TTL inputs
- Three-state, 16 mA outputs
- Compatible with standard PROM programmers
- Electrically programmable data routing
- FPLA replacement in many applications

Applications

- Data path encoding: sign extend, byte swap, shifts
- Programmable encoder: data bit selection
- Data and clock signal routing
- Instruction/Command register bit selection
- Status register control: input selection and output routing
- Microprogram multiply, divide, and shift control
- 2909/2911 Microprogram Sequencer control
- Data reformatting and format conversion
- PMUX + PROM = powerful encode/decode combination
- Programmable priority encoder with dynamic priority potential
- 2901 Bit Slice register select control
- Barrel shifters and byte/word selection operations
- I/O Line formatter for different I/O signals with same hardware
- Control signal selection by equipment operating mode
- Shift register feedback selection for CRCC generation, etc.

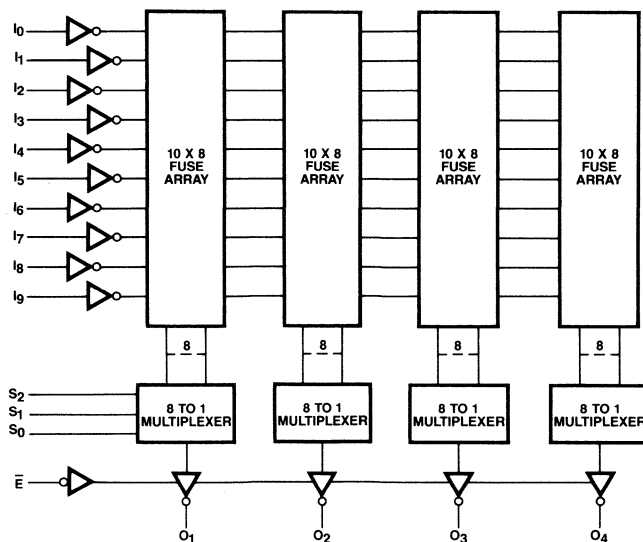
Description

The 29693 Ten Input Programmable Multiplexer (PMUX) contains four 8-line-to-1 line multiplexers with common Select and Enable lines, electrically programmable input selection, and three-state outputs. Each of the eight multiplexer inputs can be electrically connected to any of the 10 device inputs through a fusible link. The 29693 is shipped with each multiplexer input connected to all 10 device inputs through isolation diodes, resulting in a logical OR of the input signals. Undesired connections are removed by passing a short, high current pulse through the corresponding fusible link, changing it from a conductive to a non-conductive state. Nine of the 10 links on each multiplexer input will be opened in the typical case, except where the logical OR of two or more input signals is desired. Opening the fusible links is called programming, and links thus opened are termed programmed.

If all fusible links on a multiplexer input are programmed, the multiplexer output will always be low when that input is selected. If more than one link is left unprogrammed on a multiplexer input, the output will be the logical OR of the two corresponding input signals.

The 29693 is programmed by applying the desired multiplexer select code, taking the input to be disconnected to a TTL high with all other inputs low, and applying programming pulses on the Enable input and the multiplexer/device output. The 29693 is designed to be compatible with the programming pulses used on the 5300 (256 X 4) PROM. This allows the 29693 to be programmed by a standard PROM programmer with a simple adapter (see Figure 2).

Block Diagram



Absolute Maximum Ratings

Storage temperature -65 to +150°C
 Temperature (ambient) under bias -55 to +125°C
 Supply voltage to ground potential
 (Pin 20 to Pin 10) continuous -0.5V to +7V
 DC voltage applied to outputs
 (except during programming) -0.5V to +V_{CC} max.

DC input voltage (address inputs and I pins) .. -0.5V to +5.5V
 DC voltage applied to outputs during
 programming 26V
 Output current into outputs during programming 125 mA
 DC input voltage (chip select input—pin 15) .. -0.5V to +33V
 DC input current -30 mA to +5 mA

Operating Range

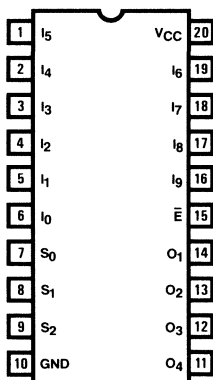
29693XC	T _A = 0 to +75°C	V _{CC} = 5.0V ±5%	Commercial	29693XM	T _A = -55 to +125°C	V _{CC} = 5.0V ±10%	Military
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Electrical Characteristics Over Operating Range (Unless otherwise noted)

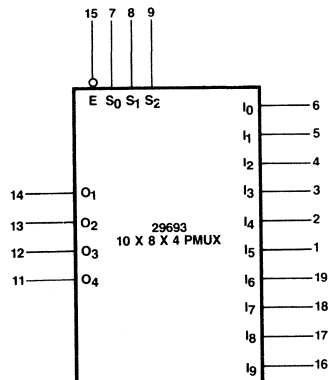
SYMBOL	DESCRIPTION	TEST CONDITIONS	MIN	TYP ¹	MAX	UNITS
V _{OH}	Output HIGH voltage	V _{CC} = MIN, I _{OH} = -2.0 mA V _{IN} = V _{IH} or V _{IL}	2.4			Volts
V _{OL}	Output LOW voltage	V _{CC} = MIN I _{OL} = 8 mA			0.4	Volts
		V _{IN} = V _{IH} or V _{IL} I _{OL} = 16 mA			0.5	Volts
V _{IH}	Input HIGH level	Guaranteed input logical HIGH voltage	2.0			Volts
V _{IL}	Input LOW level	Guaranteed input logical LOW voltage			0.8	Volts
I _{IL} (S, E)	Input LOW current	V _{CC} = MAX, V _{IN} = 0.4V		-60	-250	μA
I _{IL} (I ₀ -I ₉)	Input LOW current	V _{CC} = MAX, V _{IN} = 0.4V		-400	-700	μA
I _{IH}	Input HIGH current	V _{CC} = MAX, V _{IN} = 2.7V			10	μA
		V _{CC} = MAX, V _{IN} = 5.5V ³			1.0	mA
I _{SC}	Output short circuit current	V _{CC} = MAX, V _{OUT} = 0.0V	-12	-35	-85	mA
I _{CC}	Power supply current	All inputs = 2.7V, V _{CC} = MAX		100	140	mA
V _I	Input clamp voltage	V _{CC} = MIN, I _{IN} = 18 mA			-1.5	V
I _C EX	Output leakage current	V _{CC} = MAX V _E = 2.4V	V _O = 4.5V		100	μA
			V _O = 2.4V		40	μA
			V _O = 0.4V		-40	μA

- Notes: 1. Typical limits are V_{CC} = 5.0V and T_A = 25°C.
 2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
 3. Except V_{IN} = 4.5V at pin 15.

Pin Configuration



Logic Symbol



Switching Characteristics Over Operating Range

SYMBOL	DESCRIPTION	TEST CONDITIONS	TYP.	MAX			UNITS
			5V 25°C	25°C	COM'L	MIL	
t _{SA}	Select access time	C _L = 30 pF R _L = 300Ω to V _{CC} and 600Ω to GND (16 mA Load) ¹	35	50	55	75	ns
t _{IA}	Input data access time		35	50	55	75	ns
t _{EA}	Enable access time		20	25	30	40	ns
t _{ER}	Enable recovery time		15	20	25	30	ns

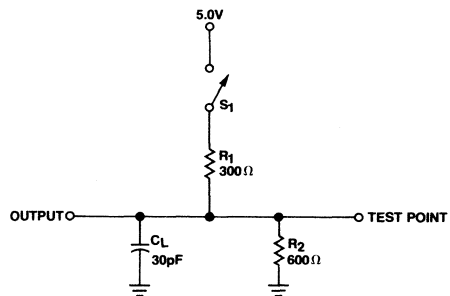
Note 1. 300Ω resistor opened for t_{EA} and t_{ER} measurements between HIGH and OFF states.

Ordering Information

Part Number	Package Type	Output	Temperature Range
29693DC	Hermetic DIP	TS	0 to +75°C
29693DM	Hermetic DIP	TS	-55 to +125°C
29693FM	Hermetic Flat Pack	TS	-55 to +125°C

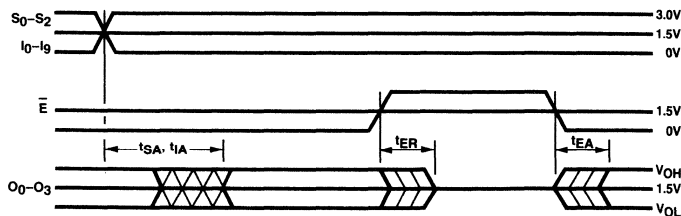
Note: For 883B processing, add the letter "B" to the order number suffix, e.g., 29693DMB.

AC Test Circuit



6

Switching Waveforms



Key to Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
[Solid line]	MUST BE STEADY	WILL BE STEADY
[Diagonal lines /]	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
[Diagonal lines \]	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
[Cross-hatch]	DON'T CARE: ANY CHANGE PERMITTED	CHANGING. STATE UNKNOWN
[Hatched /]	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF"-STATE

Note: Level on output while \bar{E} is HIGH is determined externally.

Programming Instructions

Device Description

The 29693 is manufactured with all device inputs connected to all data multiplexer inputs. To select a particular pattern of inputs to be connected to the data multiplexers, nichrome fusible links must be changed from a low to a high resistance for all undesired connections. This procedure is called programming.

There are 320 fusible links on the chip. Since each data multiplexer input is initially connected to all input buffers, all undesired links must be programmed and the desired connections left unprogrammed. Thus, 9 of the 10 fuses on each data multiplexer input and 288 of the 320 fuses for the device will be programmed in the typical case of one device input connected to each of the data multiplexer inputs. The PMUX can be programmed by a standard P/ROM programmer with an adaptor card as shown in Figure 2. The adaptor card allows the PMUX to be programmed by any P/ROM programmer that will program the 5300, 256 X 4 P/ROM. PMUX programming equipment can also be obtained from Data I/O, Inc. and other manufacturers of P/ROM programming equipment.

Programming Description

To select a particular link for programming, one of the input lines, I_0 - I_9 , has a TTL high applied with the remaining inputs left low, and the desired Select address applied to Select lines, S_2 - S_0 . With a V_{CC} of 5.50 volts applied or left applied, the program pin (Enable, \bar{E}) and the output to be programmed are taken to an elevated voltage to supply the required current to

program the fuse. Only one input and one output may be activated at any one time, since the internal programming circuitry is capable of sinking only one unit of programming current.

P/ROM Programming Adaptor

The PMUX can be programmed using a standard P/ROM programmer capable of programming the 5300, 256 X 4 P/ROM by using the adaptor card shown in Figure 2. This adaptor card converts the address signals from the P/ROM programmer into signals for the Select and Input lines at the PMUX. The five most significant bits of the P/ROM address are used to drive a decoder which selects one of the PMUX Input lines. The three least significant P/ROM bits are used to drive the PMUX Select lines. The output structure used for the PMUX is similar to that of the 5300 P/ROM and the adaptor unit allows each PMUX fuse to be identified for programming in the same manner as P/ROM fuses.

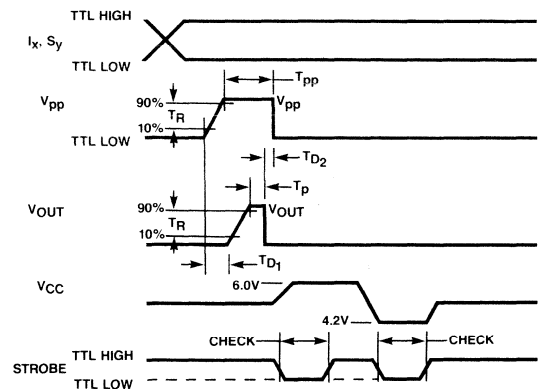
Fuses to be programmed are identified by a unique P/ROM address and one of the four PMUX outputs. The P/ROM address selects one of the I_0 - I_9 inputs and one of the eight multiplexer Select groups. The PMUX output identifies which of the four fuses selected by this code will be programmed. The address map given below defines the relationship between PMUX fuses and their corresponding P/ROM adaptor addresses. Note that addresses 80-255, etc., are not used. These addresses will show as programmed low when examined, since there is no input active to cause the outputs to go high. These addresses must be shown as programmed low on P/ROM programming tapes for correct verification.

29693 PMUX Programming Adaptor Address Map

MULTIPLEXER SELECT	INPUTS										UNUSED (LOW)
	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	
0	0	8	16	24	32	40	48	56	64	72	80-255
1	1	9	17	25	33	41	49	57	65	73	
2	2	10	18	26	34	42	50	58	66	74	
3	3	11	19	27	35	43	51	59	67	75	
4	4	12	20	28	36	44	52	60	68	76	
5	5	13	21	29	37	45	53	61	69	77	
6	6	14	22	30	38	46	54	62	70	78	
7	7	15	23	31	39	47	55	63	71	79	

Timing

The programming procedure involves the use of the program pin (Enable) and the output pin. In order to guarantee that the output transistor is off before increasing the voltage on the output pin, the program pin's voltage pulse must come before the output pin's programming pulse and leave after the output pin's programming pulse. A 100 ns delay is adequate. The programming pulse applied to the output pin and program pin must have a 50 to 70 microsecond rise time. See Figure 1.



NOTE: Output Load = 0.2 mA during 6.0V check
 Output Load = 12 mA during 4.2V check

T_R 0.4 V/ μ s \pm 15%
 T_{pp} 95 \pm 15 μ s
 T_p 1 μ s min., 8 μ s max.
 T_{D1} 80 \pm 10 μ s
 T_{D2} 100 ns min.

Figure 1. Program Timing

Verification

After programming a device, it can be checked for a low output by taking the Enable low. Since we must guarantee operation at minimum and maximum V_{CC} , current and temperature, the device must be required to sink 12 mA at 4.20V V_{CC} and 0.2 mA at 6.0V V_{CC} at room temperature.

Programming Speed

Typically fuses will blow on the rise time of the pulse. In automated programmers which must copy devices in a short time because of production requirements, the following pulse and voltage sequences have been found to maximize reliability, programming yield, and thruput. The device should be verified after each programming attempt and is advanced to the next bit after the fuse has been programmed.

PULSE NUMBER	PROGRAM PIN VOLTAGE	OUTPUT VOLTAGE
1 to 3	27V	20V
4 to 6	30V	23V
7 to 9	33V	26V

Truth Tables

MMI can program devices at our facility from MMI truth table forms (available on request). For customers desiring to make their own forms, an example is shown below:

WORD NUMBER	PIN \rightarrow	OUTPUTS			
		11 O ₄	12 O ₃	13 O ₂	14 O ₁
0		H	H	H	L
1		L	H	L	H
.	
.	
255		L	H	H	H

Note: A high voltage on the data out lines is signified by an "H." A low voltage on the data out lines is signified by an "L." The word number assumes positive logic on the address pins, so for example, word 255 = HHHHHHHH.

Commercial Programmers

The MMI PMUX is designed and tested to give a programming yield greater than 95%. Field reports agree with this expectation. Several companies make commercial programmers which will properly program the MMI PMUX. MMI makes it a practice to review these commercial programmers and works closely with the manufacturers to maintain a high programming yield and high reliability of programmed parts. MMI publishes a list of the approved programmers and recommends that MMI PMUX be programmed using one from the list.

For those customers not using an approved programmer, the programming instructions given elsewhere must be followed.

Approved PMUX Programmers

The 29693 PMUX may be programmed by any data I/O programmer using program card set 909-1226-1 and socket adapter 715-1396.

Programmable Multiplexer Construction and Operation

The internal construction of the 29693 Programmable Multiplexer is shown in the block diagram of Figure 3. Four 8-line-to-1-line multiplexers, similar to 74LS151's, with bused Select lines are shown. The inputs to these multiplexers are fed by a diode-and-fuse array, and the multiplexer outputs are connected to the inputs of the four inverting three-state output buffers.

The fuse-and-diode array is driven by 10 inverting input buffers. The fuse-and-diode array is driven by 10 inverting input buffers. If any input is driven high, its corresponding buffer output goes low. Any diodes connected to this buffer line are also driven low. The diodes are arranged such that taking one diode low on a given multiplexer input line will force that multiplexer input line

low. If that multiplexer input is selected, the multiplexer output will be low and its corresponding three-state buffer output will be high. The inversion in the three-state buffers compensates for the inversion in the input buffers.

Each multiplexer input has a pull-up resistor to V_{CC} . The diode-and-fuse elements in combination with this pull-up resistor form a logical OR function; any buffer output connected to an intact diode-and-fuse element will cause the corresponding multiplexer input line to go low and the multiplexer three-state buffer output to go high. If two buffer outputs are connected to a multiplexer input through intact diode-and-fuse combinations, taking either buffer input high will cause the corresponding three-state buffer to go high.

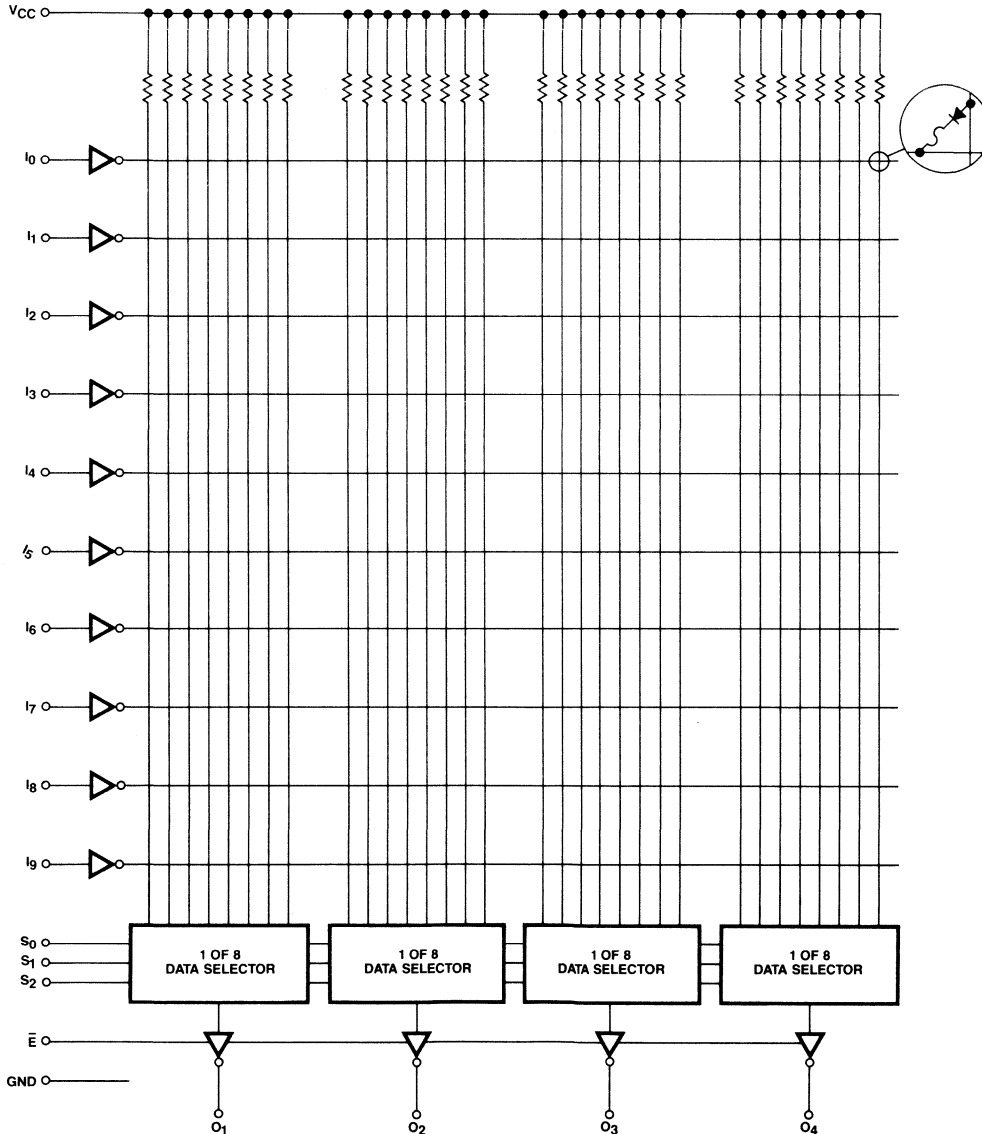
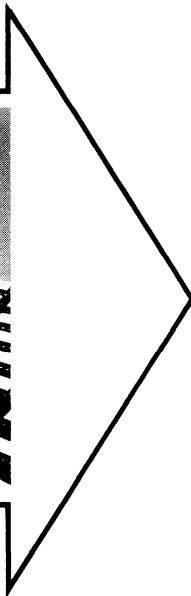
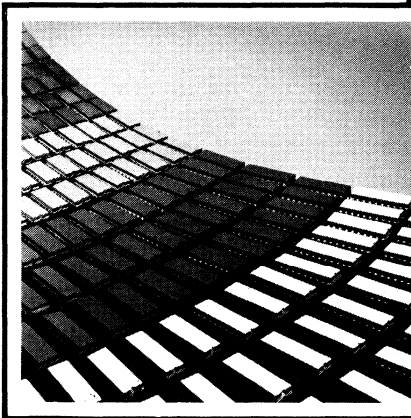


Figure 3. 29693 Programmable Multiplexer, Functional Diagram



Introduction	1
PROMS	2
ROMS	3
Character Generators	4
RAMS	5
Programmable Logic	6
LSI Logic	7
Arithmetic Elements	8
Interface	9
General Information	10
Representatives/Distributors	11

2900 Family Interchangeability and Selection Guide

CATEGORY	DESCRIPTION		AMD PART NUMBER	MMI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGN	PAGE
Arithmetic	4-Bit slice		Am2901A	2901A	2901A	7-7
	carry-look-ahead		Am2902		74S182 [†]	†
Sequencing	28 Pin sequencer slice		Am2909	2909	2909	7-35
	20 Pin sequencer slice		Am2911	2911	2911	7-35
	12-Bit sequencer		Am2910	2910	2910	†
	16-Way branch controller		Am29803		6301 ²	2-6
	Next address controller		Am29811		6331 ²	2-6
Memories	PROMs	32x8	Am29750/A/1A	6330/1	6330/1	2-6
		256x4	Am29760A/1A	6300/1	6300/1	2-6
		512x4	Am29770/1	6305/6	6305/6	2-6
		512x8 (registered)	Am29774/5		63RA483	2-30
	RAM	16x4 noninverting	Am29700/1	29700/1	29700/1	5-15
		16x4 inverting	Am29702/3	29702/3	29702/3	5-21
		256x1	Am29720/1	6560/1	6560/1	5-4
Miscellaneous	1 of 8 decoder w/3-state outputs		Am2921		PAL 16L8	3-2
Logic	8 input mux w/register		Am2922		PAL 16R4	3-2
Interface	quad-xceiver driver OC/TS	2 input driver, 3-state rcvr	Am2905/15	2905/15	2905/15	7-17/43
		2 input driver, rcvr parity	Am2906/16	2906/16	2906/16	7-23/49
		3-state receiver, rcvr parity	Am2907/17	2907/17	2907/17	7-29/55
	quad-d register	w/std. & 3-state outputs	Am2918/LS18	2918/LS18	2918/LS18	7-61/65
		w/dual 3-state outputs	Am2919	2919	2919	7-69

NOTES: 1. The 74S182 has the same pin-out as the 2902, but the 74S182 is faster
 2. The 29803/11 are pre-programmed PROMs.

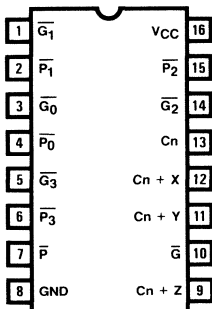
[†]Data Sheet will appear in a future edition of the LSI Data Book. Contact Application Department for additional information.

Comment: MMI philosophy is to retain the original numbers of PROMs rather than renumbering them with 2900 prefix. For the large variety of ROMs, PROMs and registered PROMs see Sections 2 and 3 in this data book.

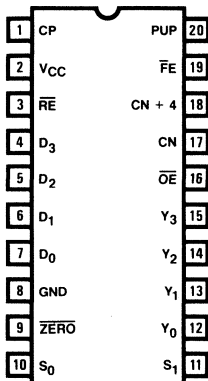


2900 Family Logic Element Pin-out

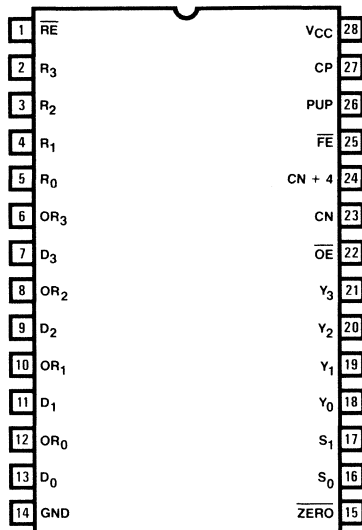
**2902
74S182**



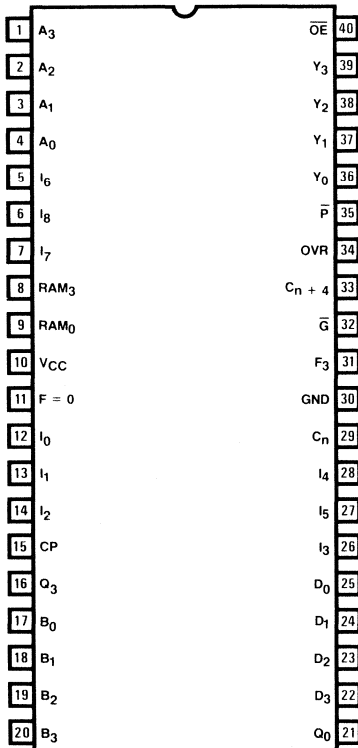
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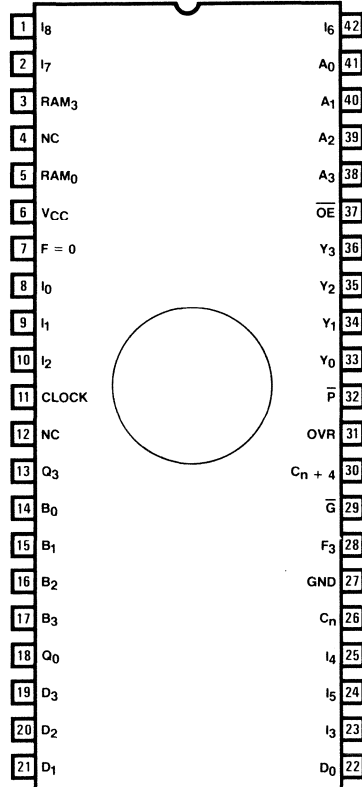
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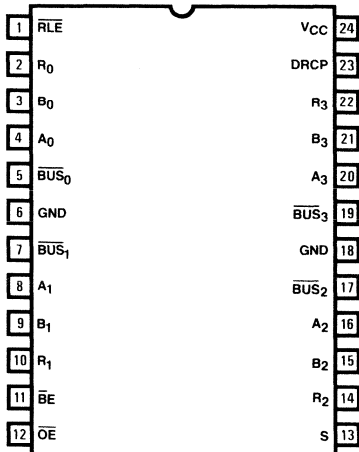
**2901A
DIP**



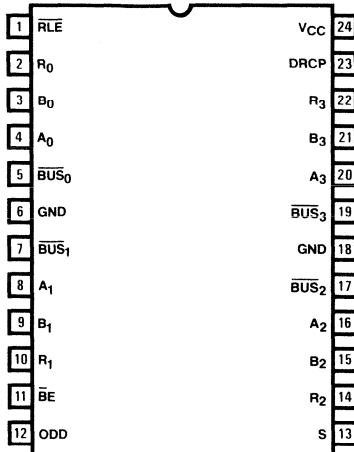
**2901A
Flat-Pack**



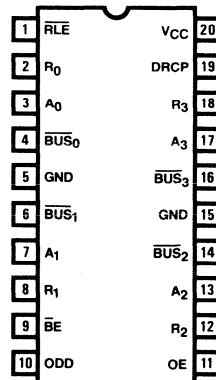
2905/15



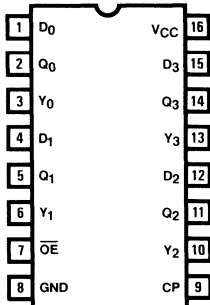
2906/16



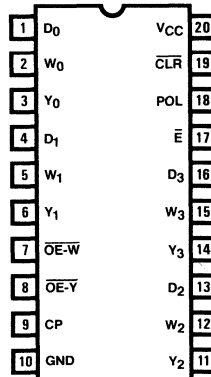
2907/17



2918/LS18



2919



Four-Bit Bipolar Microprocessor Slice 2901A

PRELIMINARY DATA

Features/Benefits

- **Two-address architecture—**
Independent simultaneous access to two working registers saves machine cycles.
- **Eight-function ALU—**
Performs addition, two subtraction operations, and five logic functions on two source operands.
- **Flexible data source selection—**
ALU data is selected from five source ports for a total of 203 source operand pairs for every ALU function.
- **Left/right shift independent of ALU—**
Add and shift operations take only one cycle.
- **Four status flags—**
Carry, overflow, zero, and negative.
- **Expandable—**
Connect any number of 2901A's together for longer word lengths.
- **Microprogrammable—**
Three groups of three bits each for source operand, ALU function, and destination control.

Description

The four-bit bipolar microprocessor slice is designed as a high-speed cascadable element intended for use in CPU's, peripheral controllers, programmable microprocessors and numerous other applications. The microinstruction flexibility of the 2901A will allow efficient emulation of almost any digital computing machine.

The device, as shown in the block diagram below, consists of a 16-word by 4-bit two-port RAM, a high-speed ALU, and the associated shifting, decoding and multiplexing circuitry. The nine-bit microinstruction word is organized into three groups of three bits each and selects the ALU source operands, the ALU function, and the ALU destination register. The microprocessor is cascadable with full look-ahead or with ripple carry, has three-state outputs, and provides various status flag outputs from the ALU. Advanced low-power Schottky processing is used to fabricate this 40-lead LSI chip. The 2901A is a plug in replacement for the 2901.

Architecture

A detailed block diagram of the bipolar microprogrammable microprocessor structure is shown in Figure 2. The circuit is a four-bit slice cascadable to any number of bits. Therefore, all data paths within the circuit are four bits wide. The two key elements in the Figure 2 block diagram are the 16-word by 4-bit 2-port RAM and the high-speed ALU.

PART NUMBER	PACKAGE	TEMPERATURE RANGE
2901ANC	N40	0°C to +70°C
2901AJC	J40	0°C to +70°C
2901AJM	J40	-55°C to +125°C
2901AFM	F42	-55°C to +125°C

Block Diagram

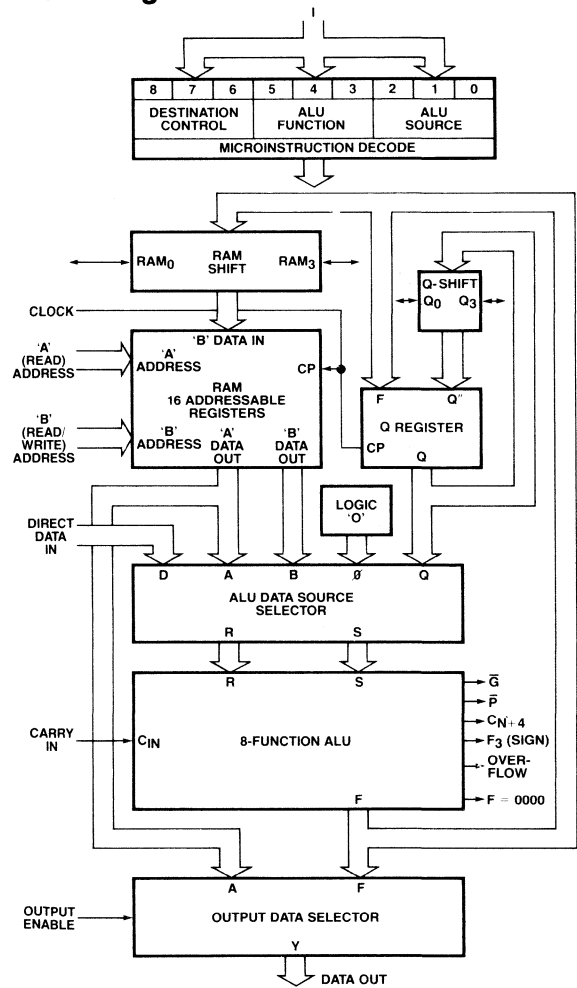


Figure 1. Microprocessor Slice Block Diagram



Data in any of the 16 words of the Random Access Memory (RAM) can be read from the A-port of the RAM as controlled by the 4-bit A address field input. Likewise, data in any of the 16 words of the RAM as defined by the B address field input can be simultaneously read from the B-port of the RAM. The same code can be applied to the A select field and B select field in which case the identical file data will appear at both the RAM A-port and B-port outputs simultaneously.

When enabled by the RAM write enable (RAM EN), new data is always written into the file (word) defined by the B address field of the RAM. The RAM data input field is driven by a 3-input multiplexer. This configuration is used to shift the ALU output data (F) if desired. This three-input multiplexer scheme allows the data to be shifted up one bit position, shifted down one bit position, or not shifted in either direction.

The RAM A-port data outputs and RAM B-port data outputs drive separate 4-bit latches. These latches hold the RAM data while the clock input is LOW. This eliminates any possible race conditions that could occur while new data is being written into the RAM.

The high-speed Arithmetic Logic Unit (ALU) can perform three binary arithmetic and five logic operations on the two 4-bit input words R and S. The R input field is driven from a 2-input multiplexer, while the S input field is driven from a 3-input multiplexer. Both multiplexers also have an inhibit capability; that is, no data is passed. This is equivalent to a "zero" source operand.

Referring to Figure 2, the ALU R-input multiplexer has the RAM A-port and the direct data inputs (D) connected as inputs. Likewise, the ALU S-input multiplexer has the RAM A-port, the RAM B-port and the Q register connected as inputs.

This multiplexer scheme gives the capability of selecting various pairs of the A, B, D, Q and "0" inputs as source operands to the ALU. These five inputs, when taken two at a time, result in ten possible combinations of source operand pairs. These combinations include AB, AD, AQ, A0, BD, BQ, B0, DQ, D0 and Q0. It is apparent that AD, AQ and A0 are somewhat redundant with BD, BQ and B0 in that if the A address and B address are the same, the identical function results. Thus, there are only seven completely non-redundant source operand pairs for the ALU. The 2901A microprocessor implements eight of these pairs. The microinstruction inputs used to select the ALU source operands are the I_0 , I_1 , and I_2 inputs. The definition of I_0 , I_1 , and I_2 for the eight source operand combinations are as shown in Table 1. Also shown is the octal code for each selection.

The two source operands not fully described as yet are the D input and Q input. The D input is the four-bit wide direct data field input. This port is used to insert all data into the working registers inside the device. Likewise, this input can be used in the ALU to modify any of the internal data files. The Q register is a separate 4-bit file intended primarily for multiplication and division routines but it can also be used as an accumulator or holding register for some applications.

The ALU itself is a high-speed arithmetic/logic operator capable of performing three binary arithmetic and five logic functions. The I_3 , I_4 , and I_5 microinstruction inputs are used to select the ALU function. The definition of these inputs is shown in Table 2. The octal code is also shown for reference. The normal technique for cascading the ALU of several devices is in a look-ahead carry mode. Carry generate, \bar{G} , and carry propagate, \bar{P} , are

outputs of the device for use with a carry-look-ahead-generator such as the 2902 ('182). A carry-out, C_{n+4} , is also generated and is available as an output for use as the carry flag in a status register. Both carry-in (C_n) and carry-out (C_{n+4}) are active HIGH.

The ALU has three other status-oriented outputs. These are F_3 , $F = 0$, and overflow (OVR). The F_3 output is the most significant (sign) bit of the ALU and can be used to determine positive or negative results without enabling the three-state data outputs. F_3 is non-inverted with respect to the sign bit output Y_3 . The $F = 0$ output is used for zero detect. It is an open-collector output and can be wire OR'ed between microprocessor slices. $F = 0$ is HIGH when all F outputs are LOW. The overflow output (OVR) is used to flag arithmetic operations that exceed the available two's complement number range. The overflow output (OVR) is HIGH when overflow exists. That is, when C_{n+3} and C_{n+4} are not the same polarity.

The ALU data output is routed to several destinations. It can be a data output of the device and it can also be stored in the RAM or the Q register. Eight possible combinations of ALU destination functions are available as defined by the I_6 , I_7 , and I_8 microinstruction inputs. These combinations are shown in Table 3.

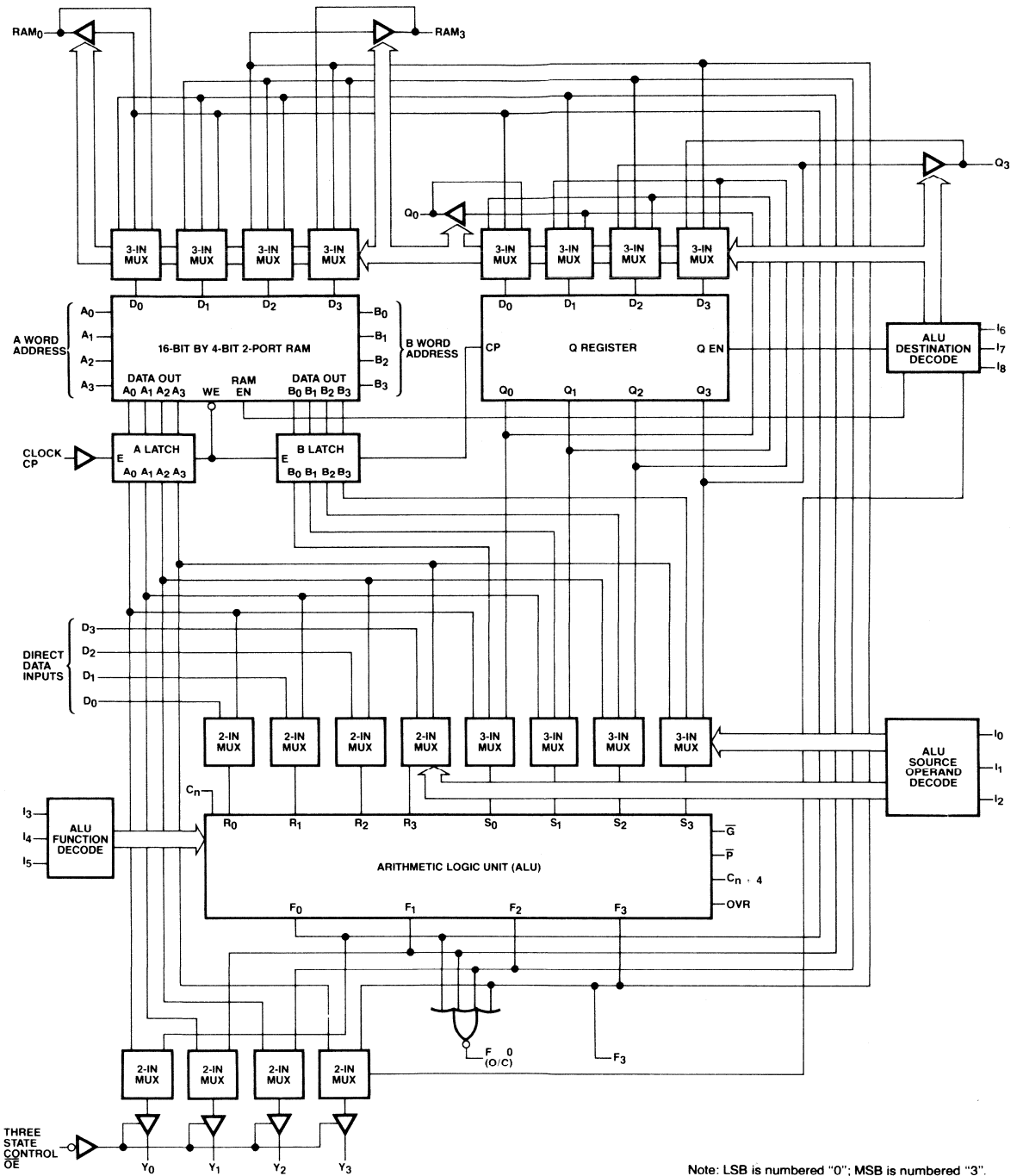
The four-bit data output field (Y) features three-state outputs and can be directly bus organized. An output control (\bar{OE}) is used to enable the three-state outputs. When \bar{OE} is HIGH, the Y outputs are in the high-impedance state.

A two-input multiplexer is also used at the data output such that either the A-port of the RAM or the ALU outputs (F) are selected at the device Y outputs. This selection is controlled by the I_6 , I_7 , and I_8 microinstruction inputs. Refer to Table 3 for the selected output for each microinstruction code combination.

As was discussed previously, the RAM inputs are driven from a three-input multiplexer. This allows the ALU outputs to be entered non-shifted, shifted up one position ($\times 2$) or shifted down one position ($\div 2$). The shifter has two ports; one is labeled RAM_0 and the other is labeled RAM_3 . Both of these ports consist of a buffer-driver with a three-state output and an input to the multiplexer. Thus, in the shift up mode, the RAM_3 buffer is enabled and the RAM_0 multiplexer input is enabled. Likewise, in the shift down mode, the RAM_0 buffer and RAM_3 input are enabled. In the no-shift mode, both buffers are in the high-impedance state and the multiplexer inputs are not selected. This shifter is controlled from the I_6 , I_7 and I_8 microinstruction inputs as defined in Table 3.

Similarly, the Q register is driven from a 3-input multiplexer. In the no-shift mode, the multiplexer enters the ALU data into the Q register. In either the shift-up or shift-down mode, the multiplexer selects the Q register data appropriately shifted up or down. The Q shifter also has two ports; one is labeled Q_0 and the other is Q_3 . The operation of these two ports is similar to the RAM shifter and is also controlled from I_6 , I_7 , and I_8 as shown in Table 3.

The clock input to the 2901A controls the RAM, the Q register, and the A and B data latches. When enabled, data is clocked into the Q register on the LOW-to-HIGH transition of the clock. When the clock input is HIGH, the A and B latches are open and will pass whatever data is present at the RAM outputs. When the clock input is LOW, the latches are closed and will retain the last data entered. If the RAM-EN is enabled, new data will be written into the RAM file (word) defined by the B address filed when the clock input is LOW.



Note: LSB is numbered "0"; MSB is numbered "3".

Figure 2. Detailed 2901A Microprocessor Block Diagram

Absolute Maximum Ratings

Supply voltage, V_{CC}	-0.5V to +7.0V
Input voltage	-0.5V to +5.5V
Input current	-30 mA to +5 mA
Output current	30mA
Storage temperature range	-65°C to +150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	COMMERCIAL			MILITARY			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.75	5.0	5.25	V
T_A	Operating free air temperature				0	25	75	°C
T_C	Operating case temperature	-55	25	125				°C

Electrical Characteristics

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY		COMMERCIAL		UNIT	
			MIN	TYP ²	MAX	MIN		TYP ²
V_{OH}	Output HIGH voltage	$V_{CC} = \text{MIN}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -1.6\text{mA}$ Y_0, Y_1, Y_2, Y_3		2.4	2.4	V	
			$I_{OH} = -1.0\text{mA}, C_{n+4}$		2.4	2.4		
			$I_{OH} = -800\mu\text{A}, \text{OVR}, \bar{P}$		2.4	2.4		
			$I_{OH} = -600\mu\text{A}, F_3$		2.4	2.4		
			$I_{OH} = -600\mu\text{A}$ $\text{RAM}_{0,3}, Q_{0,3}$		2.4	2.4		
			$I_{OH} = -1.6\text{mA}, \bar{G}$		2.4	2.4		
I_{CEX}	Output leakage current for F = 0 output	$V_{CC} = \text{MIN}, V_{OH} = 5.5\text{V}$ $V_{IN} = V_{IH}$ or V_{IL}		250		250	μA	
V_{OL}	Output LOW voltage	$V_{CC} = \text{MIN}$ $V_{IN} = V_{IH}$ or V_{IL}	$Y_0, Y_1,$	$I_{OL} = 20\text{mA}$		0.5	V	
			Y_2, Y_3	$I_{OL} = 16\text{mA}$		0.5		
			$\bar{G}, F = 0$	$I_{OL} = 16\text{mA}$		0.5		
			C_{n+4}	$I_{OL} = 10\text{mA}$		0.5		
			OVR, \bar{P}	$I_{OL} = 8.0\text{mA}$		0.5		
			$F_3,$ $\text{RAM}_{0,3},$ $Q_{0,3}$	$I_{OL} = 6.0\text{mA}$		0.5		
V_{IH}	Input HIGH level	Guaranteed input logical HIGH voltage for all inputs ⁷		2.0		2.0	V	
V_{IL}	Input LOW level	Guaranteed input logical LOW voltage for all inputs ⁷		0.8		0.8	V	
V_I	Input clamp voltage	$V_{CC} = \text{MIN}, I_{IN} = -18\text{mA}$		-1.5		-1.5	V	
I_{IL}	Input LOW current	$V_{CC} = \text{MAX},$ $V_{IN} = 0.5$	Clock, \bar{OE}		-0.36		-0.36	mA
			A_0, A_1, A_2, A_3		-0.36		-0.36	
			B_0, B_1, B_2, B_3		-0.36		-0.36	
			D_0, D_1, D_2, D_3		-0.72		-0.72	
			I_0, I_1, I_2, I_6, I_8		-0.36		-0.36	
			I_3, I_4, I_5, I_7		-0.72		-0.72	
			$\text{RAM}_{0,3}, Q_{0,3}^4$		-0.8		-0.8	
			C_n		-3.6		-3.6	

Electrical Characteristics (cont.)

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY		COMMERCIAL		UNIT		
			MIN	TYP ²	MAX	MIN		TYP ²	MAX
I _{IH}	Input HIGH current	V _{CC} = MAX, V _{IN} = 2.7V	Clock, OE		20		20	μA	
			A ₀ ,A ₁ ,A ₂ ,A ₃		20		20		
			B ₀ ,B ₁ ,B ₂ ,B ₃		20		20		
			D ₀ ,D ₁ ,D ₂ ,D ₃		40		40		
			I ₀ ,I ₁ ,I ₂ ,I ₆ ,I ₈		20		20		
			I ₃ ,I ₄ ,I ₅ ,I ₇		40		40		
			RAM _{0,3} ,Q _{0,3} ⁴		100		100		
		C _n		200		200			
I _I	Input HIGH current	V _{CC} = MAX, V _{IN} = 5.5V			1.0		1.0	mA	
I _{OZH}	Off state (high impedance) output current	V _{CC} = MAX	Y ₀ ,Y ₁ ,	V _O = 2.4V	50		50	μA	
I _{OZL}			Y ₂ ,Y ₃	V _O = 0.5V		-50			-50
			RAM _{0,3}	V _O = 2.4V ⁴		100			100
		Q _{0,3}	V _O = 0.5V ⁴		-800		-800		
I _{OS}	Output short circuit current	V _{CC} = 5.75V, V _O = 0.5V	Y ₀ ,Y ₁ ,Y ₂ ,Y ₃ , \bar{G}		-30	-85	-30	-85	mA
			C _n +4		-30	-85	-30	-85	
			OVR, \bar{P}		-30	-85	-30	-85	
			F ₃		-30	-85	-30	-85	
			RAM _{0,3} ,Q _{0,3}		-30	-85	-30	-85	
I _{CC}	Power supply current	V _{CC} = MAX	T _A = 25°C		160	250	160	250	mA
			T _A = 0°C to +70°C	2901A	160	265	160	265	
			T _A = +70°C	NC, JC	160	220	160	220	
			T _C = -55°C to +125°C	2901A	160	280	160	280	
			T _C = +125°C	JM,FM	160	190	160	190	

- Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These are three-state outputs internally connected to TTL inputs. Input characteristics are measured with I₆₇₈ in a state such that the three-state output is OFF.
5. "MIL" = 2901ADM, FM. "COM'L" = 2901A NC, JC.
6. Worst case I_{CC} is at minimum temperature.
7. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

Table 1. ALU Source Operand Control.

MICRO CODE				ALU SOURCE OPERANDS	
I ₂	I ₁	I ₀	OCTAL CODE	R	S
L	L	L	0	A	Q
L	L	H	1	A	B
L	H	L	2	O	Q
L	H	H	3	O	B
H	L	L	4	O	A
H	L	H	5	D	A
H	H	L	6	D	Q
H	H	H	7	D	O

Table 2. ALU Function Control.

MICRO CODE				ALU FUNCTION	SYMBOL
I ₅	I ₄	I ₃	OCTAL CODE		
L	L	L	0	R Plus S	R + S
L	L	H	1	S Minus R	S - R
L	H	L	2	R Minus S	R - S
L	H	H	3	R OR S	R ∨ S
H	L	L	4	R AND S	R ∧ S
H	L	H	5	\bar{R} AND S	$\bar{R} \wedge S$
H	H	L	6	R EX-OR S	R ⊕ S
H	H	H	7	R EX-NOR S	$\overline{R \oplus S}$

Table 3. ALU Destination Control.

MICRO CODE				RAM FUNCTION		Q-REQ. FUNCTION		Y OUTPUT	RAM SHIFTER		Q SHIFTER	
I ₈	I ₇	I ₆	OCTAL CODE	SHIFT	LOAD	SHIFT	LOAD		RAM ₀	RAM ₃	Q ₀	Q ₃
L	L	L	0	X	NONE	NONE	F → Q	F	X	X	X	X
L	L	H	1	X	NONE	X	NONE	F	X	X	X	X
L	H	L	2	NONE	F → B	X	NONE	A	X	X	X	X
L	H	H	3	NONE	F → B	X	NONE	F	X	X	X	X
H	L	L	4	DOWN	F/2 → B	DOWN	Q/2 → Q	F	F ₀	IN ₃	Q ₀	IN ₃
H	L	H	5	DOWN	F/2 → B	X	NONE	F	F ₀	IN ₃	Q ₀	X
H	H	L	6	UP	2F → B	UP	2Q → Q	F	IN ₀	F ₃	IN ₀	Q ₃
H	H	H	7	UP	2F → B	X	NONE	F	IN ₀	F ₃	X	Q ₃

X = Don't care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the high impedance state.
 B = Register Addressed by B inputs.
 Up is toward MSLB, Down is toward LSB.

Table 4. Source Operand and ALU Function Matrix.

I ₅₄₃ OCTAL	I ₂₁₀ OCTAL	0	1	2	3	4	5	6	7
	ALU SOURCE / ALU FUNCTION	A, Q	A, B	O, Q	O, B	O, A	D, A	D, Q	D, O
0	C _n = L R Plus S	A+Q	A+B	Q	B	A	D+A	D+Q	D
	C _n = H	A+Q+1	A+B+1	Q+1	B+1	A+1	D+A+1	D+Q+1	D+1
1	C _n = L S Minus R	Q-A-1	B-A-1	Q-1	B-1	A-1	A-D-1	Q-D-1	-D-1
	C _n = H	Q-A	B-A	Q	B	A	A-D	Q-D	-D
2	C _n = L R Minus S	A-Q-1	A-B-1	-Q-1	-B-1	-A-1	D-A-1	D-Q-1	D-1
	C _n = H	A-Q	A-B	-Q	-B	-A	D-A	D-Q	D
3	R OR S	A ∨ Q	A ∨ B	Q	B	A	D ∨ A	D ∨ Q	D
4	R AND S	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5	\bar{R} AND S	$\bar{A} \wedge Q$	$\bar{A} \wedge B$	Q	B	A	$\bar{D} \wedge A$	$\bar{D} \wedge Q$	0
6	R EX-OR S	A ⊕ Q	A ⊕ B	Q	B	A	D ⊕ A	D ⊕ Q	D
7	R EX-NOR S	$A \nabla Q$	$A \nabla B$	\bar{Q}	\bar{B}	\bar{A}	$\bar{D} \nabla A$	$\bar{D} \nabla Q$	\bar{D}

+ = Plus; - = Minus; ∨ = OR; ∧ = AND; ⊕ = EX-OR

Source Operands and ALU Functions

There are eight source operand pairs available to the ALU as selected by the I_0 , I_1 , and I_2 instruction inputs. The ALU can perform eight functions; five logic and three arithmetic. The I_3 , I_4 , and I_5 instruction inputs control this function selection. The carry input, C_n , also affects the ALU results when in the arithmetic mode. The C_n input has no effect on the logic mode. When I_0 through I_5 and C_n are viewed together, the matrix of Table 4 results. This matrix fully defines the ALU/source operand function for each state.

Table 5. ALU Logic Mode Functions. (C_n Irrelevant)

OCTAL I_{543}, I_{210}	GROUP	FUNCTION
4 0	AND	$A \wedge Q$
4 1		$A \wedge B$
4 5		$D \wedge A$
4 6		$D \wedge Q$
3 0	OR	$A \vee Q$
3 1		$A \vee B$
3 5		$D \vee A$
3 6		$D \vee Q$
6 0	EX-OR	$A \nabla Q$
6 1		$A \nabla B$
6 5		$D \nabla A$
6 6		$D \nabla Q$
7 0	EX-NOR	$\overline{A \nabla Q}$
7 1		$\overline{A \nabla B}$
7 5		$\overline{D \nabla A}$
7 6		$\overline{D \nabla Q}$
7 2	INVERT	\overline{Q}
7 3		\overline{B}
7 4		\overline{A}
7 7		\overline{D}
6 2	PASS	Q
6 3		B
6 4		A
6 7		D
3 2	PASS	Q
3 3		B
3 4		A
3 7		D
4 2	"ZERO"	0
4 3		0
4 4		0
4 7		0
5 0	MASK	$\overline{A} \wedge Q$
5 1		$\overline{A} \wedge B$
5 5		$\overline{D} \wedge A$
5 6		$\overline{D} \wedge Q$

The ALU functions can also be examined on a "task" basis, i.e., add, subtract, AND, OR, etc. In the arithmetic mode the carry will affect the function performed, while in the logic mode the carry will have no bearing on the ALU output. Table 5 defines the various logic operations that the 2901A can perform and Table 6 shows the arithmetic functions of the device. Both carry-in LOW ($C_n = 0$) and carry-in HIGH ($C_n = 1$) are defined in these operations.

Table 6. ALU Arithmetic Mode Functions.

OCTAL I_{543}, I_{210}	$C_n = 0$ (LOW)		$C_n = 1$ (HIGH)	
	GROUP	FUNCTION	GROUP	FUNCTION
0 0	ADD	$A + Q$	ADD plus one	$A + Q + 1$
0 1		$A + B$		$A + B + 1$
0 5		$D + A$		$D + A + 1$
0 6		$D + Q$		$D + Q + 1$
0 2	PASS	Q	Increment	$Q + 1$
0 3		B		$B + 1$
0 4		A		$A + 1$
0 7		D		$D + 1$
1 2	Decrement	$Q - 1$	PASS	Q
1 3		$B - 1$		B
1 4		$A - 1$		A
2 7		$D - 1$		D
2 2	1's Comp.	$-Q - 1$	2's Comp. (Negate)	$-Q$
2 3		$-B - 1$		$-B$
2 4		$-A - 1$		$-A$
1 7		$-D - 1$		$-D$
1 0	Subtract (1's Comp)	$Q - A - 1$	Subtract (2's Comp)	$Q - A$
1 1		$B - A - 1$		$B - A$
1 5		$A - D - 1$		$A - D$
1 6		$Q - D - 1$		$Q - D$
2 0		$A - Q - 1$		$A - Q$
2 1		$A - B - 1$		$A - B$
2 5		$D - A - 1$		$D - A$
2 6		$D - Q - 1$		$D - Q$

Logic Functions For G, P, C_{n+4}, and OVR

The four signals G, P, C_{n+4}, and OVR are designed to indicate carry and overflow conditions when the 2901A is in the add or subtract mode. The table below indicates the logic equations for these four signals for each of the eight ALU functions. The R and S inputs are the two inputs selected according to Table 1.

Definitions (+ = OR)

$$\begin{aligned}
 P_0 &= R_0 + S_0 & G_0 &= R_0 S_0 \\
 P_1 &= R_1 + S_1 & G_1 &= R_1 S_1 \\
 P_2 &= R_2 + S_2 & G_2 &= R_2 S_2 \\
 P_3 &= R_3 + S_3 & G_3 &= R_3 S_3 \\
 C_4 &= G_3 + P_3 G_2 = P_3 P_2 G_1 = P_3 P_2 P_1 G_0 = P_3 P_2 P_1 P_0 C_n \\
 C_3 &= G_2 + P_2 G_1 + P_2 P_1 G_0 = P_2 P_1 P_0 C_n
 \end{aligned}$$

Table 7. Logic Equations for Generate, Propagate, Carry-out and Overflow.

I543	FUNCTION	\bar{P}	\bar{G}	C _{n+4}	OVR
0	R + S	$\overline{P_3 P_2 P_1 P_0}$	$G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0$	C ₄	$C_3 \vee C_4$
1	S - R	← Same as R + S equations, but substitute \bar{R}_i for R_i in definitions →			
2	R - S	← Same as R + S equations, but substitute \bar{S}_i for S_i in definitions →			
3	RVS	LOW	$P_3 P_2 P_1 P_0$	$\overline{P_3 P_2 P_1 P_0} + C_n$	$\overline{P_3 P_2 P_1 P_0} + C_n$
4	RAS	LOW	$\overline{G_3 + G_2 + G_1 + G_0}$	$G_3 + G_2 + G_1 + G_0 + C_n$	$G_3 + G_2 + G_1 + G_0 + C_n$
5	$\bar{R} \wedge S$	LOW	← Same as R ∧ S equations, but substitute \bar{R}_i for R_i in definitions →		
6	R ∨ S	← Same as $\bar{R} \vee \bar{S}$, but substitute \bar{R}_i for R_i in definitions →			
7	$\overline{R \vee S}$	$G_3 + G_2 + G_1 + G_0$	$G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0$	$\overline{G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 P_0 (G_0 + C_n)}$	See note

Note: $(\bar{P}_2 + \bar{G}_2 \bar{P}_1 + \bar{G}_2 \bar{G}_1 \bar{P}_0 + \bar{G}_2 \bar{G}_1 \bar{G}_0 C_n) \vee (P_3 + \bar{G}_3 \bar{P}_2 + \bar{G}_3 \bar{G}_2 \bar{P}_1 + \bar{G}_3 \bar{G}_2 \bar{G}_1 \bar{P}_0 + \bar{G}_3 \bar{G}_2 \bar{G}_1 \bar{G}_0 C_n)$ + = OR

Definition of Terms

A₀₋₃—The four address inputs to the register stack used to select one register whose contents are displayed through the A-port.

B₀₋₃—The four-address inputs to the register stack used to select one register whose contents are displayed through the B-port and into which new data can be written when the clock goes LOW.

I₀₋₈—The nine instruction control lines to the 2901A, used to determine what data sources will be applied to the ALU (I₀₁₂), what function the ALU will perform (I₃₄₅), and what data is to be deposited in the Q-register or the register stack (I₆₇₈).

Q₃, RAM₃—A shift line at the MSB of the Q register (Q₃) and the register stack (RAM₃). Electrically these lines are three-state outputs connected to TTL inputs internal to the 2901A. When the destination code on I₆₇₈ indicates an up shift (octal 6 or 7) the three-state outputs are enabled and the MSB of the Q register is available on the Q₃ pin and the MSB of the ALU output is available on the RAM₃ pin. Otherwise, the three-state outputs are OFF (high-impedance) and the pins are electrically LS-TTL inputs. When the destination code calls for a down shift, the pins are used as the data inputs to the MSB of the Q register (octal 4) and RAM (octal 4 or 5).

Q₀, RAM₀—Shift lines like Q₃ and RAM₃, but at the LSB of the Q-register and RAM. These pins are tied to the Q₃ and RAM₃ pins of the adjacent device to transfer data between devices for up and down shifts of the Q register and ALU data.

D₀₋₃—Direct data inputs. A four-bit data field which may be selected as one of the ALU data sources for entering data into the 2901A. D₀ is the LSB.

Y₀₋₃—The four data outputs of the 2901A. These are three-state output lines. When enabled, they display either the four outputs of the ALU or the data on the A-port of the register stack, as determined by the destination code I₆₇₈.

\overline{OE} —Output Enable. When \overline{OE} is HIGH, the Y outputs are OFF; when \overline{OE} is LOW, the Y outputs are active (HIGH or LOW).

\bar{P} , \bar{G} —The carry generate and propagate outputs of the 2901A's ALU. These signals are used with the 2902 for carry-lookahead.

OVR—Overflow. This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's complement operation has overflowed into the sign-bit.

F = 0—This is an open collector output which goes HIGH (OFF) if the data on the four ALU outputs F₀₋₃ are all LOW. In positive logic, it indicates the result of an ALU operation is zero.

C_n—The carry-in to the 2901A's ALU.

C_{n+4}—The carry-out of the 2901A's ALU.

CP—The clock to the 2901A. The Q register and register stack outputs change on the clock LOW-to-HIGH transition. The clock LOW time is internally the write enable to the 16 x 4 RAM which compromises the "master" latches of the register stack. While the clock is LOW, the "slave" latches on the RAM outputs are closed, storing the data previously on the RAM outputs. This allows synchronous master-slave operation of the register stack.

Guaranteed Operating Conditions Over Temperature and Voltage

Tables 8, 9 and 10 define the timing requirements of the 2901A in a system. The 2901A is guaranteed to function correctly over the operating range when used within the delay and set-up time constraints of these tables for the appropriate device type. The tables are divided into three types of parameters: clock characteristics, combinational delays from inputs to outputs, and set-up and hold time requirements. The later table defines the time prior to the end of the cycle (i.e., clock LOW-to-HIGH transition) at which each input must be stable to guarantee that the correct data is written into one of the internal registers.

Table 8. Cycle Time and Clock Characteristics

TIME	COMMERCIAL	MILITARY
Read-modify-write cycle (time from selection of A, B registers to end of cycle)	100 ns	110 ns
Maximum clock frequency to shift Q register (50% duty cycle) I = 432 or 632	15MHz	12MHz
Minimum clock LOW time	30ns	30ns
Minimum clock HIGH time	30ns	30ns
Minimum clock period	100ns	110ns

Table 9. Combinational Propagation Delay⁷


TO OUTPUT FROM INPUT	COMMERCIAL								MILITARY								UNIT
	Y	F ₃	C _{n+4}	\bar{G}, \bar{P}	F = 0 R _L = 270	OVR	SHIFT OUTPUTS		Y	F ₃	C _{n+4}	\bar{G}, \bar{P}	F = 0 R _L = 270	OVR	SHIFT OUTPUTS		
							RAM ₀ RAM ₃	Q ₀ Q ₃							RAM ₀ RAM ₃	Q ₀ Q ₃	
A, B	80	80	75	65	87	85	95	—	85	85	80	70	97	90	100	—	ns
D (arithmetic mode)	45	45	45	35	57	55	65	—	50	50	50	40	62	60	70	—	ns
D (I = X37) ⁵	40	40	—	—	52	—	60	—	45	45	—	—	57	—	65	—	ns
C _n	30	30	20	—	47	30	50	—	35	35	25	—	52	35	55	—	ns
I ₀₁₂	55	55	50	45	67	65	75	—	60	60	55	50	72	70	80	—	ns
I ₃₄₅	55	55	55	50	67	65	75	—	60	60	60	55	72	70	80	—	ns
I ₆₇₈	30	—	—	—	—	—	30	30	35	—	—	—	—	—	35	35	ns
OE Enable/ Disable	35/ 25	—	—	—	—	—	—	—	40/ 25	—	—	—	—	—	—	—	ns
A bypassing ALU (I = 2xx)	45	—	—	—	—	—	—	—	50	—	—	—	—	—	—	—	ns
Clock ⁶ 	60	60	60	50	72	70	80	30	65	65	65	55	82	75	85	35	ns



Table 10. Set-up and Hold Times¹

FROM INPUT	COMMERCIAL		MILITARY		UNIT
	SET-UP TIME	HOLD TIME	SET-UP TIME	HOLD TIME	
A, B _{2,4} Source ^{3,5}	100 t _{pwL} + 30	0	110 t _{pwL} + 30	0	ns
B dest. ^{2,4}	t _{pwL} + 15	0	t _{pwL} + 15	0	ns
D (arithmetic mode)	70	0	75	0	ns
D (I = X37) ⁵	60	0	65	0	ns
C _n	55	0	60	0	ns
I ₀₁₂	80	0	85	0	ns
I ₃₄₅	80	0	85	0	ns
I ₆₇₈	t _{pwL} + 30	0	t _{pwL} + 30	0	ns
RAM _{0,3} , Q _{0,3}	25	0	25	0	ns

For notes, see Figure 3.

Set-Up and Hold Times (minimum cycles from each input)

Set-up and hold times are defined relative to the clock LOW-to-HIGH edge. Inputs must be steady at all times from the set-up time prior to the clock until the hold time after the clock. The set-up times allow sufficient time to perform the correct operation on the correct data so that the proper ALU data can be written into one of the registers.

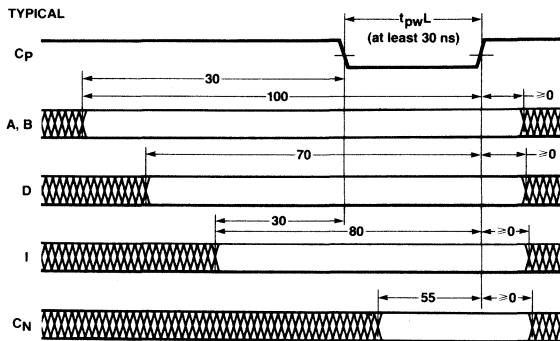
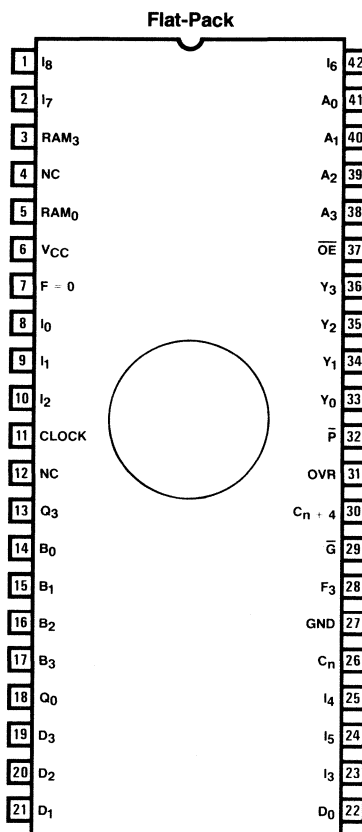
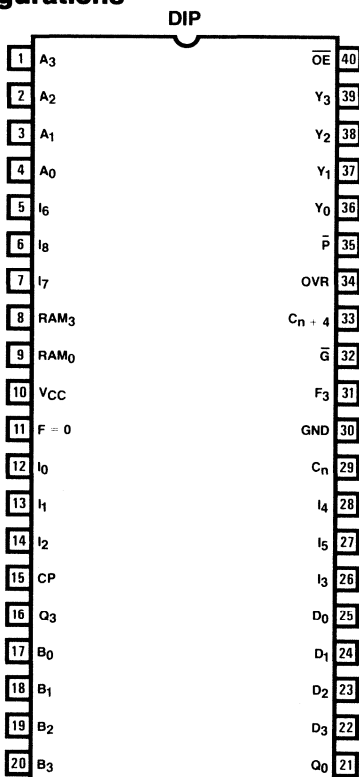


Figure 3. Minimum Cycle Times from Inputs. Numbers Shown are Minimum Data Stable Times for 2901ADC, in ns. See Table 10 for Detailed Information.

- Notes: 1. See Figure 3.
 2. If the B address is used as a source operand, allow for the "A, B source" set-up time; if it is used only for the destination address, use the "B Dest" set-up time.
 3. Where two numbers are shown, both must be met.
 4. "t_{pwL}" is the clock LOW time.
 5. D V 0 is the fastest way to load the RAM from the D inputs. This function is obtained with I = 337.
 6. Using Q register as source operand in arithmetic mode. Clock is not normally in critical speed path when Q is not a source.
 7. C_L = 50pF (except output disable tests).

Pin Configurations



Quad Two-Input OC Bus Transceiver With Three-State Receiver 2905

Features/Benefits

- Quad high-speed LSI bus-transceiver
- Open-collector bus driver
- Two-port input to D-type register on driver
- Bus driver output can sink 100 mA at 0.8V max.
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12 mA
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

Description

The 2905 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier outputs drive four D-type latches that feature three-state outputs.

This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The open-collector bus output can sink up to 100 mA at 0.8V maximum. The BUS input differential amplifier contains disconnect protection diodes such that the bus is fail-safe when power is not applied. The bus enable input

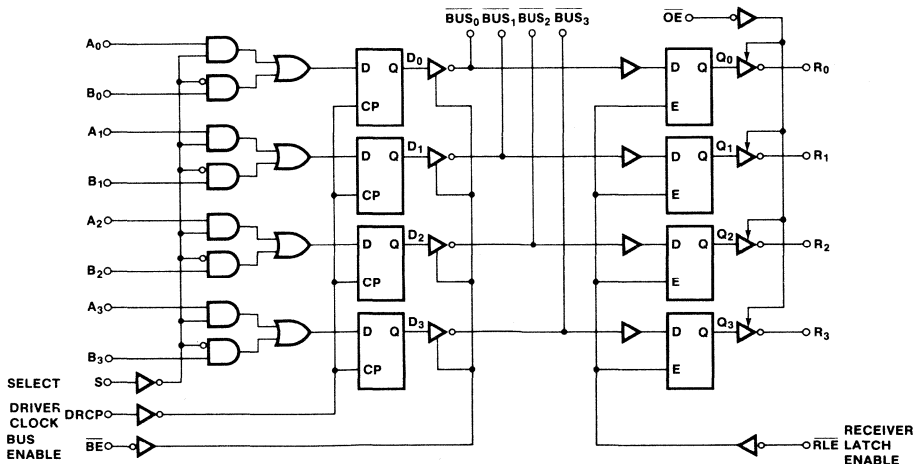
PART NUMBER	PACKAGE	TEMPERATURE RANGE
2905NC	N24	0°C to +70°C
2905JC	J24	0°C to +70°C
2905JM	J24	-55°C to +125°C
2905FM	F24	-55°C to +125°C

(\overline{BE}) is used to force the driver outputs to the high-impedance state. When \overline{BE} is HIGH, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B inputs is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable (\overline{RLE}) input. When the \overline{RLE} input is LOW, the latch is open and the

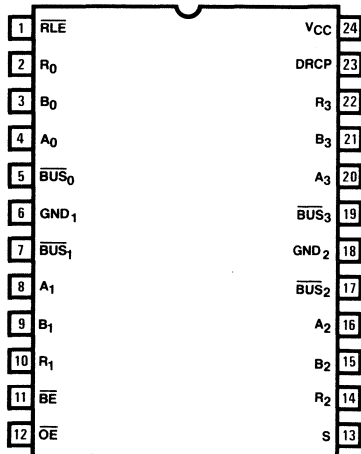
Logic Diagram



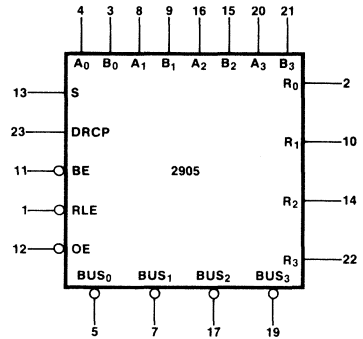
receiver outputs will follow the bus inputs (BUS data inverted and \overline{OE} LOW). When the \overline{RLE} input is HIGH, the latch will close and retain the present data regardless of the bus input. The four

latches have three-state outputs and are controlled by a buffered common three-state control (\overline{OE}) input. When \overline{OE} is HIGH, the receiver outputs are in the high impedance state.

Pin Configuration



Logic Symbol



VCC = Pin 24
 GND1 = Pin 6
 GND2 = Pin 18

Absolute Maximum Ratings

Storage temperature	-65°C to +150°C
Temperature (ambient) under bias	-55°C to +125°C
Supply voltage to ground potential	-0.5V to +7V
DC voltage applied to outputs for HIGH output state	-0.5V to +VCC max.
DC input voltage	-0.5V to +5.5V
DC output current, into outputs (except bus)	30mA
DC output current, into bus	200mA
DC input current	-30mA to +5.0mA

**Bus Input/Output Electrical Characteristics
 Over Recommended Operating Temperature Range**

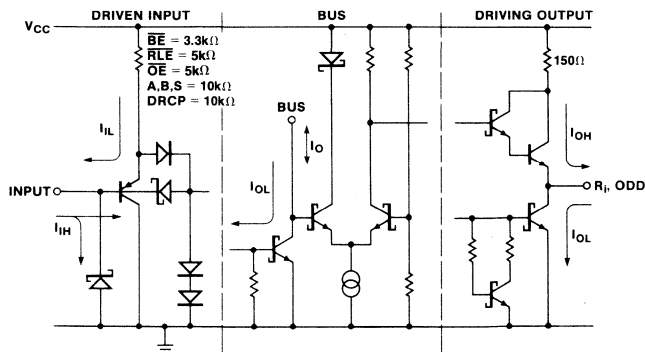
SYMBOL	PARAMETER	TEST CONDITIONS ¹	MILITARY T _A = -55°C to +125°C VCC MIN = 4.50V VCC MAX = 5.50V MIN TYP ² MAX		COMMERCIAL T _A = 0°C to +70°C VCC MIN = 4.75V VCC MAX = 5.25V MIN TYP ² MAX		UNIT	
V _{OL}	Bus output LOW voltage	VCC = MIN	I _{OL} = 40mA	0.32	0.5	0.32	0.5	V
			I _{OL} = 70mA	0.41	0.7	0.41	0.7	
			I _{OL} = 100mA	0.55	0.8	0.55	0.8	
I _O	Bus leakage current	VCC = MAX	V _O = 0.4V		-50		-50	μA
			V _O = 4.5V		200		100	
I _{OFF}	Bus leakage current (power OFF)	V _O = 4.5V		100		100	μA	
V _{TH}	Receiver input HIGH threshold	Bus enable = 2.4V	2.4	2.0		2.3	2.0	V
V _{TL}	Receiver input LOW threshold	Bus enable = 2.4V	2.0	1.5		2.0	1.6	V

Electrical Characteristics
Over Recommended Operating Temperature Range

SYMBOL	PARAMETER	TEST CONDITIONS ¹	MILITARY T _A = -55°C to +125°C V _{CC} MIN = 4.50V V _{CC} MAX = 5.50V MIN TYP ² MAX		COMMERCIAL T _A = 0°C to +70°C V _{CC} MIN = 4.75V V _{CC} MAX = 5.25V MIN TYP ² MAX		UNIT	
V _{OH}	Receiver output HIGH voltage	V _{CC} = V _{IN} V _{IN} = V _{IL} or V _{IH}	I _{OH} = -1.0mA	2.4	3.4	2.4	3.4	V
			I _{OH} = -2.6mA					
V _{OL}	Receiver output LOW voltage	V _{CC} = MIN V _{IN} = V _{IL} or V _{IH}	I _{OL} = 4mA	0.27	0.4	0.27	0.4	V
			I _{OL} = 8mA	0.32	0.45	0.32	0.45	
			I _{OL} = 12mA	0.37	0.5	0.37	0.5	
V _{IH}	Input HIGH level (except bus)	Guaranteed input logical HIGH for all inputs		2.0		2.0		V
V _{IL}	Input LOW level (except bus)	Guaranteed input logical LOW for all inputs			0.7		0.8	V
V _I	Input clamp voltage (except bus)	V _{CC} = MIN, I _{IN} = -18mA		-1.5		-1.5		V
I _{IL}	Input LOW current (except bus)	V _{CC} = MAX, V _{IN} = 0.4V		-0.36		-0.36		mA
I _{IH}	Input HIGH current (except bus)	V _{CC} = MAX, V _{IN} = 2.7V		20		20		μA
I _I	Input HIGH current (except bus)	V _{CC} = MAX, V _{IN} = 5.5V		100		100		μA
I _O	Receiver off-state output current	V _{CC} = MAX	V _O = 2.4V		20		20	μA
			V _O = 0.4V		-20		-20	
I _{SC}	Receiver output short circuit current	V _{CC} = MAX		-12	-65	-12	-65	mA
I _{CC}	Power supply current	V _{CC} = MAX, all inputs = GND		69	105	69	105	mA

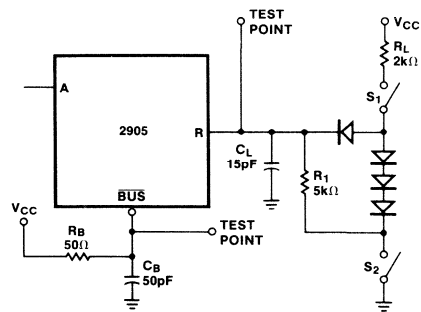


Input/Output Current Interface Conditions



Note: Actual current flow direction shown.

Standard Test Load Circuit



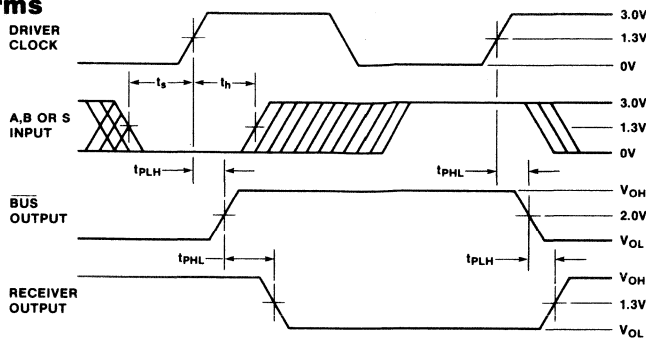
Switching Characteristics

Over Recommended Operating Temperature Range

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY T _A = -55°C to +125°C V _{CC} MIN = 4.50V V _{CC} MAX = 5.50V MIN TYP ² MAX			COMMERCIAL T _A = 0°C to +70°C V _{CC} MIN = 4.75V V _{CC} MAX = 5.25V MIN TYP ² MAX			UNIT
			MIN	TYP ²	MAX	MIN	TYP ²	MAX	
t _{PHL}	Driver clock (DRCP) to bus	C _L (bus) = 50pF R _L (bus) = 50Ω	21	40	21	36	ns		
t _{PLH}			21	40	21	36			
t _{PHL}	Bus enable ($\overline{\text{BE}}$) to bus		13	26	13	23	ns		
t _{PLH}			13	26	13	23			
t _s	Data inputs (A or B)	C _L = 15pF R _L = 2.0kΩ	25		23	ns			
t _h			8.0		7.0				
t _s	Select input (S)		33		30	ns			
t _h			8.0		7.0				
t _{PW}	Driver clock (DRCP) pulse width (HIGH)		28		25	ns			
t _{PLH}	Bus to receiver output (latch enable)		18	37	18	34	ns		
t _{PHL}			18	37	18	34			
t _{PLH}	Latch enable to receiver output		21	37	21	34	ns		
t _{PHL}			21	37	21	34			
t _s	Bus to latch enable ($\overline{\text{RLE}}$)		21		18	ns			
t _h		7.0		5.0					
t _{ZH}	Output control to receiver output	14	28	14	25	ns			
t _{ZL}		14	28	14	25				
t _{HZ}	Output control to receiver output	14	28	14	25	ns			
t _{LZ}		14	28	14	25				

- Notes: 1. For conditions shown as MIN, or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
 2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
 3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Switching Waveforms



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the BUS to R combinatorial delay.

Function Table

INPUTS							INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
S	A _i	B _i	DRCP	$\overline{B\overline{E}}$	RLE	OE	D _i	Q _i	\overline{BUS}_i	R _i	
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	L	X	H	H	L	Driver output disable and receive data via Bus input
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

H = HIGH Z = HIGH Impedance X = Don't care i = 0, 1, 2, 3
 L = LOW NC = No change ↑ = LOW-to-HIGH transition

Definition of Functional Terms

"A" word data input, A₀, A₁, A₂, A₃

The "A" word data input into the two input multiplexers of the driver register.

"B" word data input, B₀, B₁, B₂, B₃

The "B" word data input into the two input multiplexers of the driver register.

Select, S

When the select is LOW, the A data word is applied to the drive register. When the select input is HIGH, the B word is applied to the driver register.

Driver clock pulse, DRCP

Clock pulse for the driver register.

Bus enable, $\overline{B\overline{E}}$

When the bus enable is HIGH, the four drivers are in the high impedance state.

Driver outputs and receiver inputs, $\overline{BUS}_0, \overline{BUS}_1, \overline{BUS}_2, \overline{BUS}_3$

Four driver outputs and receiver inputs (data is inverted).

Receiver outputs, R₀, R₁, R₂, R₃

The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

Receiver latch enable, RLE

When RLE is LOW, data on the BUS inputs is passed through the receiver latches. When RLE is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

Output enable, \overline{OE}

When the \overline{OE} input is HIGH, the four three-state receiver outputs are in the high impedance state.



Quad Two-Input OC Bus Transceiver With Parity 2906

Features/Benefits

- Quad high-speed LSI bus transceiver.
- Open-collector bus driver.
- Two-port input to D-type register on driver.
- Bus driver output can sink 100 mA at 0.8V max.
- Internal odd 4-bit parity checker/generator.
- Receiver has output latch for pipeline operation.
- Receiver outputs sink 12 mA.
- Advanced low-power Schottky processing.
- 100% reliability assurance testing in compliance with MIL-STD-883.

Description

The 2906 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier outputs drive four D-type latches. The device also contains a four-bit odd parity checker/generator.

This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The open-collector bus output can sink up to 100 mA at 0.8V maximum. The BUS input differential amplifier contains disconnect protection diodes such that the bus is fail-

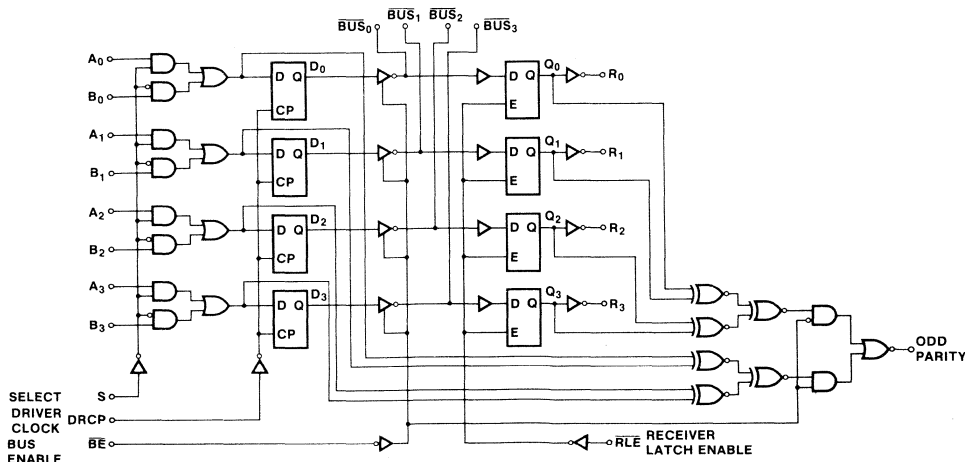
PART NUMBER	PACKAGE	TEMPERATURE RANGE
2906NC	N24	0°C to +70°C
2906JC	J24	0°C to +70°C
2906JM	J24	-55°C to +125°C
2906FM	F24	-55°C to +125°C

safe when power is not applied. The bus enable input (\overline{BE}) is used to force the driver outputs to the high-impedance state. When \overline{BE} is HIGH, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable (\overline{RLE}) input. When the \overline{RLE} input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted). When the \overline{RLE} input is HIGH, the latch will close and retain the present data regardless of the bus input.

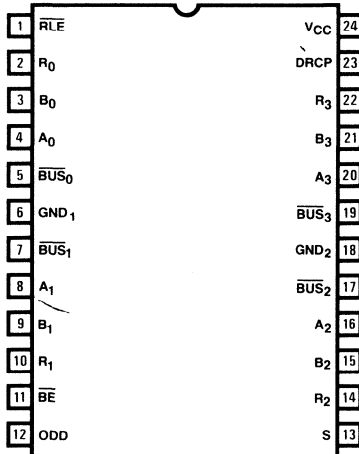
Logic Diagram



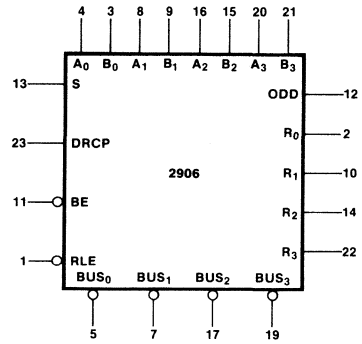
The 2906 features a built-in 4-bit odd parity checker/generator. The bus enable input (\overline{BE}) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A or B

field data input to the driver register. When \overline{BE} is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high impedance state, the BUS parity is checked.

Pin Configuration



Logic Symbol



Absolute Maximum Ratings

Storage temperature	-65°C to +150°C
Temperature (ambient) under bias	-55°C to +125°C
Supply voltage to ground potential	-0.5V to +7V
DC voltage applied to outputs for HIGH output state	-0.5V to +V _{CC} max.
DC input voltage	-0.5V to +5.5V
DC output current, into outputs (except bus)	30mA
DC output current, into bus	200mA
DC input current	-30mA to +5.0mA

**Bus Input/Output Electrical Characteristics
Over Recommended Operating Temperature Range**

SYMBOL	PARAMETER	TEST CONDITIONS ¹	MILITARY T _A = -55°C to +125°C V _{CC} MIN = 4.50V V _{CC} MAX = 5.50V MIN TYP ² MAX		COMMERCIAL T _A = 0°C to +70°C V _{CC} MIN = 4.75V V _{CC} MAX = 5.25V MIN TYP ² MAX		UNIT	
V _{OL}	Bus output LOW voltage	V _{CC} = MIN	I _{OL} = 40mA	0.32	0.5	0.32	0.5	V
			I _{OL} = 70mA	0.41	0.7	0.41	0.7	
			I _{OL} = 100mA	0.55	0.8	0.55	0.8	
I _O	Bus leakage current	V _{CC} = MAX	V _O = 0.4V		-50		-50	μA
			V _O = 4.5V		200		100	
I _{OFF}	Bus leakage current (power OFF)	V _O = 4.5V		100		100	μA	
V _{TH}	Receiver input HIGH threshold	Bus enable = 2.4V	2.4	2.0		2.3	2.0	V
V _{TL}	Receiver input LOW threshold	Bus enable = 2.4V	2.0	1.5		2.0	1.6	V

Electrical Characteristics

Over Recommended Operating Temperature Range

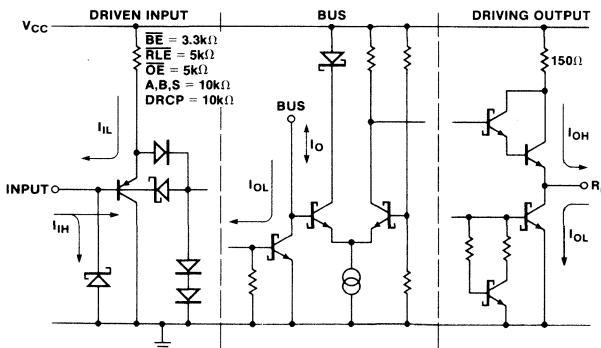
SYMBOL	PARAMETER	TEST CONDITIONS ¹	MILITARY T _A = -55°C to +125°C V _{CC} MIN = 4.50V V _{CC} MAX = 5.50V MIN TYP ² MAX		COMMERCIAL T _A = 0°C to +70°C V _{CC} MIN = 4.75V V _{CC} MAX = 5.25V MIN TYP ² MAX		UNIT
V _{OH}	Receiver Output HIGH voltage	V _{CC} = MIN V _{IN} = V _{IL} or V _{IH}	I _{OH} = -1mA	2.4	3.4		V
			I _{OH} = -2.6mA			2.4 3.4	
	Parity output HIGH voltage	V _{CC} = MIN, I _{OH} = -660μA V _{IN} = V _{IH} or V _{IL}		2.5	3.4	2.7 3.4	
V _{OL}	Output LOW voltage (except bus)	V _{CC} = MIN V _{IN} = V _{IL} or V _{IH}	I _{OL} = 4mA	0.27	0.4	0.27 0.4	V
			I _{OL} = 8mA	0.32	0.45	0.32 0.5	
			I _{OL} = 12mA	0.37	0.5	0.37 0.5	
V _{IH}	Input HIGH level (except bus)	Guaranteed input logical HIGH for all inputs		2.0		2.0	V
V _{IL}	Input LOW level (except bus)	Guaranteed input logical LOW for all inputs			0.7	0.8	V
V _I	Input clamp voltage (except bus)	V _{CC} = MIN, I _I N = -18mA			-1.2	-1.2	V
I _{IL}	Input LOW current (except bus)	V _{CC} = MAX, V _{IN} = 0.4V			-0.36	-0.36	mA
I _{IH}	Input HIGH current (except bus)	V _{CC} = MAX, V _{IN} = 2.7V			20	20	μA
I _I	Input HIGH current (except bus)	V _{CC} = MAX, V _{IN} = 5.5V			100	100	μA
I _{SC}	Output short circuit current (except bus)	V _{CC} = MAX		-12	-65	-12 -65	mA
I _{CC}	Power supply current	V _{CC} = MAX, all inputs = GND		72	105	72 105	mA

Switching Characteristics
Over Recommended Operating Temperature Range

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY T _A = -55°C to +125°C V _{CC} MIN = 4.50V V _{CC} MAX = 5.50V MIN TYP ² MAX			COMMERCIAL T _A = 0°C to +70°C V _{CC} MIN = 4.75V V _{CC} MAX = 5.25V MIN TYP ² MAX			UNIT
t _{PHL}	Driver clock (DRCP) to bus	C _L (bus) = 50pF R _L (bus) = 50Ω	21	40	21	36	ns		
t _{PLH}			21	40	21	36			
t _{PHL}	Bus enable (\overline{BE}) to bus		13	26	13	23		ns	
t _{PLH}			13	26	13	23			
t _S	Data inputs (A or B)		C _L = 15pF R _L = 2.0KΩ	25		23			ns
t _h				8.0		7.0			
t _S	Select inputs (S)	33			30		ns		
t _h		8.0			7.0				
t _{PW}	Clock pulse width (HIGH)	28			25		ns		
t _{PHL}	Bus to receiver output (latch enabled)	18		37	18	34	ns		
t _{PHL}		18		37	18	34			
t _{PLH}	Latch enable to receiver output	21		37	21	34	ns		
t _{PHL}		21		37	21	34			
t _S	Bus to latch enable (\overline{RLE})	21			18		ns		
t _h		7.0			5.0				
t _{PLH}	A or B data to odd parity output (driver enabled)	21		40	21	36	ns		
t _{PHL}		21	40	21	36				
t _{PLH}	Bus to odd parity output (driver inhibited, latch enabled)	21	40	21	36	ns			
t _{PHL}		21	40	21	36				
t _{PLH}	Latch enable (\overline{RLE}) to odd parity output	21	40	21	36	ns			
t _{PHL}		21	40	21	36				

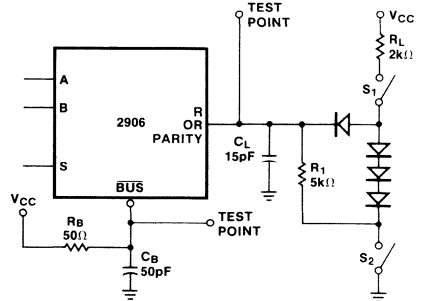
- Notes: 1. For conditions shown as MIN, or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
 2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
 3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Input/Output Current Interface Conditions

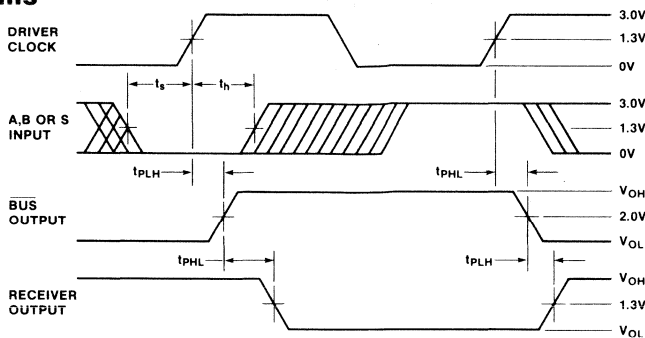


Note: Actual current flow direction shown.

Standard Test Load Circuit



Switching Waveforms



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the BUS to R combinatorial delay.

Function Table

INPUTS						INTERNAL TO DEVICE		BUS	OUTPUT		FUNCTION
S	A _i	B _i	DRCP	$\overline{B\overline{E}}$	\overline{RLE}	\overline{OE}	D _i	Q _i	BUS _i	R _i	
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	L	X	H	H	L	
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

H = HIGH Z = HIGH Impedance X = Don't care i = 0, 1, 2, 3
 L = LOW NC = No change ↑ = LOW to HIGH transition

Definition of Functional Terms

“A” word data input, A₀, A₁, A₂, A₃

The “A” word data input into the two input multiplexers of the driver register.

“B” word data input, B₀, B₁, B₂, B₃

The “B” word data input into the two input multiplexers of the driver register.

Select, S

When the select is LOW, the A data word is applied to the drive register. When the select input is HIGH, the B word is applied to the driver register.

Driver clock pulse, DRCP

Clock pulse for the driver register.

Bus enable, $\overline{B\overline{E}}$

When the bus enable is HIGH, the four drivers are in the high impedance state.

Driver outputs and receiver inputs, $\overline{BUS_0}$, $\overline{BUS_1}$, $\overline{BUS_2}$, $\overline{BUS_3}$

Four driver outputs and receiver inputs (data is inverted).

Receiver outputs, R₀, R₁, R₂, R₃

The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

Receiver latch enable, \overline{RLE}

When \overline{RLE} is LOW, data on the BUS inputs is passed through the receiver latches. When \overline{RLE} is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

Output enable, \overline{OE}

When the \overline{OE} input is HIGH, the four three-state receiver outputs are in the high-impedance state.



Quad Bus Transceiver With Three-State Receiver and Parity

2907

Features/Characteristics

- Quad high-speed LSI bus transceiver
- Open-collector bus driver
- D-type register on driver
- Bus driver output can sink 100 mA at 0.8 V max.
- Internal odd 4-bit parity checker/generator
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12 mA
- Advanced Low-Power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

Description

The 2907 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier outputs drive four D-type latches, that feature three-state outputs. The device also contains a four-bit odd parity checker/generator.

This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs)

PART NUMBER	PACKAGE	TEMPERATURE RANGE
2907NC	N20	0°C to +70°C
2907JC	J20	0°C to +70°C
2907JM	J20	-55°C to +125°C
2907FM*	F20	-55°C to +125°C

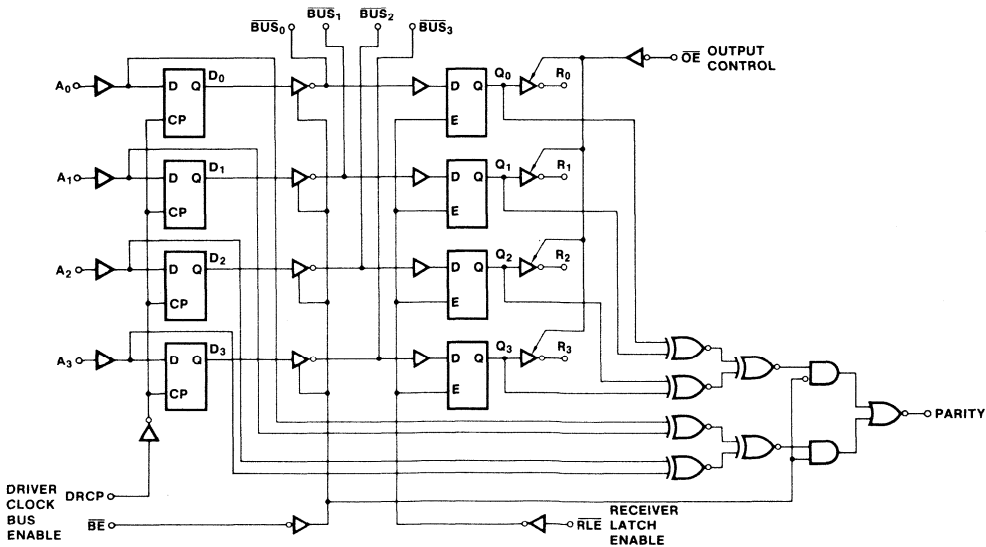
* Available on special order

are one LS unit load. The open-collector bus output can sink up to 100 mA at 0.8 V maximum. The BUS input differential amplifier contains disconnect protection diodes such that the bus is fail-safe when power is not applied. The bus enable input (\overline{BE}) is used to force the driver outputs to the high-impedance state. When \overline{BE} is HIGH, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

The input register consists of four D-type flip-flops with a buffered common clock. The buffered common clock (DRCP) enters the A_i data into this drive register on the LOW-to-HIGH transition.

Data from the A input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four

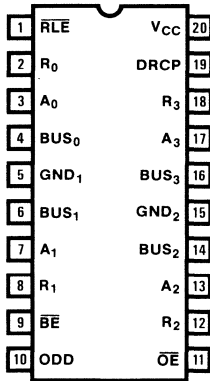
Logic Diagram



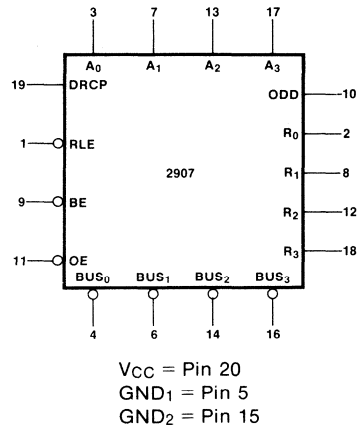
receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable (\overline{RLE}) input. When the \overline{RLE} input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and \overline{OE} LOW). When the \overline{RLE} input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control (\overline{OE}) input. When \overline{OE} is HIGH, the receiver outputs are in the high-impedance state.

The 2907 features a built-in four-bit odd parity checker/generator. The bus enable input (\overline{BE}) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A field data input to the driver register. When \overline{BE} is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

Pin Configuration



Logic Symbol



Absolute Maximum Ratings

Storage temperature	-65°C to +150°C
Temperature (ambient) under bias	-55°C to +125°C
Supply voltage to ground potential	-0.5V to +7V
DC voltage applied to outputs for HIGH output state	-0.5V to +VCC max.
DC input voltage	-0.5V to +5.5V
DC output current, into outputs (except bus)	30mA
DC output current, into bus	200mA
DC input current	-30mA to +5.0mA

Bus Input/Output Electrical Characteristics
Over Recommended Operating Temperature Range

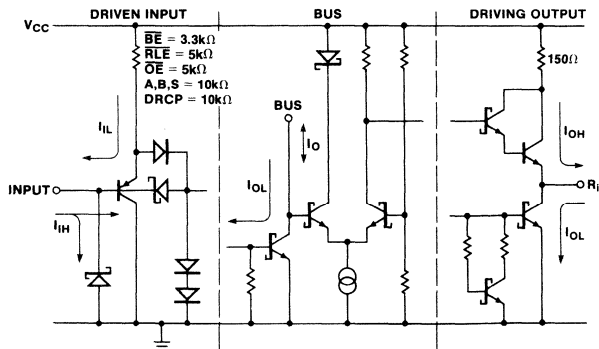
SYMBOL	PARAMETER	TEST CONDITIONS ¹	MILITARY TA = -55°C to +125°C VCC MIN = 4.50V VCC MAX = 5.50V MIN TYP ² MAX		COMMERCIAL TA = 0°C to +70°C VCC MIN = 4.75V VCC MAX = 5.25V MIN TYP ² MAX		UNIT	
VOL	Bus output LOW voltage	VCC = MIN	IOL = 40mA	0.32	0.5	0.32	0.5	V
			IOL = 70mA	0.41	0.7	0.41	0.7	
			IOL = 100mA	0.55	0.8	0.55	0.8	
IOL	Bus leakage current	VCC = MAX	VO = 0.4V		-50		-50	μA
			VO = 4.5V		200		100	
I _{OFF}	Bus leakage current (power OFF)	VO = 4.5V		100		100	μA	
VTH	Receiver input HIGH threshold	Bus enable = 2.4V	2.4	2.0		2.3	2.0	V
VTL	Receiver input LOW threshold	Bus enable = 2.4V	2.0	1.5		2.0	1.6	V

Electrical Characteristics
Over Recommended Operating Temperature Range

SYMBOL	PARAMETER	TEST CONDITIONS ¹	MILITARY T _A = -55°C to +125°C V _{CC} MIN = 4.50V V _{CC} MAX = 5.50V MIN TYP ² MAX		COMMERCIAL T _A = 0°C to +70°C V _{CC} MIN = 4.75V V _{CC} MAX = 5.25V MIN TYP ² MAX		UNIT
V _{OH}	Receiver Output HIGH voltage	V _{CC} = MIN V _{IN} = V _{IL} or V _{IH}	I _{OH} = -1mA	2.4	3.4		V
			I _{OH} = -2.6mA			2.4 3.4	
	Parity output HIGH voltage	V _{CC} = MIN, I _{OH} = -660μA V _{IN} = V _{IH} or V _{IL}		2.5	3.4	2.7 3.4	
V _{OL}	Output LOW voltage (except bus)	V _{CC} = MIN V _{IN} = V _{IL} or V _{IH}	I _{OL} = 4mA	0.27	0.4	0.27 0.4	V
			I _{OL} = 8mA	0.32	0.45	0.32 0.5	
			I _{OL} = 12mA	0.37	0.5	0.37 0.5	
V _{IH}	Input HIGH level (except bus)	Guaranteed input logical HIGH for all inputs		2.0		2.0	V
V _{IL}	Input LOW level (except bus)	Guaranteed input logical LOW for all inputs			0.7	0.8	V
V _I	Input clamp voltage (except bus)	V _{CC} = MIN, I _{IIN} = -18mA			-1.2	-1.2	V
I _{IL}	Input LOW current (except bus)	V _{CC} = MAX, V _{IN} = 0.4V			-0.36	-0.36	mA
I _{IH}	Input HIGH current (except bus)	V _{CC} = MAX, V _{IN} = 2.7V			20	20	μA
I _I	Input HIGH current (except bus)	V _{CC} = MAX, V _{IN} = 5.5V			100	100	μA
I _{SC}	Output short circuit current (except bus)	V _{CC} = MAX		-12	-65	-12 -65	mA
I _{CC}	Power supply currents	V _{CC} = MAX, all inputs = GND		72	110	75 110	mA
I _O	Off-state output current (receiver outputs)	V _{CC} = MAX	V _O = 2.4V			20	μA
			V _O = 0.4V			-20	

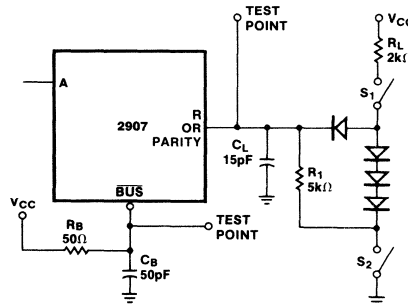


Input/Output Current Interface Conditions



Note: Actual current flow direction shown.

Standard Test Load Circuit



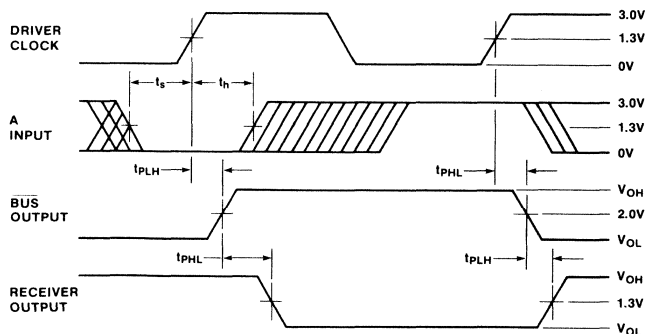
Switching Characteristics

Over Recommended Operating Temperature Range

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ V_{CC} MIN = 4.50V V_{CC} MAX = 5.50V MIN TYP2 MAX			COMMERCIAL $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ V_{CC} MIN = 4.75V V_{CC} MAX = 5.25V MIN TYP2 MAX			UNIT
t _{PHL}	Driver clock (DRCP)	$C_L(\text{bus}) = 50\text{pF}$ $R_L(\text{bus}) = 50\Omega$	21	40	21	36	ns		
t _{PLH}	to bus		21	40	21	36			
t _{PHL}	Bus enable ($\overline{\text{BE}}$) to bus		13	26	13	23			
t _{PLH}			13	26	13	23			
t _s	A data inputs	$C_L = 15\text{pF}$ $R_L = 2.0\text{k}\Omega$	25		23		ns		
t _h			8.0		7.0				
t _{PW}	Clock pulse width (HIGH)		28		25		ns		
t _{PLH}	Bus to receiver output		18	37	18	34	ns		
t _{PHL}	(latch enabled)		18	37	18	34			
t _{PLH}	Latch enable to		21	37	21	34	ns		
t _{PHL}	receiver output		21	37	21	34			
t _s	Bus to latch		21		18		ns		
t _h	enable ($\overline{\text{RL}}\overline{\text{E}}$)		7.0		5.0				
t _{PLH}	A data to odd parity		21	40	21	36	ns		
t _{PHL}	out (driver enabled)		21	40	21	36			
t _{PLH}	Bus to odd parity		21	40	21	36	ns		
t _{PHL}	out (driver inhibit)		21	40	21	36			
t _{PLH}	Latch enable ($\overline{\text{RL}}\overline{\text{E}}$)		21	40	21	36	ns		
t _{PHL}	to odd parity output	21	40	21	36				
t _{ZH}	Output control to output	$C_L = 5.0\text{pF}$ $R_L = 2.0\text{k}\Omega$	14	28	14	25	ns		
t _{ZL}			14	28	14	25			
t _{HZ}	Output control to output		14	28	14	25	ns		
t _{LZ}			14	28	14	25			

- Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
 2. Typical limits are at $V_{CC} = 5.0\text{V}$, 25°C ambient and maximum loading.
 3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Switching Waveforms



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the BUS to R combinatorial delay.

Function Table

INPUTS					INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
A _i	DRCP	\overline{BE}	\overline{RLE}	\overline{OE}	D _i	Q _i	B _i	R _i	
X	X	H	X	X	X	X	H	X	Driver output disable
X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	H	L	L	X	H	H	L	
X	X	X	H	X	X	NC	X	X	Latch received data
L	↑	X	X	X	L	X	X	X	Load driver register
H	↑	X	X	X	H	X	X	X	
X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	H	X	X	X	NC	X	X	X	
X	X	L	X	X	L	X	H	X	Drive Bus
X	X	L	X	X	H	X	L	X	

H = HIGH

Z = High Impedance

X = Don't Care

i = 0, 1, 2, 3

L = LOW

NC = No Change

↑ = LOW-to-HIGH Transition

Definition of Functional Terms

Driver clock pulse, DRCP

Clock pulse for the driver register.

Bus enable, \overline{BE}

When the bus enable is LOW, the four drivers are in the high impedance state.

Driver outputs and receiver inputs, BUS₀, BUS₁, BUS₂, BUS₃

Four driver outputs and receiver inputs (data is inverted).

Receiver outputs, R₀, R₁, R₂, R₃

The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

Receiver latch enable, \overline{RLE}

When \overline{RLE} is LOW, data on the BUS inputs is passed through the receiver latches. When \overline{RLE} is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

Odd parity output, ODD

Generates parity with the driver enabled, checks parity with the driver in the high-impedance state.

Output enable, \overline{OE}

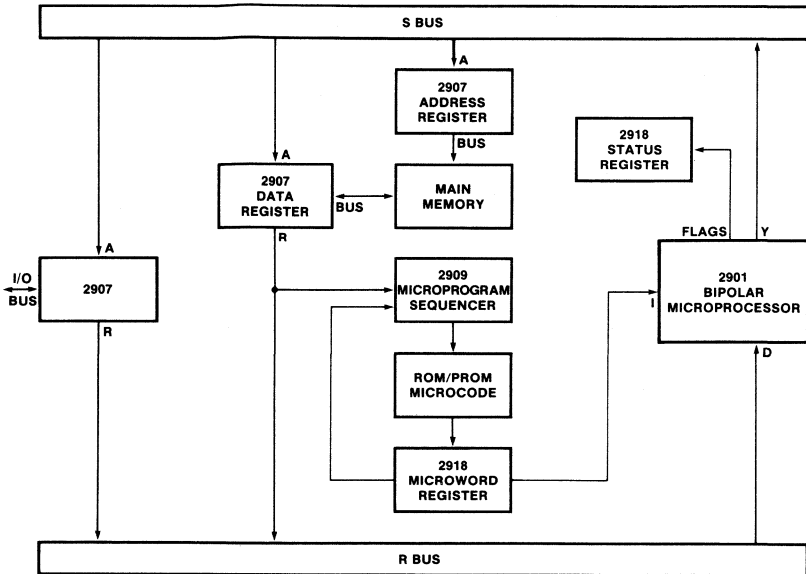
When the \overline{OE} input is HIGH, the four three-state receiver outputs are in the high-impedance state.

Parity Output Function Table

\overline{BE}	ODD PARITY OUTPUT
L	ODD = A ₀ ⊕ A ₁ ⊕ A ₂ ⊕ A ₃
H	ODD = Q ₀ ⊕ Q ₁ ⊕ Q ₂ ⊕ Q ₃

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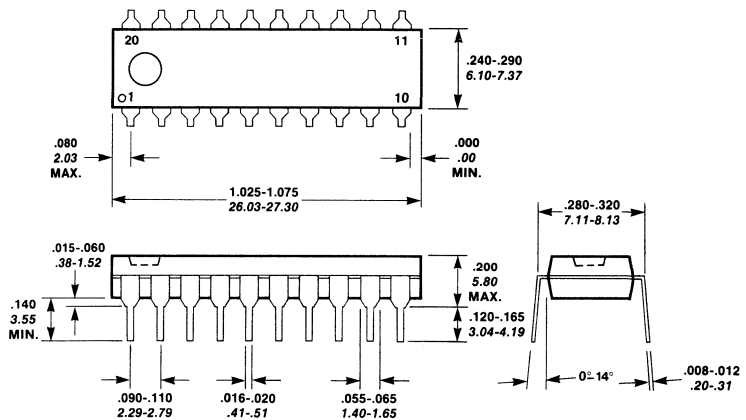
Applications



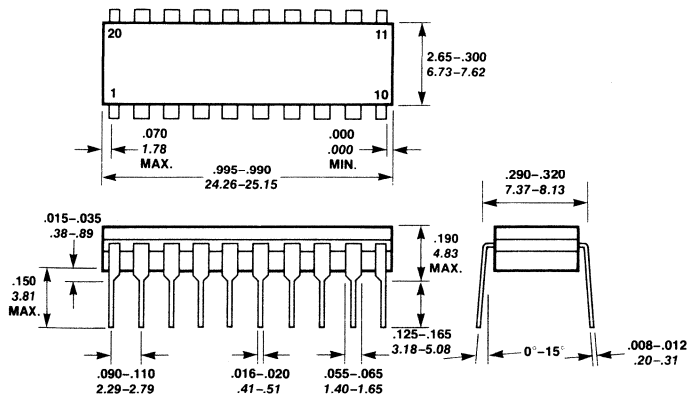
The 2907 can be used as an I/O Bus Transceiver and Main Memory I/O Transceiver in high-speed Microprocessor Systems.

Package Drawings

N20 Plastic Kool DIP



J20 Ceramic DIP



UNLESS OTHERWISE SPECIFIED:
 ALL DIMENSIONS MIN.-MAX. IN INCHES.
 ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.

Microprogram Sequencers

2909/2911

Features/Benefits

- 4-bit slice cascadable to any number of microwords
- Internal address register
- Branch input for N-way branches
- Cascadable 4-bit microprogram counter
- 4 x 4 file with stack pointer and push/pop control for nesting microsubroutines
- Zero input for returning to the zero microcode word
- Individual OR input for each bit for branching to higher microinstructions (2909 only)
- Three-state outputs
- All internal registers change state on the LOW-to-HIGH transition of the clock
- 2909 in 28 pin package
- 2911 in 20 pin package

Description

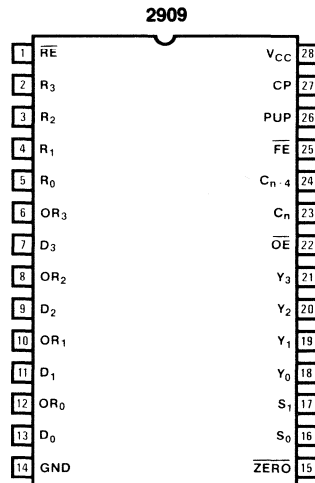
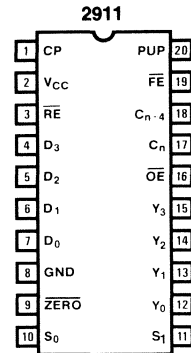
The 2909 is a 4-bit wide address controller intended for sequencing through a series of microinstructions contained in a ROM or PROM. Two 2909's may be interconnected to generate an 8-bit address (256 words), and three may be used to generate a 12-bit address (4K words).

The 2909 can select an address from any of four sources. They are: 1) a set of external direct inputs (D); 2) external data from the R inputs, stored in an internal register; 3) a four-word deep push/pop stack; or 4) a program counter register (which usually contains the last address plus one). The push/pop stack includes certain control lines so that it can efficiently execute nested subroutine linkages. Each of the four outputs can be OR'ed with an external input for conditional skip or branch instructions, and a separate line forces the outputs to all zeroes. The outputs are three-state.

The 2911 is an identical circuit to the 2909, except the four OR inputs are removed and the D and R inputs are tied together. The 2911 is in a 20 pin, 0.3" centers package.

PART NUMBER		PACKAGE		TEMPERATURE RANGE
2909	2911	2909	2911	
2909NC	2911NC	N28	N20	0°C to +70°C
2909JC	2911JC	J28	J20	0°C to +70°C
2909JM	2911JM	J28	J20	-55°C to +125°C
2909FM	—	F28	—	-55°C to +125°C

Pin Configuration



Block Diagram

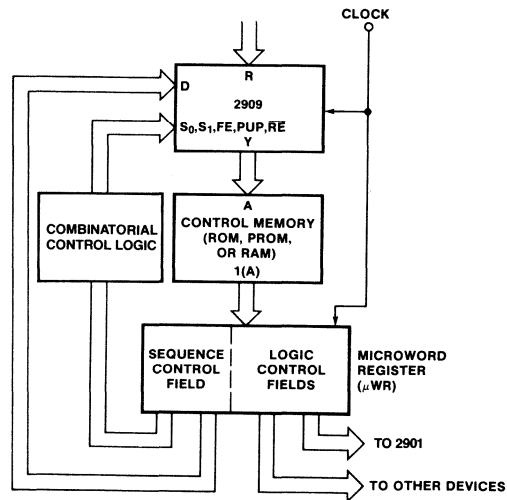
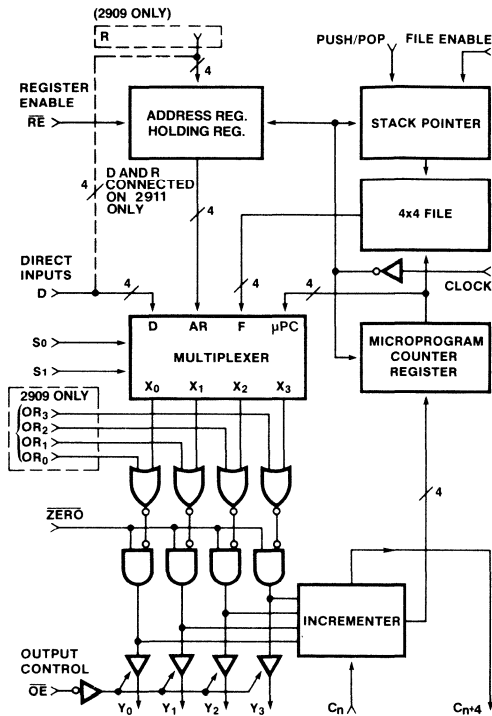


Figure 3. Microprogram Sequencer Control.

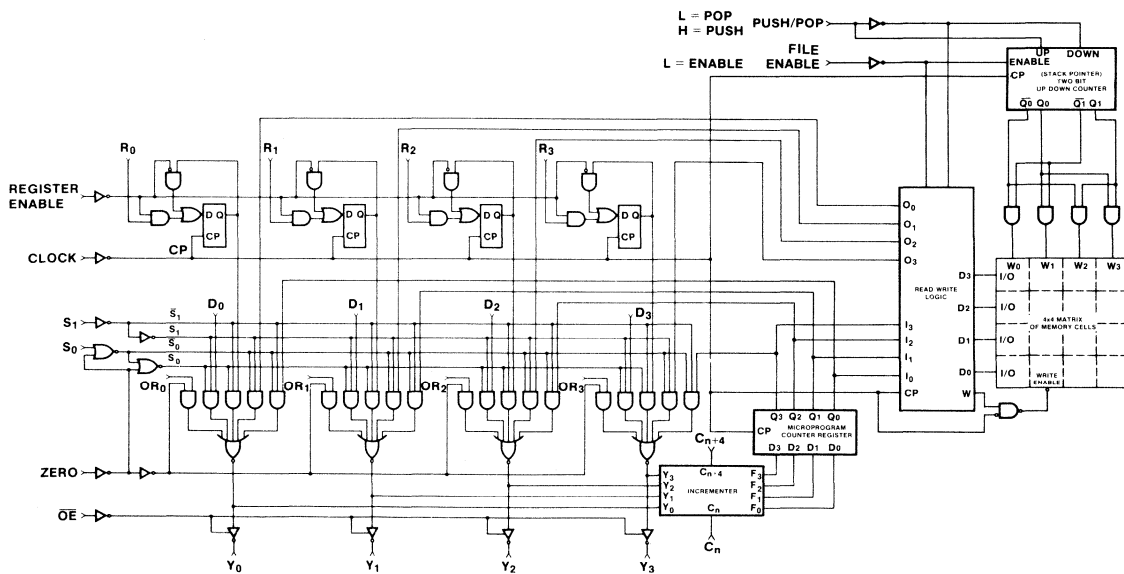


Figure 2. Microprogram Sequencer Block Diagram.

Absolute Maximum Ratings

Storage temperature	-65°C to +150°C
Temperature (ambient) under bias	-55°C to +125°C
Supply voltage to ground potential	-0.5 V to +7.0 V
DC voltage applied to outputs for HIGH output state	-0.5 V to +V _{CC} max.
DC input voltage	-0.5 V to +7.0 V
DC output current, into outputs	30 mA
DC input current	-30 mA to +5.0 mA

Electrical Characteristics

Over Recommended Operating Range

SYMBOL	PARAMETER	TEST CONDITIONS ¹	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	Output HIGH voltage	V _{CC} = MIN., V _{IN} = V _{IH} or V _{IL}	I _{OH} = -1.0mA		2.4			V	
			I _{OH} = -2.6mA			2.4			
V _{OL}	Output LOW voltage	V _{CC} = MIN., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 4.0mA			0.4	0.4	V	
			I _{OL} = 8.0mA			0.45	0.45		
			I _{OL} = 12mA ⁵			0.5	0.5		
V _{IH}	Input HIGH level	Guaranteed input logical HIGH voltage for all inputs			2.0		2.0	V	
V _{IL}	Input LOW level	Guaranteed input logical LOW voltage for all inputs				0.7	0.8	V	
V _I	Input clamp voltage	V _{CC} = MIN., I _{IN} = -18mA				-1.5	-1.5	V	
I _{IL}	Input LOW current	V _{CC} = MAX., V _{IN} = 0.4V	C _n			-1.08	-1.08	mA	
			Push/Pop, \overline{OE}			-0.72	-0.72		
			Others ⁶			-0.36	-0.36		
I _{IH}	Input HIGH current	V _{CC} = MAX., V _{IN} = 2.7V	C _n			40	40	μA	
			Push/Pop			40	40		
			Others ⁶			20	20		
I _I	Input HIGH current	V _{CC} = MAX., V _{IN} = 7.0V	C _n , Push/Pop			0.2	0.2	mA	
			Others ⁶			0.1	0.1		
I _{OS}	Output short circuit current ³	V _{CC} = MAX	Y ₀ -Y ₃		-30	-100	-30	-100	mA
			C _n +4		-30	-85	-30	-85	
I _{CC}	Power supply current	V _{CC} = MAX ⁴			80	130	80	130	mA
I _{OZL}	Output OFF current	V _{CC} = MAX., \overline{OE} = 2.7V	V _{OUT} = 0.4V			-20	-20	μA	
I _{OZH}			V _{OUT} = 2.7V			20	20		

- NOTES: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
 2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
 3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

4. Apply GND to C_n, R₀, R₁, R₂, R₃, OR₀, OR₁, OR₂, OR₃, D₀, D₁, D₂, and D₃. Other inputs open. All outputs open. Measured after a LOW-to-HIGH clock transition.
 5. The 12mA guarantee applies only to Y₀, Y₁, Y₂ and Y₃.
 6. For the 2911, D_i and R_i are internally connected. Loading is doubled (to same values as Push/Pop).

7

Switching Characteristics

Over Operating Range

All parameters are guaranteed worst case over the operating voltage and temperature range for the device type.
(Grade C = 0°C to +70°C, 4.75V to 5.25V; Grade M = -55°C to +125°C, 4.5V to 5.5V)

Table 1
Minimum Clock Requirements

Minimum Clock LOW Time	50
Minimum Clock HIGH Time	30

Table 2
Maximum Combinatorial Propagation Delays

OUTPUTS INPUTS	Y_i	$C_n + 4$
\overline{OE}	25	—
ZERO	35	45
OR_i	20	32
S_0, S_1	40	50
D_i	20	32
C_n	—	18

Table 3
Maximum Delays
From Clock to Outputs

FUNCTIONAL PATH	GRADE	CLOCK TO Y_i	CLOCK TO $C_n + 4$
Register ($S_1 S_0 = LH$)	C	48	58
	M	55	65
μ Program Counter ($S_1 S_0 = LL$)	C	48	58
	M	55	65
File ($S_1 S_0 = HL$)	C	70	80
	M	80	90

$$R_L = 2.0k\Omega \quad C_L = 15pF$$

Table 4
Set-up and Hold Time
Requirements

EXTERNAL INPUTS	t_s	t_h
\overline{RE}	20	5.0
R_i	15	0
PUSH/POP	20	5.0
FE	20	0
C_n	15	0
D_i	20	0
OR_i	20	0
S_0, S_1	40	0
ZERO	40	0

Architecture of the 2909/2911

The 2909/2911 are bipolar microprogram sequencers intended for use in high-speed microprocessor applications. The device is a cascaded 4-bit slice such that two devices allow addressing of up to 256 words of microprogram and three devices allow addressing of up to 4K words of microprogram. A detailed logic diagram is shown in Figure 2.

The device contains a four-input multiplexer that is used to select either the address register, direct inputs, microprogram counter, or file as the source of the next microinstruction address. This multiplexer is controlled by the S_0 and S_1 inputs.

The address register consists of four D-type, edge triggered flip-flops with a common clock enable. When the address register enable is LOW, new data is entered into the register on the clock LOW-to-HIGH transition. The address register is available at the multiplexer as a source for the next microinstruction address. The direct input is a 4-bit field of inputs to the multiplexer and can be selected as the next microinstruction address. On the 2911, the direct inputs are also used as inputs to the register. This allows an N-way branch where N is any word in the microcode.

The 2909/2911 contains a microprogram counter (μ PC) that is composed of a 4-bit incrementer followed by a 4-bit register. The incrementer has carry-in (C_n) and carry-out (C_{n+4}) such that cascading to larger word lengths is straightforward. The μ PC can be used in either of two ways. When the least significant carry-in to the incrementer is HIGH, the microprogram register is loaded on the next clock cycle with the current Y output word plus one ($Y+1 \rightarrow \mu$ PC.) Thus sequential microinstructions can be executed. If this least significant C_n is LOW, the incrementer passes the Y output word unmodified and the microprogram register is loaded with the same Y word on the next clock cycle ($Y \rightarrow \mu$ PC). Thus, the same microinstruction can be executed any number of times by using the least significant C_n as the control.

The last source available at the multiplexer input is the 4 x 4 file (stack). The file is used to provide return address linkage when executing microsubroutines. The file contains a built-in stack pointer (SP) which always points to the last file word written. This allows stack reference operations (looping) to be performed without a push or pop.

The stack pointer operates as an up/down counter with separate push/pop and file enable inputs. When the file enable input is LOW and the push/pop input is HIGH, the PUSH operation is enabled. This causes the stack pointer to increment and the file to be written with the required return linkage—the next microinstruction address following the subroutine jump which initiated the PUSH.

If the file enable input is LOW and the push/pop control is LOW, a POP operation occurs. This implies the usage of the return linkage during this cycle and thus a return from subroutine. The next LOW-to-HIGH clock transition causes the stack pointer to decrement. If the file enable is HIGH, no action is taken by the stack pointer regardless of any other input.

The stack pointer linkage is such that any combination of pushes, pops or stack references can be achieved. One microinstruction subroutines can be performed. Since the stack is 4 words deep, up to four microsubroutines can be nested.

The ZERO input is used to force the four outputs to the binary zero state. When the ZERO input is LOW, all Y outputs are LOW

regardless of any other inputs (except $\bar{O}E$). Each Y output bit also has a separate OR input such that a conditional logic one can be forced at each Y output. This allows jumping to different microinstructions on programmed conditions.

The 2909/2911 feature three-state Y outputs. These can be particularly useful in military designs requiring external Ground Support Equipment (GSE) to provide automatic checkout of the microprocessor. The internal control can be placed in the high-impedance state, and preprogrammed sequences of microinstructions can be executed via external access to the control ROM/PROM.

Definition of Terms

A set of symbols is used in this data sheet to represent various internal and external registers and signals used with the 2909. Since its principle application is as a controller for a microprogram store, it is necessary to define some signals associated with the microcode itself. Figure 3 illustrates the basic interconnection of 2909, memory, and microinstruction register. The definitions here apply to this architecture.

Inputs to 2909/2911

S_1, S_0	Control lines for address source selection
$\bar{F}E, PUP$	Control lines for push/pop stack
$\bar{R}E$	Enable line for internal address register
OR_i	Logic OR inputs on each address output line
$\bar{Z}ERO$	Logic AND input on the output lines
$\bar{O}E$	Output Enable. When $\bar{O}E$ is HIGH, the Y outputs are OFF (high impedance)
C_n	Carry-in to the incrementer
R_i	Inputs to the internal address register
D_i	Direct inputs to the multiplexer
CP	Clock input to the AR and μ PC register and Push-Pop stack

Outputs from the 2909/2911

Y_i	Address outputs from 2909. (Address inputs to control memory.)
C_{n+4}	Carry out from the incrementer

Internal Signals

μ PC	Contents of the microprogram counter
REG	Contents of the register
STK0-STK3	Contents of the push/pop stack. By definition, the word in the four-by-four file, addressed by the stack pointer is STK0. Conceptually data is pushed into the stack at STK0; a subsequent push moves STK0 to STK1; a pop implies STK3 \rightarrow STK2 \rightarrow STK1 \rightarrow STK0. Physically, only the stack pointer changes when a push or pop is performed. The data does not move. I/O occurs at STK0.
SP	Contents of the stack pointer.

External to the 2909/2911

A	Address to the control memory
I(A)	Instruction in control memory at address A
μ WR	Contents of the microword register (at output of control memory). The microword register contains the instruction currently being executed.
T_n	Time period (cycle) n

7

Address Selection

OCTAL	S ₁	S ₀	SOURCE FOR Y OUTPUTS	SYMBOL
0	L	L	Microprogram Counter	μPc
1	L	H	Register	REG
2	H	L	Push-Pop stack	STK0
3	H	H	Direct inputs	D _i

Output Control

OR _i	$\overline{\text{ZERO}}$	$\overline{\text{OE}}$	Y _i
X	X	H	Z
X	L	L	L
H	H	L	H
L	H	L	Source selected by S ₀ S ₁

Z = High Impedance

Synchronous Stack Control

$\overline{\text{FE}}$	PUP	PUSH-POP STACK CHANGE
H	X	No change
L	H	Increment stack pointer, then push current PC onto STK0
L	L	Pop stack (decrement stack pointer)

H = High
L = Low
X = Don't Care

Figure 5.

CYCLE	S ₁ , S ₀ , $\overline{\text{FE}}$, PUP	μPC	REG	STK0	STK1	STK2	STK3	YOUT	COMMENT	PRINCIPLE USE
N N+1	0 0 0 0 —	J J+1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	J —	Pop Stack	End Loop
N N+1	0 0 0 1 —	J J+1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	J —	Push μPC	Set-up Loop
N N+1	0 0 1 X —	J J+1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	J —	Continue	Continue
N N+1	0 1 0 0 —	J K+1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	K —	Pop Stack; Use AR for Address	End Loop
N N+1	0 1 0 1 —	J K+1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	K —	Push μPC; Jump to Address in AR	JSR AR
N N+1	0 1 1 X —	J K+1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	K —	Jump to Address in AR	JMP AR
N N+1	1 0 0 0 —	J Ra+1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	Ra —	Jump to Address in STK0; Pop Stack	RTS
N N+1	1 0 0 1 —	J Ra+1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	Ra —	Jump to Address in STK0; Push μPc	
N N+1	1 0 1 X —	J Ra+1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	Ra —	Jump to Address in STK0	Stack Ref (Loop)
N N+1	1 1 0 0 —	J D+1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	D —	Pop Stack; Jump to Address on D	End Loop
N N+1	1 1 0 1 —	J D+1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	D —	Jump to Address on D; Push μPC	JSR D
N N+1	1 1 1 X —	J D+1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	D —	Jump to Address on D	JMP D

X = Don't care, 0 = LOW, 1 = HIGH, Assume C_n = HIGH

Note: STK0 is the location addressed by the stack pointer.

Figure 6. Output and Internal Next-Cycle Register States for 2909/2911.

Operation of the 2909/2911

Figure 5 lists the select codes for the multiplexer. The two bits applied from the microword register (and additional combinational logic for branching) determine which data source contains the address for the next microinstruction. The contents of the selected source will appear on the Y outputs. Figure 5 also shows the truth table for the output control and for the control of the push/pop stack. Figure 6 shows in detail the effect of S₀, S₁, \overline{FE} and PUP on the 2909. These four signals define what address appears on the Y outputs and what the state of all the internal registers will be following the clock LOW-to-HIGH edge. In this illustration, the microprogram counter is assumed to contain initially some word J, the address register some word K, and the four words in the push/pop stack contain R_A through R_D.

Figure 7 illustrates the execution of a subroutine using the 2909. The configuration of Figure 3 is assumed. The instruction being executed at any given time is the one contained in the microword

register (μ WR). The contents of the μ WR also controls (indirectly, perhaps) the four signals S₀, S₁, FE, and PUP. The starting address of the subroutine is applied to the D inputs of the 2909 at the appropriate time.

In the columns on the left is the sequence of microinstructions to be executed. At address J+2, the sequence control portion of the microinstruction contains the command "Jump to subroutine at A". At the time T₂, this instruction is in the μ WR, and the 2909 inputs are set-up to execute the jump and save the return address. The subroutine address A is applied to the D inputs from the μ WR and appears on the Y outputs. The first instruction of the subroutine, I(A), is accessed and is at the inputs of the μ WR. On the next clock transition, I(A) is loaded into the μ WR for execution, and the return address J+3 is pushed onto the stack. The return instruction is executed at T₅. Figure 8 is a similar timing chart showing one subroutine linking to a second, the latter consisting of only one microinstruction.

Control Memory

EXECUTE CYCLE	MICROPROGRAM		EXECUTE CYCLE SIGNALS	EXECUTE CYCLE CLOCK										
	ADDRESS	SEQUENCER INSTRUCTION		T ₀	T ₁	T ₂	T ₃	T ₄	T ₅	T ₆	T ₇	T ₈	T ₉	
T ₀	J-1	—	2909 Inputs (from μ WR)	S ₁ , S ₀	0	0	3	0	0	3	2	0	2	0
T ₁	J	—		FE	H	H	L	H	H	L	L	H	L	H
T ₂	J+1	—		PUP	X	X	H	X	X	H	L	X	L	X
T ₂	J+2	JSR A		D	X	X	A	X	X	B	X	X	X	X
T ₉	J+3	—												
	—	—	Internal Registers	μ PC	J+1	J+2	J+3	A+1	A+2	A+3	B+1	A+4	A+5	J+4
	—	—		STK0	—	—	—	J+3	J+3	J+3	A+3	J+3	J+3	
	—	—		STK1	—	—	—	—	—	—	J+3	—	—	
	—	—		STK2	—	—	—	—	—	—	—	—	—	
	—	—		STK3	—	—	—	—	—	—	—	—	—	
T ₃	A	I(A)	2909 Output	Y	J+1	J+2	A	A+1	A+2	B	A+3	A+4	J+3	J+4
T ₄	A+1	—	ROM Output	(Y)	I(J+1)	JSR A	I(A)	I(A+1)	JSR B	RTS	I(A+3)	RTS	I(J+3)	I(J+4)
T ₅	A+2	JSR B												
T ₇	A+3	—	Contents of μ WR (Instruction being executed)	μ WR	I(J)	I(J+1)	JSR A	I(A)	I(A+1)	JSR B	RTS	I(A+3)	RTS	I(J+3)
T ₈	A+4	RTS												
T ₆	B	RTS												

Figure 7. Subroutine Execution.



Control Memory

EXECUTE CYCLE	MICROPROGRAM		EXECUTE CYCLE CLOCK SIGNALS		T ₀	T ₁	T ₂	T ₃	T ₄	T ₅	T ₆	T ₇	T ₈	T ₉
	ADDRESS	SEQUENCER INSTRUCTION												
	J-1	—	2909	S ₁ , S ₀	0	0	3	0	0	2	0	0		
T ₀	J	—	Inputs	\overline{FE}	H	H	L	H	H	L	H	H		
T ₁	J+1	—	(from PUP	μWR)	X	X	H	X	X	L	X	X		
T ₂	J+2	JSR A		D	X	X	A	X	X	X	X	X		
T ₆	J+3	—												
T ₇	J+4	—												
	—	—		μPC	J+1	J+2	J+3	A+1	A+2	A+3	J+4	J+5	—	—
	—	—	Internal Registers	STK0	—	—	—	J+3	J+3	J+3	—	—	—	—
	—	—		STK1	—	—	—	—	—	—	—	—	—	—
	—	—		STK2	—	—	—	—	—	—	—	—	—	—
	—	—		STK3	—	—	—	—	—	—	—	—	—	—
T ₃	A	1(-A)	2909	Y	J+1	J+2	A	A+1	A+2	J+3	J+4	J+5		
T ₄	A+1	—	Output											
T ₅	A+2	RTS	ROM	(Y)	I(J+1)	JSR A	I(A)	I(A+1)	RTS	I(J+3)	I(J+4)	I(J+5)		
	—	—	Output											
	—	—	Contents of μWR											
	—	—	(Instruction being executed)	μWR	I(J)	I(J+1)	JSR A	I(A)	I(A+1)	RTS	I(J+3)	I(J+4)		

Figure 8. Two Nested Subroutines. Routine B is Only One Instruction.

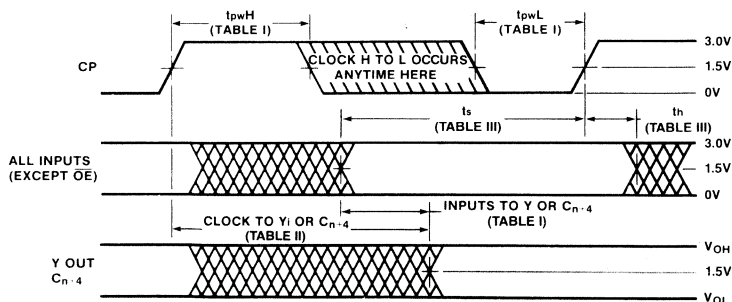


Figure 12. Switching Waveforms. See Tables for Specific Values.

Quad Three-State Bus Transceiver With Interface Logic 2915

Features/Benefits

- Quad high-speed LSI bus transceiver
- Three-state bus driver
- Two-port input to D-type register on driver
- Bus driver output can sink 40mA at 0.5V max.
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12mA
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883
- 3.5V minimum output high voltage for direct interface to MOS microprocessors

Description

The 2915 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches that feature three-state outputs.

This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 40mA at 0.5V maximum. The bus enable input (\overline{BE}) is used to force the driver outputs to the high-impedance state. When \overline{BE} is HIGH,

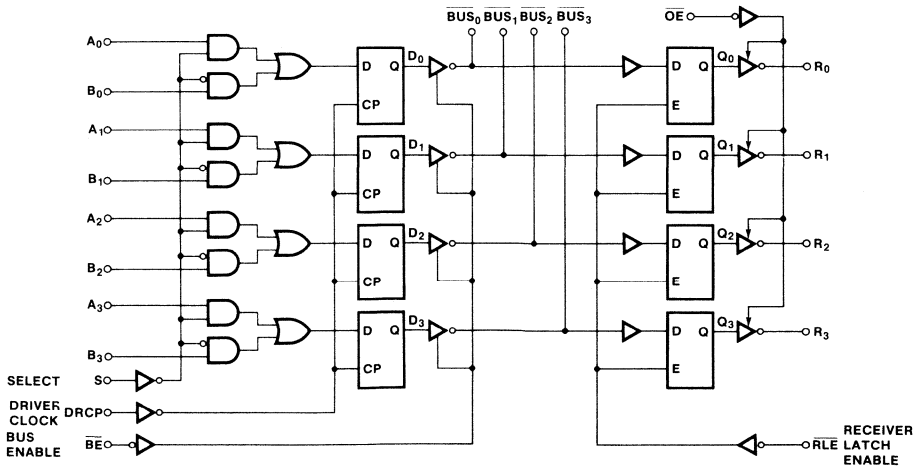
PART NUMBER	PACKAGE	TEMPERATURE RANGE
2915NC	N24	0°C to +70°C
2915JC	J24	0°C to +70°C
2915JM	J24	-55°C to +125°C
2915FM	F24	-55°C to +125°C

the driver is disabled. The V_{OH} and V_{OL} of the bus driver are selected for compatibility with standard and Low-Power Schottky inputs.

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B inputs is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable (\overline{RLE}) input. When the \overline{RLE} input is LOW, the latch is open and the

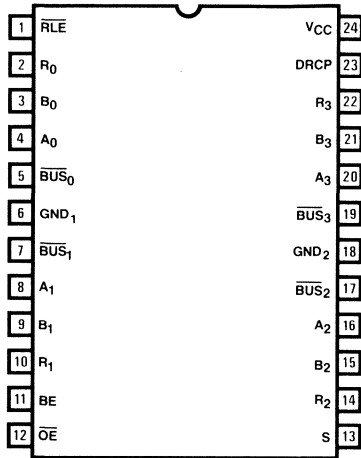
Logic Diagram



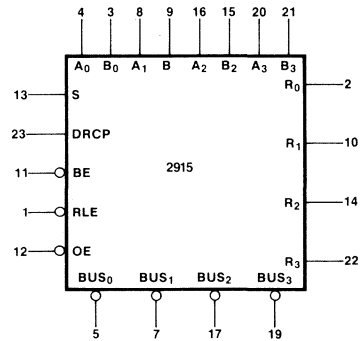
receiver outputs will follow the bus inputs (BUS data inverted and OE LOW). When the \overline{RLE} input is HIGH, the latch will close and retain the present data regardless of the bus input. The four

latches have three-state outputs and are controlled by a buffered common three-state control (\overline{OE}) input. When \overline{OE} is HIGH, the receiver outputs are in the high impedance state.

Pin Configuration



Logic Symbol



VCC = Pin 24
 GND1 = Pin 6
 GND2 = Pin 18

Absolute Maximum Ratings

Storage temperature	-65°C to +150°C
Temperature (ambient) under bias	-55°C to +125°C
Supply voltage to ground potential	-0.5V to +7V
DC voltage applied to outputs for HIGH output state	-0.5V to +VCC max.
DC input voltage	-0.5V to +5.5V
DC output current, into outputs (except bus)	30mA
DC output current, into bus	100mA
DC input current	-30mA to +5.0mA

**Bus Input/Output Characteristics
 Over Operating Temperature Range**

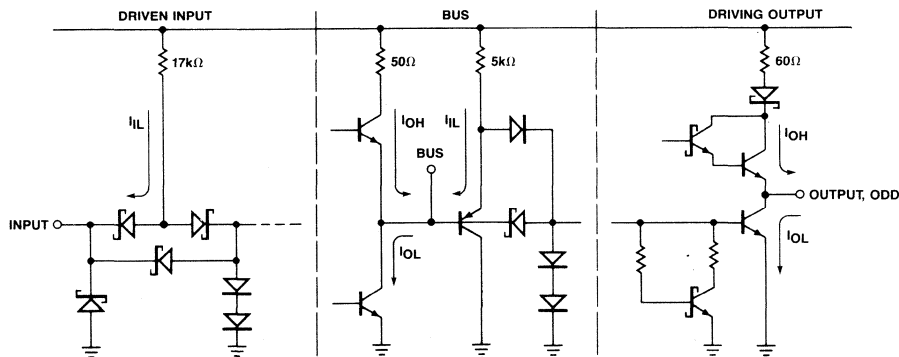
SYMBOL	PARAMETER	TEST CONDITIONS ¹	MILITARY TA = -55°C to +125°C VCC MIN = 4.50V VCC MAX = 5.50V			COMMERCIAL TA = 0°C to +70°C VCC MIN = 4.75V VCC MAX = 5.25V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
VOL	Bus output LOW voltage	VCC = MIN	IOL = 24mA		0.4		0.4		V
			IOL = 40mA		0.5		0.5		
VOH	Bus output HIGH voltage	VCC = MIN	IOH = -20mA		2.4		2.4		V
IO	Bus leakage current (high impedance)	VCC = MAX Bus enable = 2.4V	VO = 0.4V		-200		-200		µA
			VO = 2.4V		50		50		
			VO = 4.5V		100		100		
IOFF	Bus leakage current (power OFF)	VO = 4.5V VCC = 0V			100		100		µA
VIH	Receiver input HIGH threshold	Bus enable = 2.4V	2.0		2.0		2.0		V
VIL	Receiver input LOW threshold	Bus enable = 2.4V			0.8		0.8		V
ISC	Bus output short circuit current	VCC = MAX VO = 0V	-50	-85	-130	-50	-85	-130	mA

Electrical Characteristics Over Recommended Operating Range

SYMBOL	PARAMETER	TEST CONDITIONS ¹	MILITARY $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ V_{CC} MIN = 4.50V V_{CC} MAX = 5.50V MIN TYP ² MAX			COMMERCIAL $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ V_{CC} MIN = 4.75V V_{CC} MAX = 5.25V MIN TYP ² MAX			UNIT	
			MIN	TYP ²	MAX	MIN	TYP ²	MAX		
V_{OH}	Receiver output HIGH voltage	$V_{CC} = \text{MIN}$ $V_{IN} = V_{IL}$ or V_{IH}	$I_{OH} = -1.0\text{mA}$		2.4	3.4			V	
			$I_{OH} = -2.6\text{mA}$				2.4	3.4		
		$V_{CC} = 5.0\text{V}$, $I_{OH} = -100\mu\text{A}$	3.5		3.5					
V_{OL}	Output LOW voltage (except BUS)	$V_{CC} = \text{MIN}$ $V_{IN} = V_{IL}$ or V_{IH}	$I_{OL} = 4.0\text{mA}$			0.27	0.4	0.27	0.4	V
			$I_{OL} = 8.0\text{mA}$			0.32	0.45	0.32	0.45	
			$I_{OL} = 12\text{mA}$			0.37	0.5	0.37	0.5	
V_{IH}	Input HIGH level (except BUS)	Guaranteed input logical HIGH for all inputs			2.0		2.0		V	
V_{IL}	Input LOW level (except BUS)	Guaranteed input logical LOW for all inputs				0.8		0.8	V	
V_I	Input clamp voltage (except BUS)	$V_{CC} = \text{MIN}$, $I_{IN} = -18\text{mA}$				-1.2		-1.2	V	
I_{IL}	Input LOW current	$V_{CC} = \text{MAX}$ $V_{IN} = 0.4\text{V}$	BE, RLE			-0.72		-0.72	mA	
		All other inputs				-0.36		-0.36		
I_{IH}	Input HIGH current (except BUS)	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7\text{V}$				20		20	μA	
I_I	Input HIGH current (except BUS)	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0\text{V}$				100		100	μA	
I_{SC}	Output short circuit current (except BUS)	$V_{CC} = \text{MAX}$			-30	-85	-30	-85	mA	
I_{CC}	Power Supply current	$V_{CC} = \text{MAX}$			60	90	60	90	mA	
I_O	Off-state output current (receiver outputs)	$V_{CC} = \text{MAX}$	$V_O = 2.4\text{V}$			20		20	μA	
			$V_O = 0.4\text{V}$			-20		-20		

7

Input/Output Current Interface Conditions



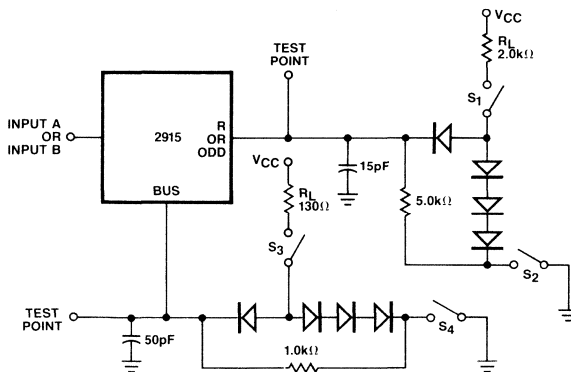
Note: Actual current flow direction shown.

Switching Characteristics
Over Recommended Operating Temperature Range

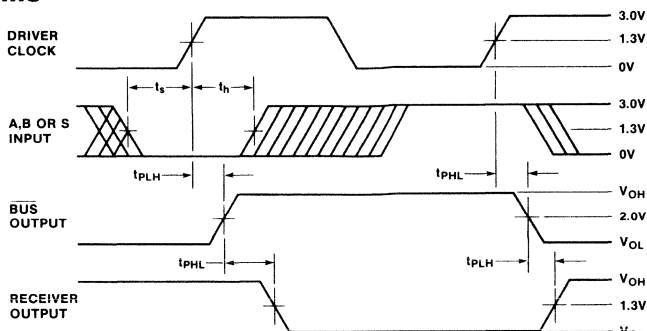
SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY T _A = -55°C to +125°C V _{CC} MIN = 4.50V V _{CC} MAX = 5.50V			COMMERCIAL T _A = 0°C to +70°C V _{CC} MIN = 4.75V V _{CC} MAX = 5.25V			UNIT
			MIN	TYP ²	MAX	MIN	TYP ²	MAX	
t _{PHL}	Driver clock (DRCP) to bus	C _L (bus) = 50pF R _L (bus) = 130Ω	21	36	21	32	ns		
t _{PLH}			21	36	21	32			
t _{ZH} , t _{ZL}	Bus enable (\overline{BE}) to bus		13	26	13	23	ns		
t _{HZ} , t _{LZ}			13	26	13	23			
t _s	Data inputs (A or B)		C _L = 15pF R _L = 2.0kΩ	23		20		ns	
t _h				8.0		6.0			
t _s	Select input (S)	28			25		ns		
t _h		8.0			6.0				
t _{PW}	Driver clock (DRCP) pulse width (HIGH)	20			17		ns		
t _{PLH}	Bus to receiver output (latch enable)	18		30	18	27	ns		
t _{PHL}		18		30	18	27			
t _{PLH}	Latch enable to receiver output	21		30	21	27	ns		
t _{PHL}		21		30	21	27			
t _s	Bus to latch enable (\overline{RE})	17			14		ns		
t _h		6.0			4.0				
t _{ZH} , t _{ZL}	Output control to receiver output	14		26	14	23	ns		
t _{HZ} , t _{LZ}		14	26	14	23				

- Notes: 1. For conditions shown as MIN, or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
 2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
 3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Standard Test Load Circuit



Switching Waveforms



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the BUS to R combinatorial delay.

Function Table

INPUTS							INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
S	A _i	B _i	DRCP	\overline{BE}	\overline{RLE}	\overline{OE}	D _i	Q _i	\overline{BUS}_i	R _i	
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	L	X	H	H	L	Driver output disable and receive data via Bus input
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	Drive Bus

H = HIGH

Z = HIGH Impedance

X = Don't care

i = 0, 1, 2, 3

L = LOW

NC = No change

↑ = LOW-to-HIGH transition

Definition of Functional Terms

"A" word data input, A₀, A₁, A₂, A₃

The "A" word data input into the two input multiplexers of the driver register.

"B" word data input, B₀, B₁, B₂, B₃

The "B" word data input into the two input multiplexers of the driver register.

Select, S

When the select input is LOW, the A data word is applied to the drive register. When the select input is HIGH, the B word is applied to the driver register.

Driver clock pulse, DRCP

Clock pulse for the driver register.

Bus enable, \overline{BE}

When the bus enable is HIGH, the four drivers are in the high impedance state.

Driver outputs and receiver inputs, \overline{BUS}_0 , \overline{BUS}_1 , \overline{BUS}_2 , \overline{BUS}_3

Four driver outputs and receiver inputs (data is inverted).

Receiver outputs, R₀, R₁, R₂, R₃

The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

Receiver latch enable, \overline{RLE}

When RLE is LOW, data on the BUS inputs is passed through the receiver latches. When RLE is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

Output enable, \overline{OE}

When the \overline{OE} input is HIGH, the four three-state receiver outputs are in the high-impedance state.

7

Quad Three-State Bus Transceiver With Interface Logic 2916

Features/Benefits

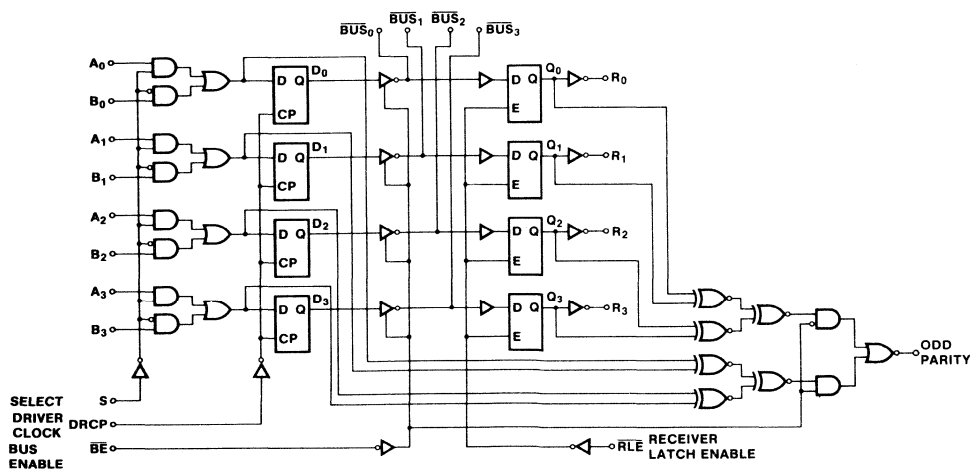
- Quad high-speed LSI bus transceiver
- Three-state bus driver
- Two-port input to D-type register on driver
- Bus driver output can sink 40mA at 0.5V max.
- Internal odd 4-bit parity checker/generator
- Receiver has output latch for pipeline operation
- Receiver outputs sink 12mA
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883
- 3.5V minimum output high voltage for direct interface to MOS microprocessors

Description

The 2916 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches. The device also contains a four-bit odd parity checker/generator.

The LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 40 mA at 0.5V maximum. The bus enable input (\overline{BE}) is used to force the driver outputs to the high-impedance state. When \overline{BE} is HIGH, the driver is disabled.

Logic Diagram



PART NUMBER	PACKAGE	TEMPERATURE RANGE
2916NC	N24	0°C to +70°C
2916JC	J24	0°C to +70°C
2916JM	J24	-55°C to +125°C
2916FM	F24	-55°C to +125°C

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable (\overline{RLE}) input. When the \overline{RLE} input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted). When the \overline{RLE} input is HIGH, the latch will close and retain the present data regardless of the bus input.

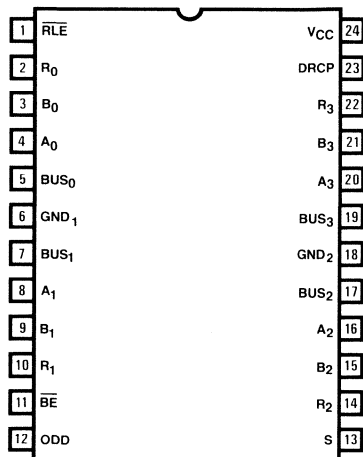
The 2916 features a built-in four-bit odd parity checker/generator. The bus enable input (BE) controls whether the parity output is



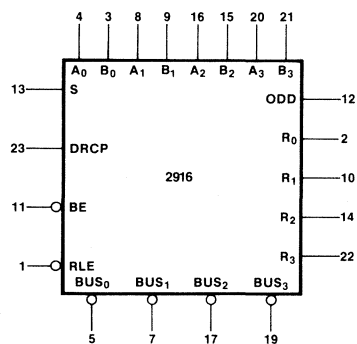
in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A or B field data input to the driver register. When \overline{BE} is HIGH, the parity

output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high impedance state, the BUS parity is checked.

Pin Configuration



Logic Symbol



V_{CC} = Pin 24
 GND_1 = Pin 6
 GND_2 = Pin 18

Absolute Maximum Ratings

Storage temperature	-65°C to +150°C
Temperature (ambient) under bias	-55°C to +125°C
Supply voltage to ground potential	-0.5V to +7V
DC voltage applied to outputs for HIGH output state	-0.5V to V_{CC} max.
DC input voltage	-0.5V to +5.5V
DC output current, into outputs (except bus)	30mA
DC output current, into bus	100mA
DC input current	-30mA to +5.0mA

Bus Input/Output Characteristics Over Operating Temperature Range

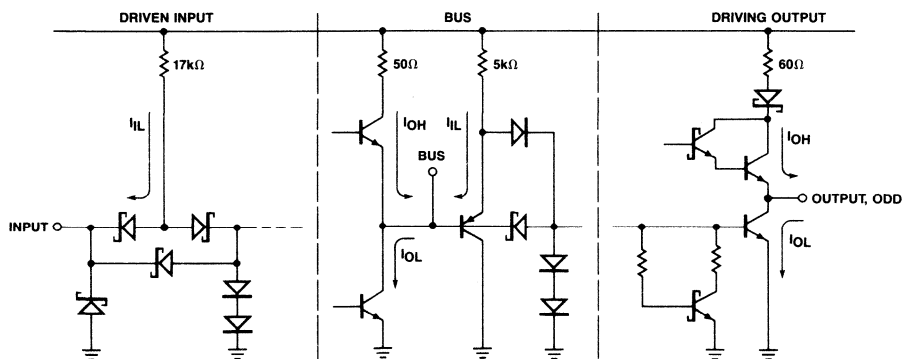
SYMBOL	PARAMETER	TEST CONDITIONS ¹	MILITARY $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ V_{CC} MIN = 4.50V V_{CC} MAX = 5.50V			COMMERCIAL $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ V_{CC} MIN = 4.75V V_{CC} MAX = 5.25V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OL}	Bus output LOW voltage	$V_{CC} = \text{MIN}$	$I_{OL} = 24\text{mA}$		0.4		0.4		V
			$I_{OL} = 40\text{mA}$		0.5		0.5		
V_{OH}	Bus output HIGH voltage	$V_{CC} = \text{MIN}$	$I_{OH} = -20\text{mA}$		2.4		2.4		V
I_O	Bus leakage current (high impedance)	$V_{CC} = \text{MAX}$ Bus enable = 2.4V	$V_O = 0.4\text{V}$		-200		-200		μA
			$V_O = 2.4\text{V}$		50		50		
			$V_O = 4.5\text{V}$		100		100		
I_{OFF}	Bus leakage current (power OFF)	$V_O = 4.5\text{V}$ $V_{CC} = 0\text{V}$			100		100		μA
V_{IH}	Receiver input HIGH threshold	Bus enable = 2.4V	2.0		2.0				V
V_{IL}	Receiver input LOW threshold	Bus enable = 2.4V			0.8		0.8		V
I_{SC}	Bus output short Circuit current	$V_{CC} = \text{MAX}$ $V_O = 0\text{V}$	-50	-85	-130	-50	-85	-130	mA

Electrical Characteristics
Over Recommended Operating Range

SYMBOL	PARAMETER	TEST CONDITIONS ¹	MILITARY T _A = -55°C to +125°C V _{CC} MIN = 4.50V V _{CC} MAX = 5.50V			COMMERCIAL T _A = 0°C to +70°C V _{CC} MIN = 4.75V V _{CC} MAX = 5.25V			UNIT
			MIN	TYP ²	MAX	MIN	TYP ²	MAX	
V _{OH}	Receiver output HIGH voltage	V _{CC} = MIN V _{IN} = V _{IL} or V _{IH}	I _{OH} = -1.0mA		2.4	3.4			V
			I _{OH} = -2.6mA				2.4	3.4	
		V _{CC} = 5.0V, I _{OH} = -100μA			3.5		3.5		
V _{OH}	Parity output HIGH voltage	V _{CC} = MIN, I _{OH} = -660μA V _{IN} = V _{IH} or V _{IL}	2.5	3.4	2.7	3.4		V	
V _{OL}	Output LOW voltage (except bus)	V _{CC} = MIN V _{IN} = V _{IL} or V _{IH}	I _{OL} = 4mA		0.27	0.4	0.27	0.4	V
			I _{OL} = 8mA		0.32	0.45	0.32	0.5	
			I _{OL} = 12mA		0.37	0.5	0.37	0.5	
V _{IH}	Input HIGH level (except bus)	Guaranteed input logical HIGH for all inputs	2.0		2.0			V	
V _{IL}	Input LOW level (except bus)	Guaranteed input logical LOW for all inputs					0.8	V	
V _I	Input clamp voltage (except bus)	V _{CC} = MIN, I _{IN} = -18mA			-1.2		-1.2	V	
I _{IL}	Input LOW current (except bus)	V _{CC} = MAX, V _{IN} = 0.4V	BE, RE	-0.72		-0.72		mA	
			All other inputs	-0.36		-0.36			
I _{IH}	Input HIGH current (except bus)	V _{CC} = MAX, V _{IN} = 2.7V	20		20		μA		
I _I	Input HIGH current (except bus)	V _{CC} = MAX, V _{IN} = 7.0V	100		100		μA		
I _{SC}	Output short circuit current (except bus)	V _{CC} = MAX	-30	-85	-30	-85	mA		
I _{CC}	Power supply currents	V _{CC} = MAX, all inputs = GND	75	110	75	110	mA		



Input/Output Current Interface Conditions



Note: Actual current flow direction shown.

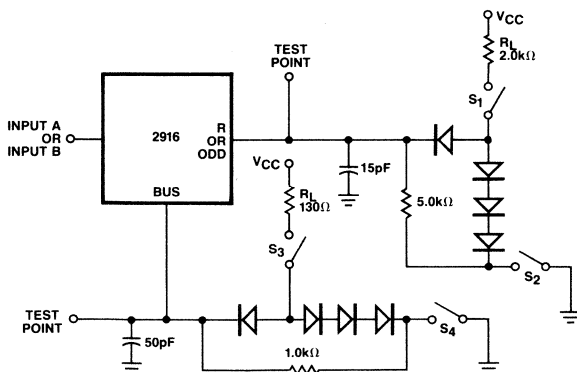
Switching Characteristics
Over Recommended Operating Temperature Range

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY T _A = -55°C to +125°C V _{CC} MIN = 4.50V V _{CC} MAX = 5.50V MIN TYP ² MAX			COMMERCIAL T _A = 0°C to +70°C V _{CC} MIN = 4.75V V _{CC} MAX = 5.25V MIN TYP ² MAX			UNIT
			MIN	TYP ²	MAX	MIN	TYP ²	MAX	
t _{PHL}	Driver clock (DRCP) to bus	C _L (bus) = 50pF R _L (bus) = 130Ω	21	36		21	32	ns	
t _{PLH}			21	36		21	32		
t _{ZH} , t _{ZL}	Bus enable (\overline{BE}) to bus		13	26		13	23	ns	
t _{HZ} , t _{LZ}			13	26		13	23		
t _s	Data inputs (A or B)		23			20		ns	
t _h			8.0			6.0			
t _s	Select inputs (S)		28			25		ns	
t _h			8.0			6.0			
t _{PW}	Clock pulse width (HIGH)		20			17		ns	
t _{PHL}	Bus to receiver output (latch enabled)	C _L = 15pF R _L = 2.0kΩ	18	30		18	27	ns	
t _{PHL}			18	30		18	27		
t _{PLH}	Latch enable to receiver output		21	30		21	27	ns	
t _{PHL}			21	30		21	27		
t _s	Bus to latch enable (\overline{RLE})		17			14		ns	
t _h			6.0			4.0			
t _{PLH}	A or B data to odd parity output (driver enabled)		21	36		21	32	ns	
t _{PHL}			21	36		21	32		
t _{PLH}	Bus to odd parity output (driver inhibited, latch enabled)		21	36		21	32	ns	
t _{PHL}			21	36		21	32		
t _{PLH}	Latch enable (\overline{RLE}) to odd parity output		21	36		21	32	ns	
t _{PHL}			21	36		21	32		

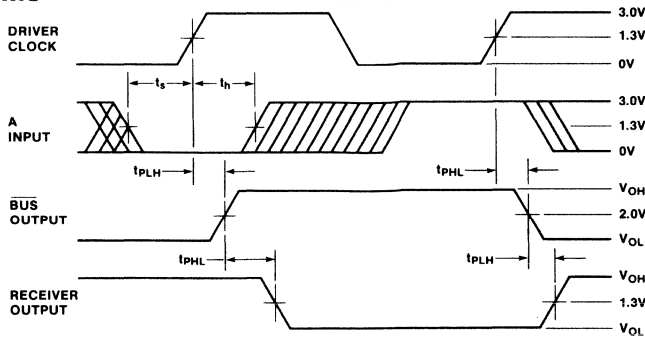
Notes: 1. For conditions shown as MIN, or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.

- Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
- Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Switching Test Circuit



Switching Waveforms



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the \overline{BUS} to R combinatorial delay.

Function Table

INPUTS							INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
S	A _i	B _i	DRCP	\overline{BE}	\overline{RLE}	\overline{OE}	D _i	Q _i	\overline{BUS}_i	R _i	
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	L	X	H	H	L	Driver output disable and receive data via Bus input
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

H = HIGH Z = HIGH Impedance X = Don't care i = 0, 1, 2, 3
 L = LOW NC = No change ↑ = LOW-to-HIGH transition

Definition of Functional Terms

"A" word data input, A₀, A₁, A₂, A₃

The "A" word data input into the two input multiplexers of the driver register.

"B" word data input, B₀, B₁, B₂, B₃

The "B" word data input into the two input multiplexers of the driver register.

Select, S

When the select input is LOW, the A data word is applied to the drive register. When the select input is HIGH, the B word is applied to the driver register.

Driver clock pulse, DRCP

Clock pulse for the driver register.

Bus enable, \overline{BE}

When the bus enable is HIGH, the four drivers are in the high impedance state.

Driver outputs and receiver inputs, \overline{BUS}_0 , \overline{BUS}_1 , \overline{BUS}_2 , \overline{BUS}_3

Four driver outputs and receiver inputs (data is inverted).

Receiver outputs, R₀, R₁, R₂, R₃

The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

Receiver latch enable, \overline{RLE}

When RLE is LOW, data on the BUS inputs is passed through the receiver latches. When RLE is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

Output enable, \overline{OE}

When the \overline{OE} input is HIGH, the four three-state receiver outputs are in the high-impedance state.



Quad Three-State Bus Transceiver With Interface Logic 2917

Features/Benefits

- Quad high-speed LSI bus-transceiver
- Three-state bus driver
- D-type register on driver
- Bus driver output can sink 40mA at 0.5V max
- Internal odd 4-bit parity checker/generator
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12mA
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883
- 3.5V minimum output high voltage for direct interface to MOS microprocessors

Description

The 2917 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches, that feature three-state outputs. The device also contains a four-bit odd parity checker/generator.

The LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 40mA at

PART NUMBER	PACKAGE	TEMPERATURE RANGE
2917NC	N20	0°C to +70°C
2917JC	J20	0°C to +70°C
2917JM	J20	-55°C to +125°C
2917FM*	F20	-55°C to +125°C

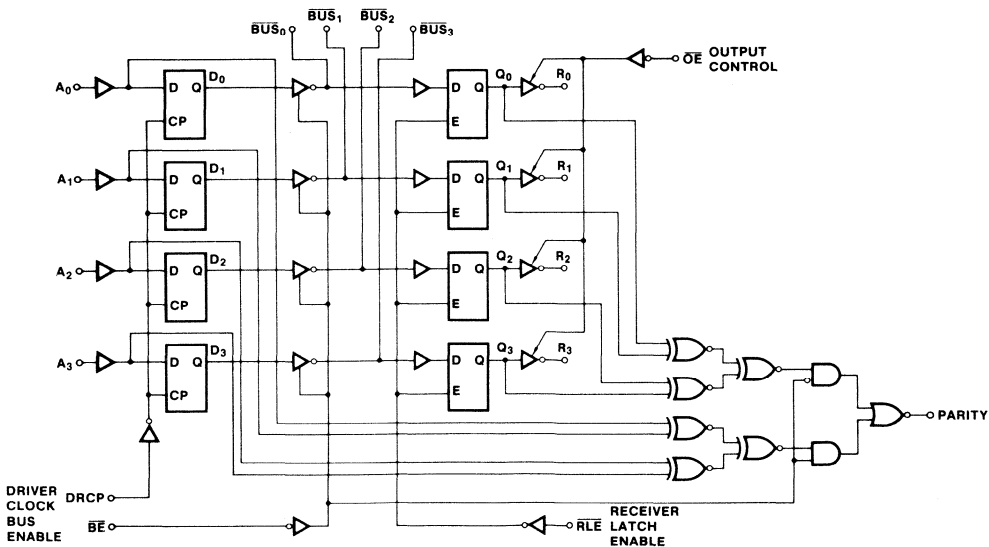
*Available on special order

0.5V maximum. The bus enable input (\overline{BE}) is used to force the driver outputs to the high-impedance state. When \overline{BE} is HIGH, the driver is disabled.

The input register consists of four D-type flip-flops with a buffered common clock. The buffered common clock (DRCP) enters the A_1 data into this drive register on the LOW-to-HIGH transition.

Data from the A input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable (\overline{RLE}) input. When the \overline{RLE} input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and \overline{OE} LOW). When the \overline{RLE} input is HIGH, the latch will close and retain the present

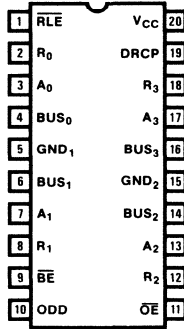
Logic Diagram



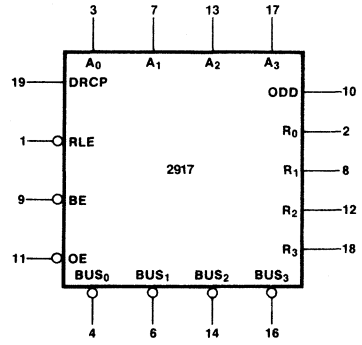
data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control (\overline{OE}) input. When \overline{OE} is HIGH, the receiver outputs are in the high-impedance state. The 2917 features a built in 4-bit odd parity checker/generator. The bus enable input (BE) controls whether the parity output is

in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A field data input to the driver register. When BE is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

Pin Configuration



Logic Symbol



VCC = Pin 20
GND₁ = Pin 5
GND₂ = Pin 15

Absolute Maximum Ratings

Storage temperature	-65°C to +150°C
Temperature (ambient) under bias	-55°C to +125°C
Supply voltage to ground potential	-0.5V to +7V
DC voltage applied to outputs for HIGH output state	-0.5V to +V _{CC} max.
DC input voltage	-0.5V to +5.5V
DC output current, into outputs (except bus)	30mA
DC output current, into bus	100mA
DC input current	-30mA to +5.0mA

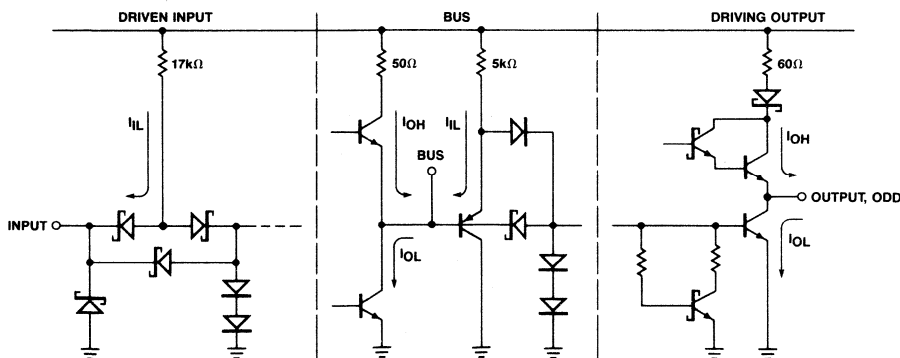
**Bus Input/Output Characteristics
Over Operating Temperature Range**

SYMBOL	PARAMETER	TEST CONDITIONS ¹	MILITARY T _A = -55°C to +125°C V _{CC} MIN = 4.50V V _{CC} MAX = 5.50V			COMMERCIAL T _A = 0°C to +70°C V _{CC} MIN = 4.75V V _{CC} MAX = 5.25V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OL}	Bus output LOW voltage	V _{CC} = MIN	I _{OL} = 24mA		0.4	0.4		V	
			I _{OL} = 40mA		0.5	0.5			
V _{OH}	Bus output HIGH voltage	V _{CC} = MIN	I _{OH} = -20mA		2.4	2.4		V	
I _O	Bus leakage current (high impedance)	V _{CC} = MAX Bus enable = 2.4V	V _O = 0.4V		-200	-200		μA	
			V _O = 2.4V		50	50			
			V _O = 4.5V		100	100			
I _{OFF}	Bus leakage current (power OFF)	V _O = 4.5V V _{CC} = 0V			100	100		μA	
V _{IH}	Receiver input HIGH threshold	Bus enable = 2.4V			2.0	2.0		V	
V _{IL}	Receiver input LOW threshold	Bus enable = 2.4V			0.8	0.8		V	
I _{SC}	Bus output short circuit current	V _{CC} = MAX V _O = 0V	-50	-85	-130	-50	-85	-130	mA

Electrical Characteristics Over Recommended Operating Range

SYMBOL	PARAMETER	TEST CONDITIONS ¹	MILITARY T _A = -55°C to +125°C V _{CC} MIN = 4.50V V _{CC} MAX = 5.50V MIN TYP ² MAX			COMMERCIAL T _A = 0°C to +70°C V _{CC} MIN = 4.75V V _{CC} MAX = 5.25V MIN TYP ² MAX			UNIT
V _{OH}	Receiver output HIGH voltage	V _{CC} = MIN V _{IN} = V _{IL} or V _{IH}	I _{OH} = -1.0mA	2.4	3.4				V
		V _{CC} = 5.0V, I _{OH} = -100μA	I _{OH} = -2.6mA			2.4	3.4		
V _{OH}	Parity output HIGH voltage	V _{CC} = MIN, I _{OH} = -660μA V _{IN} = V _{IH} or V _{IL}		2.5	3.4	2.7	3.4		V
V _{OL}	Output LOW voltage (except bus)	V _{CC} = MIN V _{IN} = V _{IL} or V _{IH}	I _{OL} = 4mA		0.27	0.4	0.27	0.4	V
			I _{OL} = 8mA		0.32	0.45	0.32	0.5	
			I _{OL} = 12mA		0.37	0.5	0.37	0.5	
V _{IH}	Input HIGH level (except bus)	Guaranteed input logical HIGH for all inputs		2.0		2.0		V	
V _{IL}	Input LOW level (except bus)	Guaranteed input logical LOW for all inputs					0.8	V	
V _I	Input clamp voltage (except bus)	V _{CC} = MIN, I _I N = -18mA			-1.2		-1.2	V	
I _{IL}	Input LOW current (except bus)	V _{CC} = MAX, V _{IN} = 0.4V	\overline{BE} , \overline{RE}		-0.72		-0.72	mA	
			All other inputs		-0.36		-0.36		
I _{IH}	Input HIGH current (except bus)	V _{CC} = MAX, V _{IN} = 2.7V		20		20		μA	
I _I	Input HIGH current (except bus)	V _{CC} = MAX, V _{IN} = 7.0V		100		100		μA	
I _{SC}	Output short circuit current (except bus)	V _{CC} = MAX		-30	-85	-30	-85	mA	
I _{CC}	Power supply currents	V _{CC} = MAX, all inputs = GND		63	95	63	95	mA	
I _O	Off-state output current (receiver outputs)	V _{CC} = MAX.	V _O = 2.4V		20		20	μA	
			V _O = 0.4V		-20		-20		

Input/Output Current Interface Conditions



Note: Actual current flow direction shown.

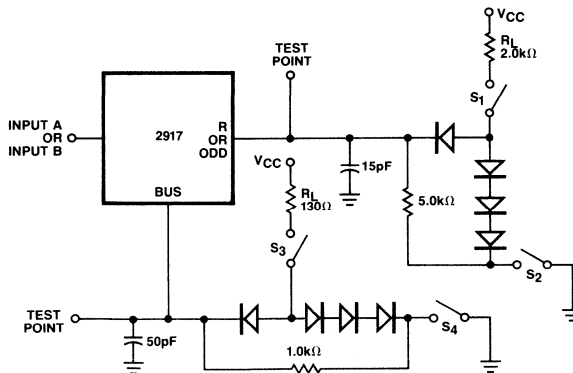
Switching Characteristics

Over Recommended Operating Temperature Range

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ V_{CC} MIN = 4.50V V_{CC} MAX = 5.50V			COMMERCIAL $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ V_{CC} MIN = 4.75V V_{CC} MAX = 5.25V			UNIT
			MIN	TYP ²	MAX	MIN	TYP ²	MAX	
t_{PHL}	Driver clock (DRCP)	$C_L(\text{bus}) = 50\text{pF}$ $R_L(\text{bus}) = 50\Omega$	21	36	21	32	ns		
t_{PLH}	to bus		21	36	21	32			
t_{ZH}, t_{ZL}	Bus enable (\overline{BE}) to bus		13	26	13	23			
t_{HZ}, t_{LZ}			13	26	13	23			
t_s	A data inputs	$C_L = 15\text{pF}$ $R_L = 2.0\text{k}\Omega$	23		20		ns		
t_h			8.0		6.0				
t_{PW}	Clock pulse width (HIGH)		20		17		ns		
t_{PLH}	Bus to receiver output		18	30	18	27	ns		
t_{PHL}	(latch enabled)		18	30	18	27			
t_{PLH}	Latch enable to		21	30	21	27	ns		
t_{PHL}	receiver output		21	30	21	27			
t_s	Bus to latch		17		14		ns		
t_h	enable (\overline{RLE})		6.0		4.0				
t_{PLH}	A data to odd parity		21	36	21	32	ns		
t_{PHL}	out (driver enabled)		21	36	21	32			
t_{PLH}	Bus to odd parity		21	36	21	32	ns		
t_{PHL}	out (driver inhibit)		21	36	21	32			
t_{PLH}	Latch enable (\overline{RLE})		21	36	21	32	ns		
t_{PHL}	to odd parity output		21	36	21	32			
t_{ZH}, t_{ZL}	Output control to output		14	26	14	23	ns		
t_{HZ}, t_{LZ}		14	26	14	23				

- Notes: 1. For conditions shown as MIN, or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
 2. Typical limits are at $V_{CC} = 5.0\text{V}$, 25°C ambient and maximum loading.
 3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Standard Test Load Circuit



Function Table

INPUTS					INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
A _i	DRCP	$\overline{\text{BE}}$	$\overline{\text{RLE}}$	$\overline{\text{OE}}$	D _i	Q _i	BUS _i	R _i	
X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	H	L	L	X	H	H	L	
X	X	X	H	X	X	NC	X	X	Latch received data
L	↑	X	X	X	L	X	X	X	Load driver register
H	↑	X	X	X	H	X	X	X	
X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	H	X	X	X	NC	X	X	X	
X	X	L	X	X	L	X	H	X	Drive Bus
X	X	L	X	X	H	X	L	X	

H = HIGH Z = High Impedance X = Don't Care i = 0, 1, 2, 3
L = LOW NC = No Change ↑ = LOW-to-HIGH Transition

Definition of Functional Terms

Driver clock pulse, DRCP

Clock pulse for the driver register.

Bus enable, $\overline{\text{BE}}$

When the bus enable is LOW, the four drivers are in the high impedance state.

Driver outputs and receiver inputs, BUS₀, BUS₁, BUS₂, BUS₃

Four driver outputs and receiver inputs (data is inverted).

Receiver outputs, R₀, R₁, R₂, R₃

The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

Receiver latch enable, $\overline{\text{RLE}}$

When $\overline{\text{RLE}}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{\text{RLE}}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

Odd parity output, ODD

Generates parity with the driver enabled, checks parity with the driver in the high-impedance state.

Output enable, $\overline{\text{OE}}$

When the $\overline{\text{OE}}$ input is HIGH, the four three-state receiver outputs are in the high-impedance state.

Parity Output Function Table

$\overline{\text{BE}}$	ODD PARITY OUTPUT
L	ODD = A ₀ ⊕ A ₁ ⊕ A ₂ ⊕ A ₃
H	ODD = Q ₀ ⊕ Q ₁ ⊕ Q ₂ ⊕ Q ₃

Quad D Register With Standard and Three-State Outputs 2918

Features/Benefits

- Advanced Schottky technology
- Four D-type flip-flops
- Four standard totem-pole outputs
- Four three-state outputs
- 75 MHz clock frequency

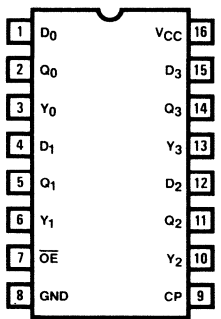
Description

New Schottky circuits such as the 2918 register provide the design engineer with additional flexibility in system configuration—especially with regard to bus structure, organization and speed. The 2918 is a quadruple D-type register with four standard totem pole outputs and four three-state bus-type outputs. The 16-pin device also features a buffered common clock (CP) and a buffered common output control (\overline{OE}) for the Y outputs. Information meeting the set-up and hold requirements on the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock.

The same data as on the Q outputs is enabled at the three-state Y outputs when the "output control" (\overline{OE}) input is LOW. When the \overline{OE} input is HIGH, the Y outputs are in the high-impedance state.

The 2918 register can be used in bipolar microprocessor designs as an address register, status register, instruction register or for various data or microword register applications. Because of the unique design of the three-state output, the device features very short propagation delay from the clock to the Q or Y outputs. Thus, system performance and architectural design can be improved by using the 2918 register. Other applications of 2918 register can be found in microprogrammed display systems, communications systems and most general or special purpose digital signal processing equipment.

Pin Configuration

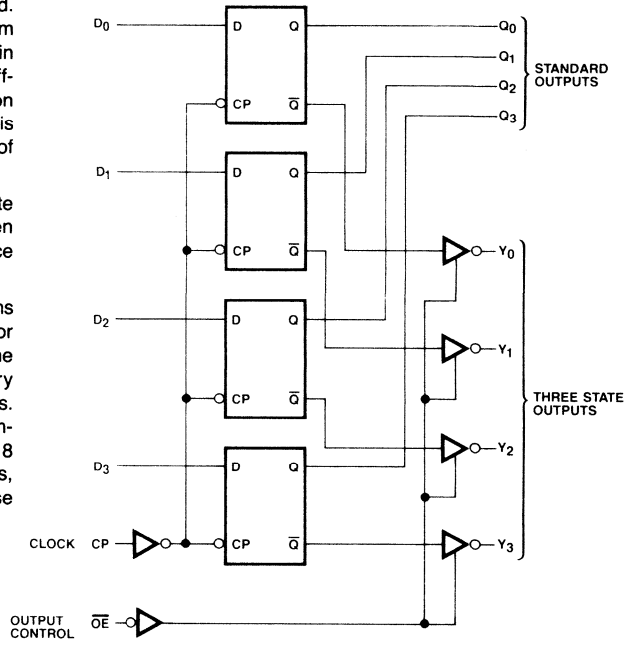


Note: Pin 1 is marked for orientation.

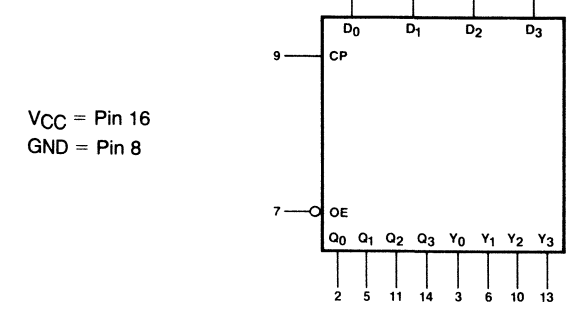
Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE RANGE
2918NC	N16	0°C to +70°C
2918JC	J16	0°C to +70°C
2918JM	J16	-55°C to +125°C
2918FM	F16	+55°C to +125°C

Logic Diagram



Logic Symbol



Absolute Maximum Ratings

Storage temperature	-65°C to +150°C
Temperature (ambient) under bias	-55°C to +125°C
Supply voltage to ground potential continuous	-0.5 V to +7.0 V
DC voltage applied to outputs for high output state	-0.5 V to + V _{CC} max.
DC input voltage	-0.5 V to +7.0 V
DC output current, into outputs	30mA
DC input current	-30mA to +5.0mA

Electrical Characteristics Over Recommended Operating Range

SYMBOL	PARAMETER	TEST CONDITIONS ¹	MIN	TYP ²	MAX	UNIT	
V _{OH}	Output HIGH Voltage	V _{CC} = MIN., V _{IN} = V _{IH} or V _{IL}	Q I _{OH} = -1mA	MIL	2.5	3.4	V
				COM'L	2.7	3.4	
		Y	XM, I _{OH} = -2Ma	2.4	3.4		
			XC, I _{OH} = -6.5mA	2.4	3.4		
V _{OL}	Output LOW Voltage ⁶	V _{CC} = MIN., I _{OL} = 20mA V _{IN} = V _{IH} or V _{IL}			0.5	V	
V _{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			V	
V _{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	V	
V _I	Input Clamp Voltage	V _{CC} = MIN., I _{IN} = -18mA			-1.2	V	
I _{IL} ³	Input LOW Current	V _{CC} = MAX., V _{IN} = 0.5V			-2.0	mA	
I _{IH} ³	Input HIGH Current	V _{CC} = MAX., V _{IN} = 2.7V			50	μA	
I _I	Input HIGH Current	V _{CC} = MAX., V _{IN} = 5.5V			1.0	mA	
I _O	Y Output Off-State Leakage Current	V _{CC} = MAX.	V _O = 2.4V		50	μA	
			V _O = 0.4V		-50		
I _{SC}	Output Short Circuit Current ⁴	V _{CC} = MAX.	-40		-100	mA	
I _{CC}	Power Supply Current	V _{CC} = MAX.		80	130	mA	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical limits are at V_{CC} = 5.0V, T_A = 25°C ambient and maximum loading.

3. Actual input currents = Unit Load Current x Input Load Factor (see Loading Rules).

4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

5. I_{CC} is measured with all inputs at 4.5V and all outputs open.

6. Measured on Q outputs with Y outputs open. Measured on Y outputs with Q outputs open.

Switching Characteristics $T_A = +25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$

SYMBOL	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
t _{PLH}	Clock to Q Output	C _L = 15pF		6.0	9.0	ns	
t _{PHL}				8.5	13		
t _{pw}	Clock Pulse Width		HIGH	7.0		ns	
			LOW	9.0			
t _s	Data			5.0		ns	
t _h	Data			3.0		ns	
t _{PLH}	Clock to Y Output ($\overline{\text{OE}}$ LOW)				6.0	9.0	ns
t _{PHL}					8.5	13	
t _{ZH}	Output Control to Output		C _L = 15pF		12.5	19	ns
t _{ZL}					12	18	
t _{HZ}		C _L = 5.0pF		4.0	6.0		
t _{LZ}				7.0	10.5		
f _{max}	Maximum Clock Frequency	C _L = 15pF	75	100		MHz	

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Functional Table

INPUTS			OUTPUTS		NOTES
\overline{OE}	CLOCK CP	D	Q	Y	
H	L	X	NC	Z	—
H	H	X	NC	Z	—
H	↑	L	L	Z	—
H	↑	H	H	Z	—
L	↑	L	L	L	—
L	↑	H	H	H	—
L	—	—	L	L	1
L	—	—	H	H	1

L = LOW

H = HIGH

X = Don't care

NC = No change

↑ = LOW to HIGH transition

Z = High impedance

Note: 1. When OE is LOW, the Y output will be in the same logic state as the Q output.

Definition of Functional Terms

Data inputs, D_i

The four data inputs to the register.

Data outputs, Q_i

The four data outputs of the register with standard totem-pole active pull-up outputs. Data is passed non-inverted.

Three-state data outputs, Y_i

The four three-state data outputs of the register. When the three-state outputs are enabled, data is passed non-inverted. A HIGH on the "output control" input forces the Y_i outputs to the high impedance state.

Clock, CP

The buffered common clock for the register. Enters data on the LOW-to-HIGH transition.

Output Control, OE

When the OE input is HIGH, the Y_i outputs are in the high impedance state. When the OE input is LOW, the TRUE register data is present at the Y_i outputs.

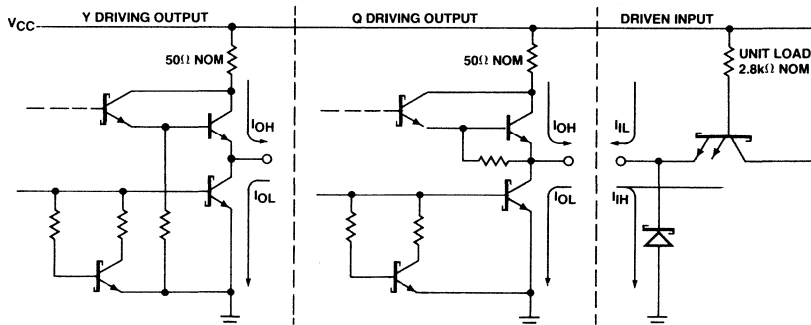
Loading Rules (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out	
			Output HIGH	Output LOW
D_0	1	1	—	—
Q_0	2	—	20	10*
Y_0	3	—	40/130	10*
D_1	4	1	—	—
Q_1	5	—	20	10*
Y_1	6	—	40/130	10*
\overline{OE}	7	1	—	—
GND	8	—	—	—
CP	9	1	—	—
Y_2	10	—	40/130	10*
Q_2	11	—	20	10*
D_2	12	1	—	—
Y_3	13	—	40/130	10*
Q_3	14	—	20	10*
D_3	15	1	—	—
V_{CC}	16	—	—	—

A Schottky TTL Unit Load is defined as $50\mu\text{A}$ measured at 2.7V HIGH and -2.0mA measured at 0.5V LOW.

*Fan-out on each Q_i and Y_i output pair should not exceed 15 unit loads (30mA) for $i = 0, 1, 2, 3$.

Schottky Input/Output Current Interface Conditions



Note: Actual current flow direction shown.

Quad D Register With Standard And Three-State Outputs 29LS18

Features/Benefits

- Low-power Schottky version of the popular 2918
- Four standard totem-pole outputs
- Four three-state outputs
- Four D-type flip-flops
- 100% product assurance screening to MIL-STD-883 requirements

PART NUMBER	PACKAGE	TEMPERATURE RANGE
29LS18NC	N16	0°C to +70°C
29LS18JC	J16	0°C to +70°C
29LS18JM	J16	-55°C to +125°C
29LS18FM	F16	+55°C to +125°C

Description

The 29LS18 consists of four D-type flip-flops with a buffered common clock. Information meeting the set-up and hold requirements on the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock.

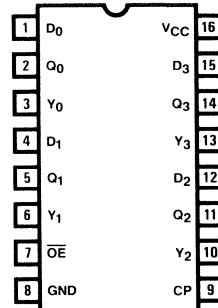
The same data as on the Q outputs is enabled at the three-state Y outputs when the "output control" (OE) input is LOW. When the OE input is HIGH, the Y outputs are in the high impedance state.

The 29LS18 is a 4-bit, high-speed register intended for use in real-time signal processing systems. The standard outputs are used in a recursive algorithm, and the three-state outputs provide access to a data bus to dump the results after a number of iterations.

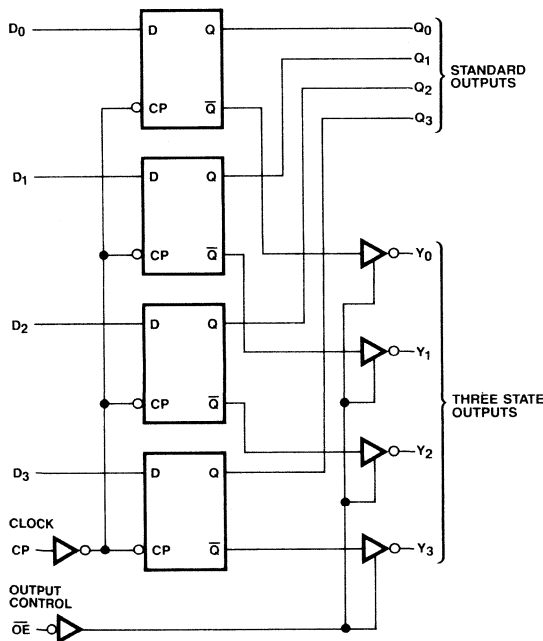
The device can also be used as an address register or status register in computers or computer peripherals.

Likewise, the 29LS18 is also useful in certain display applications where the standard outputs can be decoded to drive LED's (or equivalent) and the three-state outputs are bus organized for occasional interrogation of the data as displayed.

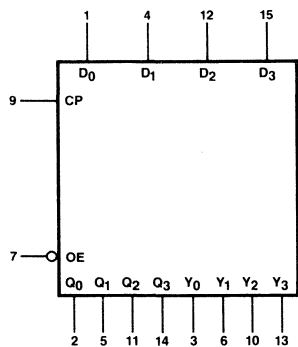
Pin Configuration



Logic Diagram



Logic Symbol



VCC = Pin 16
GND = Pin 8



Absolute Maximum Ratings

Storage temperature	-65°C to +150°C
Temperature (ambient) under bias	-55°C to +125°C
Supply voltage to ground potential continuous	-0.5 V to +7.0 V
DC voltage applied to outputs for high output state	-0.5 V to + V _{CC} max.
DC input voltage	-0.5 V to +7.0 V
DC output current, into outputs	30mA
DC input current	-30mA to +5.0mA

Electrical Characteristics Over Recommended Operating Range

SYMBOL	PARAMETER	TEST CONDITIONS ¹	MILITARY T _A = -55°C to +125°C V _{CC} = 5.0V ± 10% MIN = 4.50V, MAX = 5.50V			COMMERCIAL T _A = 0°C to +70°C V _{CC} = 5.0V ± 5% MIN = 4.75V, MAX = 5.25V			UNIT
			MIN	TYP ²	MAX	MIN	TYP ²	MAX	
V _{OH}	Output HIGH voltage	V _{CC} = MIN V _{IN} = V _{IH} or V _{IL}	Q, I _{OH} = -660μA	2.5	3.4	2.7	3.4	V	
			Y, I _{OH} = -1.0mA	2.4	3.4				
			Y, I _{OH} = 2.6mA			2.4	3.4		
V _{OL}	Output LOW voltage	V _{CC} = MIN V _{IN} = V _{IH} or V _{IL}	I _{OL} = 4.0mA		0.4		0.4	V	
			I _{OL} = 8.0mA		0.45		0.45		
			I _{OL} = 12mA		0.5		0.5		
V _{IH}	Input HIGH level	Guaranteed input logical HIGH voltage for all inputs	2.0		2.0		V		
V _{IL}	Input LOW level	Guaranteed input logical LOW voltage for all inputs		0.7		0.8	V		
V _I	Input clamp voltage	V _{CC} = MIN, I _{IN} = -18mA		-1.5		-1.5	V		
I _{IL}	Input LOW current	V _{CC} = MAX, V _{IN} = 0.4V		-0.36		-0.36	mA		
I _{IH}	Input HIGH current	V _{CC} = MAX, V _{IN} = 2.7V		20		20	μA		
I _I	Input HIGH current	V _{CC} = MAX, V _{IN} = 7.0V		0.1		0.1	mA		
I _{OZ}	Off-state (high impedance) output current	V _{CC} = MAX	V _O = 0.4V		-20		-20	μA	
			V _O = 2.4V		20		20		
I _{SC}	Output short circuit current ³	V _{CC} = MAX	-15	-85	-15	-85	mA		
I _{CC}	Power supply current ⁴	V _{CC} = MAX		17	28		17	28	mA

NOTES: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.

3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

4. I_{CC} is measured with all inputs at 4.5V and all outputs open.

Switching Characteristics $T_A = +25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t_{PLH}	Clock to Q_i	$C_L = 15\text{pF}$ $R_L = 2.0\text{k}\Omega$		18	27	ns	
t_{PHL}				18	27		
t_{PLH}	Clock to Y_i (\overline{OE} LOW)			18	27	ns	
t_{PHL}				18	27		
t_{pw}	Clock Pulse Width		LOW	18		ns	
			HIGH	15			
t_s	Data			15		ns	
t_h	Data			5.0		ns	
t_{ZH}	\overline{OE} to Y_i				7.0	11	ns
t_{ZL}					8	12	
t_{HZ}	\overline{OE} to Y_i	$C_L = 5.0\text{pF}$ $R_L = 2.0\text{k}\Omega$		14	21	ns	
t_{LZ}				12	18		
f_{max}	Maximum Clock Frequency ¹		35	50		MHz	

**Switching Characteristics
Over Operating Range²**

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL $T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 5\%$		MILITARY $T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		UNIT	
			MIN	MAX	MIN	MAX		
t_{PLH}	Clock to Q_i	$C_L = 50\text{pF}$ $R_L = 2.0\text{k}\Omega$		38		45	ns	
t_{PHL}				38		45		
t_{PLH}	Clock to Y_i (\overline{OE} LOW)			35		40	ns	
t_{PHL}				35		40		
t_{pw}	Clock Pulse Width		LOW	20		20	ns	
			HIGH	20		20		
t_s	Data			15		15	ns	
t_h	Data			5.0		5.0	ns	
t_{ZH}	\overline{OE} to Y_i				15		17	ns
t_{ZL}					16		17	
t_{HZ}	\overline{OE} to Y_i	$C_L = 5.0\text{pF}$ $R_L = 2.0\text{k}\Omega$		27		30	ns	
t_{LZ}				24		30		
f_{max}	Maximum Clock Frequency ¹		30			MHz		

- NOTES: 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r , t_f , pulse width or duty cycle.
2. AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

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Functional Table

INPUTS			OUTPUTS		NOTES
\overline{OE}	CLOCK CP	D	Q	Y	
H	L	X	NC	Z	—
H	H	X	NC	Z	—
H	↑	L	L	Z	—
H	↑	H	H	Z	—
L	↑	L	L	L	—
L	↑	H	H	H	—
L	—	—	L	L	1
L	—	—	H	H	1

L = LOW

H = HIGH

X = Don't care

NC = No change

↑ = LOW to HIGH transition

Z = High impedance

Note: 1. When \overline{OE} is LOW, the Y output will be in the same logic state as the Q output.

Definition of Functional Terms

Data inputs, D_i

The four data inputs to the register.

Data outputs, Q_i

The four data outputs of the register with standard totem-pole active pull-up outputs. Data is passed non-inverted.

Three-state data outputs, Y_i

The four three-state data outputs of the register. When the three-state outputs are enabled, data is passed non-inverted. A HIGH on the "output control" input forces the Y_i outputs to the high-impedance state.

Clock, CP

The buffered common clock for the register. Enters data on the LOW-to-HIGH transition.

Output Control, \overline{OE}

When the \overline{OE} input is HIGH, the Y_i outputs are in the high impedance state. When the \overline{OE} input is LOW, the TRUE register data is present at the Y_i outputs.

Quad Register With Two Independently Controlled Three-State Outputs 2919

Features/Benefits

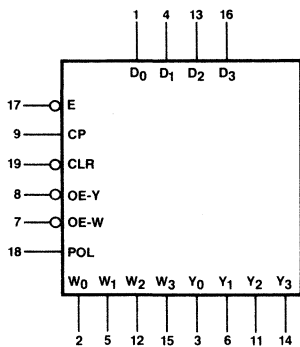
- Two sets of fully buffered three-state outputs
- Four D-type flip-flops
- Polarity control on one set of outputs
- Buffered common clock enable
- Buffered common asynchronous clear
- Separate buffered common output enable for each set of outputs
- 100% product assurance screening to MIL-STD-883 requirements

Description

The 29LS19 consists of four D-type flip-flops with a buffered common clock enable. Information meeting the set-up and hold time requirements of the D inputs is transferred to the flip-flop outputs on the LOW-to-HIGH transition of the clock. Data on the Q outputs of the flip-flops is enabled at the three-state outputs when the output control (\overline{OE}) input is LOW. When the appropriate \overline{OE} input is HIGH, the outputs are in the high impedance state. Two independent sets of outputs—W and Y—are provided such that the register can simultaneously and independently drive two buses. One set of outputs contains a polarity control such that the outputs can either be inverting or non-inverting.

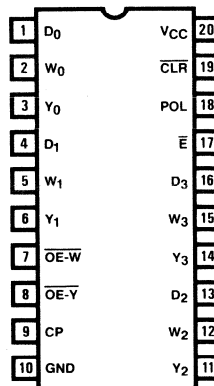
The device also features an active LOW asynchronous clear. When the clear input is LOW, the Q output of the internal flip-flops are forced LOW independent of the other inputs. The 29LS19 is packaged in a space saving (0.3-inch row spacing) 20-pin package.

Logic Symbol

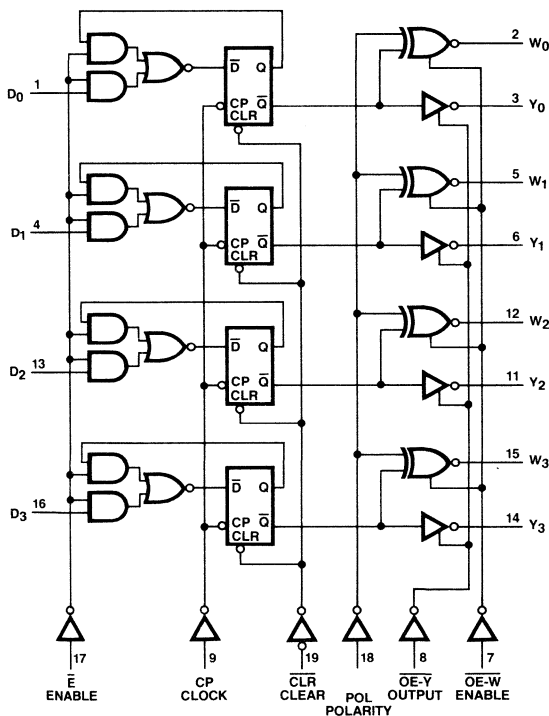


V_{CC} = Pin 20
GND = Pin 10

Pin Configuration



Logic Diagram



Absolute Maximum Ratings

Storage temperature	-65°C to +150°C
Temperature (ambient) under bias	-55°C to +125°C
Supply voltage to ground potential continuous	-0.5 V to +7.0 V
DC voltage applied to outputs for high output state	-0.5 V to + V _{CC} max.
DC input voltage	-0.5 V to +7.0 V
DC output current, into outputs	30mA
DC input current	-30mA to +5.0mA

Electrical Characteristics Over Recommended Operating Range

SYMBOL	PARAMETER	TEST CONDITIONS ¹	MILITARY T _A = -55°C to +125°C V _{CC} = 5.0V ± 10% MIN = 4.50V, MAX = 5.50V		COMMERCIAL T _A = 0°C to +70% V _{CC} = 5.0V ± 5% MIN = 4.75V, MAX = 5.25V			UNIT
			MIN	TYP ² MAX	MIN	TYP ² MAX		
V _{OH}	Output HIGH voltage	V _{CC} = MIN V _{IN} = V _{IH} or V _{IL}	I _{OH} = -1.0mA	2.4	3.4			V
			I _{OH} = -2.6mA			2.4	3.4	
V _{OL}	Output LOW voltage	V _{CC} = MIN V _{IN} = V _{IH} or V _{IL}	I _{OL} = 4.0mA			0.4	0.4	V
			I _{OL} = 8.0mA			0.45	0.45	
			I _{OL} = 12mA			0.5	0.5	
V _{IH}	Input HIGH level	Guaranteed input logical HIGH voltage for all inputs	2.0		2.0		V	
V _{IL}	Input LOW level	Guaranteed input logical LOW voltage for all inputs		0.7		0.8	V	
V _I	Input clamp voltage	V _{CC} = MIN, I _{IN} = -18mA		-1.5		-1.5	V	
I _{IL}	Input LOW current	V _{CC} = MAX, V _{IN} = 0.4V		-0.36		-0.36	mA	
I _{IH}	Input HIGH current	V _{CC} = MAX, V _{IN} = 2.7V		20		20	μA	
I _I	Input HIGH current	V _{CC} = MAX, V _{IN} = 7.0V		0.1		0.1	mA	
I _{OZ}	Off-state (high-impedance) output current	V _{CC} = MAX	V _O = 0.4V			-20	-20	μA
			V _O = 2.4V			20	20	
I _{SC}	Output short circuit current ³	V _{CC} MAX	-15	-85	-15	-85	mA	
I _{CC}	Power supply current ⁴	V _{CC} = MAX		24	36	24	39	mA

NOTES: 1. For conditions shown as MIN, or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical limits are V_{CC} = 5.0V, 25°C ambient and maximum loading.

3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Switching Characteristics**TA +25°C, VCC = 5.0V**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PHL}	Clock to Y _i	C _L = 15pF R _L = 2.0kΩ		22	33	ns
t _{PHL}				20	30	
t _{PHL}	Clock to W _i (either polarity)			24	36	ns
t _{PHL}				24	36	
t _{PHL}	Clear to Y _i			29	43	ns
t _{PLH}	Clear to W _i			25	37	ns
t _{PHL}			30	45		
t _{PLH}	Polarity to W _i			23	34	ns
t _{PHL}			25	37		
t _{pw}	Clear			18		ns
t _{pw}	Clock pulse width		LOW	15		ns
			HIGH	18		
t _s	Data		15		ns	
t _n	Data		5		ns	
t _s	Data enable		20		ns	
t _n	Data enable		0		ns	
t _s	Set-up time, clear recovery (inactive) to clock		20	15	ns	
t _{ZH}	Output enable to W or Y			11	17	ns
t _{ZL}				13	20	
t _{HZ}	Output enable to W or Y	C _L = 5.0pF		13	20	ns
t _{LZ}		R _L = 2.0kΩ		11	17	
f _{max}	Maximum clock frequency ¹	C _L = 15pF R _L = 2.0kΩ	35	45		MHz

NOTES: 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.
2. 4AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.



Switching Characteristics
Over Operating Range²

SYMBOL	PARAMETER		TEST CONDITIONS	COMMERCIAL		MILITARY		UNIT
				$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 5\%$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		
				MIN	MAX	MIN	MAX	
t _{PLH}	Clock to Y _i		C _L = 50pF R _L = 2.0kΩ		39		42	ns
t _{PHL}					39		45	
t _{PLH}	Clock to W _i				41		43	ns
t _{PHL}	(Either polarity)				44		48	
t _{PHL}	Clear to Y _i				52		58	ns
t _{PLH}	Clear to W _i				42		43	ns
t _{PHL}					51		53	
t _{PLH}	Polarity to W _i				41		45	ns
t _{PHL}					42		44	
t _{pw}	Clear				20		20	ns
t _{pw}	Clock	LOW			20		20	ns
		HIGH			20		20	
t _s	Data				15		15	ns
t _h	Data				10		10	ns
t _s	Data enable				25		25	ns
t _h	Data enable				0		0	ns
t _s	Set-up time, clear recovery (inactive) to clock				23		24	ns
t _{ZH}	Output enable to W _i or Y _i				24		27	ns
t _{ZL}					29		35	
t _{HZ}	Output enable to W _i or Y _i			C _L = 5.0pF R _L = 2.0kΩ		33		45
t _{LZ}					22		26	
f _{max}	Maximum clock frequency ¹		C _L = 50pF R _L = 2.0kΩ	30		25	MHz	

NOTES: 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.
2. 4AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Function Table

FUNCTION	INPUTS							INTERNAL	OUTPUTS	
	CP	D _i	\bar{E}	\bar{CLR}	POL	$\overline{OE-W}$	$\overline{OE-Y}$	Q	W _i	Y _i
Output Three-State Control	X	X	X	X	X	H	L	NC	Z	Enabled
	X	X	X	X	X	L	H	NC	Enabled	Z
	X	X	X	X	X	H	H	NC	Z	Z
	X	X	X	X	X	L	L	NC	Enabled	Enabled
W _i Polarity	X	X	X	X	L	L	L	NC	Non-Inverting	Non-Inverting
	X	X	X	X	H	L	L	NC	Inverting	Non-Inverting
Asynchronous Clear	X	X	X	L	L	L	L	L	L	L
	X	X	X	L	H	L	L	L	H	L
Clock Enabled	↑	X	H	H	X	X	X	NC	NC	NC
	↑	L	L	H	L	L	L	L	L	L
	↑	L	L	H	H	L	L	L	H	L
	↑	H	L	H	L	L	L	H	H	H
	↑	H	L	H	H	L	L	H	L	H

L LOW
H = HIGH
Z = High Impedance

X = Don't Care
NC = No Change
↑ = LOW to HIGH Transition

Definition of Functional Terms

Data lines, D_i

Any of the four D flip-flops data lines.

Clock enable \bar{E}

When LOW, the data is entered into the register on the next clock LOW-to-HIGH transition. When HIGH, the data in the register remains unchanged, regardless of the data in.

Clock pulse, CP

Data is entered into the register on the LOW-to-HIGH transition.

Output enable, $\overline{OE-W}$, $\overline{OE-Y}$

When \overline{OE} is LOW, the register is enable to the output. When HIGH, the output is in the high-impedance state. The $\overline{OE-W}$

controls the W set of outputs, and $\overline{OE-Y}$ controls the Y set.

Output lines, Y_i

Any of the four non-inverting three-state output lines.

Outputs with polarity control, W_i

Any of the four three-state outputs with polarity control.

Polarity Control, POL

The W_i outputs will be non-inverting when POL is LOW, and when it is HIGH, the outputs are inverting.

Asynchronous clear, \bar{CLR}

When \bar{CLR} is LOW, the internal Q flip-flops are reset to LOW.

4-Bit Bipolar Microprocessor-slice 6701

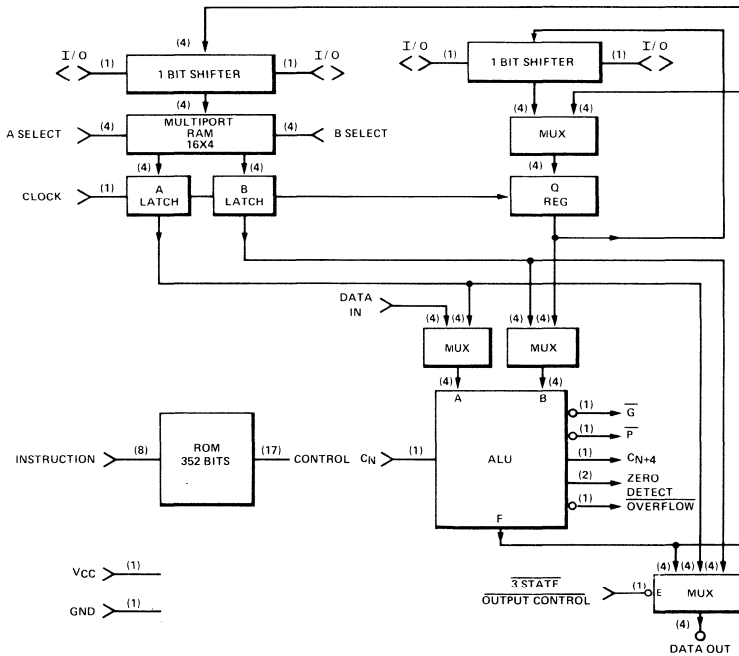
Features/Benefits

- Complete 4-Bit Bipolar LSI Processor Slice on a Single Chip.
- Replaces 25 TTL MSI Packages and Saves 5.5 Watts.
- 1000 Gate Complexity Schottky LSI – Single Layer Metal.
- 36 Instructions – Arithmetic, Logic, and Shifting Capability with Overflow Detection. Active High or Active Low Logic.
- 16 Directly Addressable, Two-Port, General Purpose Accumulators – Full 2 Address Capability, Some 3 Register Operations
- A Separate Q-Register Useful as a Scratchpad or Accumulator Extension. Direct Data in and Accumulator Operations.
- Separate Low Fan in Input Bus and 3 State Output Bus.
- Expandable to Handle N Bit Words with Full Carry Look-Ahead.
- 175 ns Cycle (6701) Which Can Perform Multiple Nano-instructions such as Subtract, Shift, and Store in One Cycle.

Applications

- The Ideal Product for Upgrading or Replacing Existing Central Processing Units and Maintaining the Existing Software. The 6701 can be Microprogrammed to Efficiently Emulate (Simulate) Most Machines.
- Hard Wired Controllers – Tape and Disk Controllers – Data Concentrators.
- Point of Sale Terminals, Special Purpose Processors.
- Process and Machine Control.
- Word Processing and Navigation Systems.
- Intelligent Terminals and Game Machines.
- Traffic Control and Communications Systems.

Block Diagram



Note: The numbers in parentheses are the numbers of signal lines.



Expandable 4 Bit Slice—40 Pin Pkg.

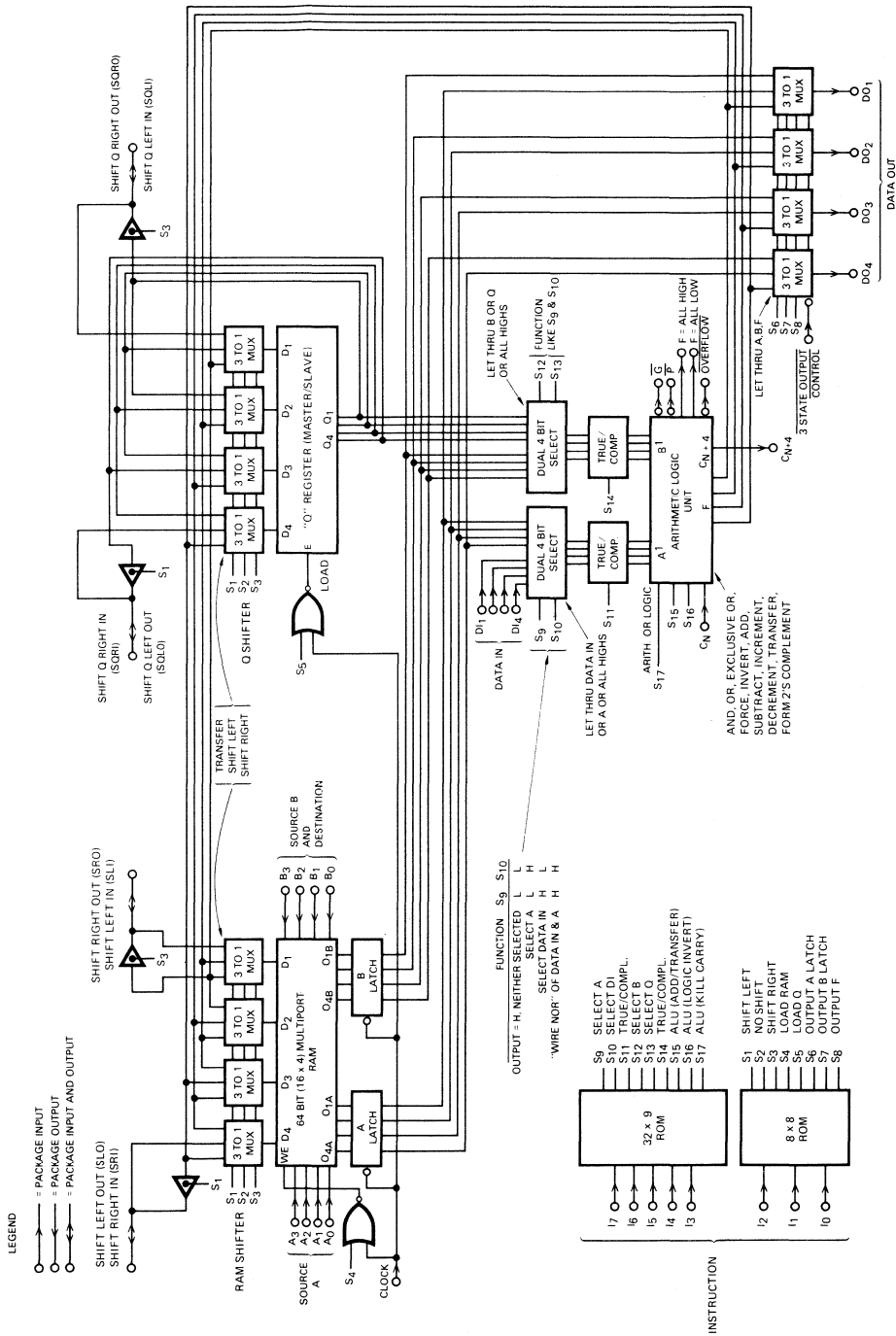


Figure 1

Introduction

General Description

The 6701 is designed to be used as a 4-bit processor slice of a conventional central processing unit (C.P.U.). It can also be used in peripheral controllers, (tape, disk, etc.,) or as the heart of a microprocessor, terminal, or computer. It is a single chip bipolar LSI device which replaces more than 1000 TTL gates.

The two address capability (ability to work on two accumulators at once) and the powerful nano-instructions permit design of sub 1 microsecond cycle time hard wired C.P.U.'s or efficient emulation (imitation) of conventional machines using off chip ROMs for microprogramming.

The 6701 will handle the data flow section of most computers since it is expandable to handle any word length in increments of 4 bits without significant speed degradation (look-ahead outputs are available). The 16 on-chip general purpose accumulators implement the type of C.P.U. usually found only in high performance top of the line 16-bit minicomputers or 24 or 32-bit computers. It can be thought of as a general purpose 4-bit register and arithmetic logic unit with a separate A operand, B operand, data-in, and data-out ports. Additional accumulators or registers if required can be added with off chip packages tied to the data in pins.

TTL Equivalent

The 6701 is similar in function to the 25 TTL MSI packages listed below. It saves 375 I/O pins, 5.6 watts and 30 square inches of board area.

TABLE 1

Function	TTL #	#14 Pin or #16 Pin Pkgs.	#24 Pin Pkgs.	Advertised Gate Complexity (Each Pkg.)	Gate Complexity Total	Typical Power Each (Watts)	Total Power (Watts)
32 x 9 & 8 x 8 ROMs	7488	3		70	210	.50	1.50
16 x 4 Multiport RAM	74172		4	110*	440	.56	2.24
Arithmetic Logic Unit	74181		1	75	75	.55	.55
Storage Latches	7475	2		28	56	.16	.32
J-K Flip Flop (Q Reg)	74107	2		22	44	.10	.20
4 to 1 MUX	74153	6		16	96	.20	1.20
O/I True Complement	74H87	2		18	36	.27	.54
Dual 4-Bit Select	74157	2		15	30	.15	.30
Quad 2 to 1 MUX with 3 State Outputs	74S257	2		15	30	.30	.60
3 State Buffer	DM8094	1		5	5	.18	.18
Totals		20	5		1022		6.63

*The 74172 is advertised at 201 gate complexity but we are using only 2 of the 3 address capability, hence we have counted it as 110 gates.

Process and Packaging

The 6701 is manufactured by an advanced Schottky bipolar single layer metal process. The chip requires only 5 volts and ground and all inputs and outputs are totally TTL compatible. The chip is packaged in a standard 40-pin dual in-line ceramic package.

Power

The chip is designed to dissipate maximum power at low temperature. The power is minimum at high temperature.

Performance

A single 6701 can execute one instruction every 175ns. The instructions are more complex than normal micro-instructions permitting multiple operations in one cycle without timing problems.

Operation

See Figure 1 – Expandable 4-Bit Slice

Block Diagram

A detailed block diagram of the chip is shown in Figure 1. Note the legend used in the upper left hand corner for package inputs and outputs. The logic and control ones are shown as they are implemented on the chip even though fewer control inputs might be required by discrete logic devices. The dual 4-bit selects, at the input to the arithmetic logic unit, for example, have two "S" input control lines rather than the 74157 TTL equivalent which has one control line for letting through the left four bits or the right four bits on the output 4 bits.

ROM (Lower Left Corner)

Two on chip ROMs (352 bits total) are used to translate the eight (8) instruction lines I_0 to I_7 into 17 on chip control lines (labeled S_1 through S_{17}) which open and close data paths required to execute an instruction.

Multiport RAM (Upper Left Corner)

A 16 word by 4-bit multiple port memory is used to fetch two operands at the same time. The RAM is double decoded (4 A-address pins and 4 B-address pins and has one set of 64 storage cells). We could, for example, read from 0101 on the A address (file #5) and read from 0001 on the B address (file #1) at the same time. The B side of the RAM can be read out or written into independent of the address on the A side. The A side can only be read. The RAM must be loaded via the B side. The RAM, if it is enabled, is loaded when the clock is low. The duration of time the clock is low, is the write enable plus width required to switch the RAM. If the clock is held high, operations can be performed and the results examined, but no results are stored.

Latches (Center Left)

The latches on the RAM outputs are the zero delay type (like 7475) which let the data into the latches appear on the latch outputs until the clock goes low and then hold the data. The latches permit parallel accessing of the RAM and ROM without two delays (one for the ROM and one for the RAM), since the access time of the ROM is masked by the delay through the RAM. The latches eliminate race conditions when the RAM data is fetched and updated in one cycle.

Arithmetic Logic Unit (Lower Center)

Input multiplexers into the arithmetic logic unit (A.L.U.) under ROM control permit the entry of data in or the A channel of the RAM into the A port of the ALU, and the B channel of the RAM or the Q register into the B port of the ALU.

The ALU is of the conventional type except 0/1 true complement elements have been put in the input ports permitting the realization of a totally symmetrical ALU (i.e., A minus B or B minus A). Overflow detection and two zero detect pin (one for positive and one for negative logic) are also included.

Output Multiplexers (Lower Right Hand Corner)

The 3 to 1 output multiplexers under ROM control let through the ALU output, the A latch output, the B latch output on the data out pins. The output multiplexers are three-state outputs controlled by the three-state output control pin. The three-state outputs permit processing to be performed in the 6701 without tying up the data out bus and allow one bus system to tie 6701 data in pins to data out pins. The outputs are enabled when the three-state enable pin is low.

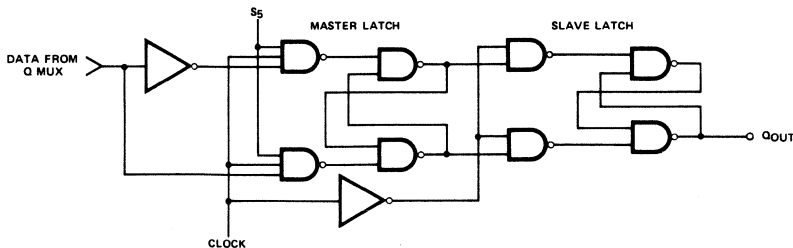
Shift Multiplexers (Upper Left and Upper Right)

The four 3 to 1 mux's on top of the Q register permit the ALU output bus F to be loaded into the Q register. The Q register can also be shifted on itself one place left or right. The four 3 to 1 multiplexers above the RAM permit a transfer or 1 bit left or right shift of the F bus before storage in the RAM. Both the RAM shifter and the Q shifter employ bi-directional shift in/shift out pins to permit expansion to more than 4 bits.

Q Register (Upper Right)

The Q register can function as an accumulator extension register. It would normally be used to hold the least significant half of the double length product of a multiplication or as a storage register to catch the bits shifted off the beginning or end of a word during left or right shifting. In this mode of operation, the shift out pin of the least significant bit of the RAM shifter would be tied to the shift in pin of the most significant bit of the Q register. The Q register can be shifted on itself or be loaded from the ALU bus. The Q shift control pins are in common with RAM shift controls permitting simultaneous RAM and Q shifting. It can also be used as a program counter or scratchpad.

The Q register is a master slave flip-flop. Data is loaded into the master while the clock is low (assuming it is enabled by the ROM) and transferred from the master to the slave when the clock goes high. The Q register is not an edge-triggered latch. Whatever data is present before the clock goes high (assuming the setup time is obeyed) it will be loaded into Q. If the clock is held high, operations can be performed but no results are stored.



Package Pins

Figure 2 shows a listing of the 40 pin I/O. The 6701 uses a standard 40 lead ceramic dip approximately 2.00 inches long and 0.60 inch wide. See Figure 3 for the package details. NOTE THAT V_{CC} AND GROUND ARE NOT ON THE CONVENTIONAL END PINS. This was necessary because the package current would produce too high a voltage drop in the package lead resistance out to the end pins to meet the V_{OL} requirements.

Pin Configuration

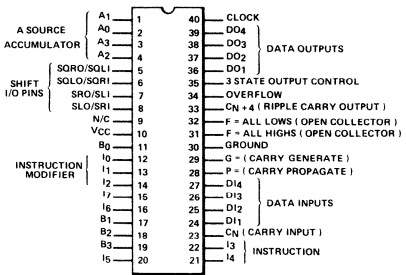
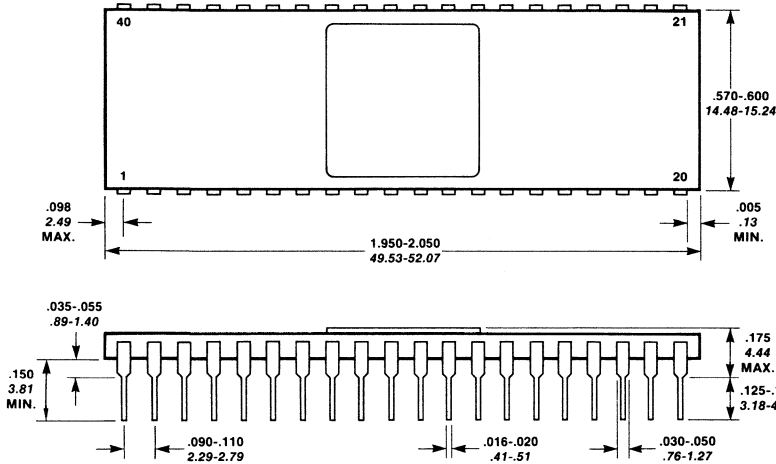


Figure 2.

Package Outline



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES.
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.

40 Pin Ceramic (Side Braze)

Θ_{JA} (thermal resistance from junction to ambient soldered to a printed circuit board in still air) ≈ 35°C/watt
Θ_{JC} (thermal resistance from junction to case with freon as a heat sink) ≈ 20°C/watt

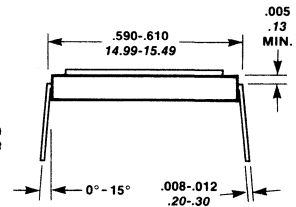


Figure 3.

Burn-In Circuit

The circuit in Figure 4 below puts the device in an instruction where the state of all outputs is known. Any other set of levels on the inputs may result in undefined output states and possible damage to the device under burn-in conditions. The other instructions involve the use of internal register whose initial conditions, after power-up, are undefined. The burn-in circuit shown comes closest to the usual reverse burn-in circuits of logic devices. The unit is in the force LLLL mode with the shift I/O pins disabled, the data outputs disabled, and with a single accumulator always selected.

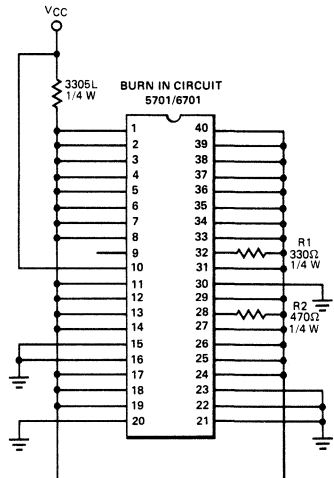


Figure 4.



Absolute Maximum Ratings

Supply Voltage, V_{CC}	-0.5 to 7.0 V
Input Voltage	-1.0 to 5.5 V
Output Current	100 mA
Input Current	-20 to 5 mA
Storage Temperature	-65 to +150 C

Stresses above or extended time at Absolute Maximum Ratings may cause permanent damage or affect device reliability.

DC Characteristics

Unless otherwise indicated, all limits for the 6701 are guaranteed for $5\text{ V} \pm 5\%$ in a free air temperature of 0° to 75°C ; all limits for the 5701 are guaranteed for $5\text{ V} \pm 10\%$ in a free air temperature of -55° to 125°C .

PARAMETER	DEVICE PINS	CONDITIONS	6701			UNITS
			MIN.	TYP. ¹	MAX.	
I_F Input Load Current	Any A, B, or I	$V_{CC} = \text{Max}, V_F = .45\text{ V}$			-250	μA
	Clock or 3 State Control	$V_{CC} = \text{Max}, V_F = .45\text{ V}$			-250	μA
	Shift I/O & Data In	$V_{CC} = \text{Max}, V_F = .45\text{ V}$			-0.80	mA
	C_N	$V_{CC} = \text{Max}, V_F = .45\text{ V}$			-4.80	mA
I_R Input Leakage Current	Any A, B, or I	$V_{CC} = \text{Max}, V_R = 2.40\text{ V}$			25	μA
	Clock or 3 State Control	$V_{CC} = \text{Max}, V_R = 2.40\text{ V}$			25	μA
	Shift I/O	Used as an Input			100	μA
	Data Inputs	Used as an Input			20	μA
	C_N	Used as an Input			120	μA
I_{RB} Input Leakage Current	Any A, B, or I	$V_{CC} = \text{Max}, V_{RB} = 5.50\text{ V}$			1.0	mA
	Clock or 3 State Control	$V_{CC} = \text{Max}, V_{RB} = 5.50\text{ V}$			1.0	mA
	Shift I/O	$V_{CC} = \text{Max}, V_{RB} = 5.50\text{ V}$			1.0	mA
	Data Input	$V_{CC} = \text{Max}, V_{RB} = 5.50\text{ V}$			1.0	mA
	C_N	$V_{CC} = \text{Max}, V_{RB} = 5.50\text{ V}$			1.0	mA
V_{OL} Low Level Output Voltage	Data Outputs, \bar{G} , C_{N+4} , F = All High, F = All Low	$V_{CC} = \text{Min}, I_{OL} = 16\text{ mA}$		0.35	0.50	V
	\bar{P} , Overflow	$V_{CC} = \text{Min}, I_{OL} = 10\text{ mA}$		0.35	0.50	V
	Shift I/O	$V_{CC} = \text{Min}, I_{OL} = 3.2\text{ mA}$ Used as an Output		0.35	0.50	V
I_{CC} Power Supply Current	V_{CC} , Grd	All inputs ground (worst case), All Outputs Open, Shift I/O Open Temp = Max		215	250	mA
		All inputs ground (worst case), All Outputs Open, Shift I/O Open Temp = Min		230	280	mA
V_{IL} Low Level Input Voltage	All Inputs and Shift I/O	$V_{CC} = 5.00\text{ V}$			0.80	V
V_{IH} High Level Input Voltage	All Inputs and Shift I/O	$V_{CC} = 5.00\text{ V}$	2.0			V
V_{IC} Input Clamp Voltage	All Inputs and Shift I/O	$V_{CC} = \text{Min}, I_{IC} = -5.0\text{ mA}$		-1.0	-1.5	V
I_{CEX} Output Leakage Current	All Outputs	$V_{CC} = \text{Max}, V_{CEX} = 2.40\text{ V}$, High Stored or Disabled			100	μA
		$V_{CC} = \text{Max}, V_{CEX} = 0.45\text{ V}$ Disabled			-100	μA
I_{CEXB} Output Leakage Current	All Outputs Shift I/O	$V_{CC} = \text{Max} = V_{CEXB}$ High Stored or Disabled			1	mA
I_{SC} Output Short Circuit Current	$DO_1, DO_2, DO_3, DO_4, \bar{G}, \bar{P}, \bar{OVFL}$	$V_{OUT} = 0\text{ V}, V_{CC} = 5\text{ V}$ Only one Output at a time should be Shorted	5	15	90	mA
V_{OH} Output Voltage "High"	$DO_1, DO_2, DO_3, DO_4, \bar{G}, C_{N+4}$	$I_O = -3.2\text{ mA}, V_{CC} = \text{Min}$ High Stored	2.4	3.5		V
	Shift I/O, \bar{P}, \bar{OVFL}	$I_O = -500\text{ }\mu\text{A}, V_{CC} = \text{Min}$ High Stored	2.4	3.5		V
C_I Input Capacitance	All Inputs	$V_{CC} = 5.0\text{ V}, V_I = 2.0\text{ V}, 25^\circ\text{C}$, 1 MHz		8		pF
C_O Output Capacitance	All Outputs	$V_{CC} = 5.0\text{ V}, V_O = 2.0\text{ V}, 25^\circ\text{C}$, 1 MHz		8		pF

1. Typical values are measured at 5.0 V and 25°C .

AC Characteristics*

PARAMETER	SYMBOL/CONDITIONS	TIME IN NANOSECONDS		
		5 V \pm 5% 0° TO 75°C 6701		
		MIN.	TYP. ¹	MAX.
Delay from RAM Address (A_N or B_N) to	Figure 5A Clock High			
\overline{G}			85	100
\overline{P}			85	100
C_{N+4}			95	110
Zero Detect			120	140
Overflow			100	125
RAM Shifter Outputs			110	135
Data Outputs (bypass ALU)	T_{C1}	20	85	100
Data Outputs (through ALU)	T_{AA}	40	110	140
Delay from Instruction Input (I_N) to	Figure 5A			
\overline{G}			55	75
\overline{P}			55	75
C_{N+4}			60	80
Zero Detect			80	105
Overflow			75	95
RAM Shifter Outputs			75	95
Q Shifter Outputs			25	40
Data Outputs	T_{ID}	15	85	100
Delay from Data Inputs (D_{IN}) to	Figure 5A			
\overline{G}			25	40
\overline{P}			25	40
C_{N+4}			25	45
Zero Detect			20	75
Overflow			40	55
RAM Shifter Outputs			50	70
Data Outputs	T_{DD}	10	50	75
Delay from Carry In (C_N) to	Figure 5A			
C_{N+4}			15	25
Zero Detect			30	40
Overflow			25	35
RAM Shifter Outputs			25	35
Data Outputs		5	30	40
Delay from Clock (low to high) to	A_N, B_N, I_N, D_{IN} constant			
\overline{G}			95	115
\overline{P}			95	115
C_{N+4}			105	125
Zero Detect			120	140
Overflow			115	135
RAM Shifter Outputs			110	135
Q Shifter Outputs			30	40
Data Outputs (bypass ALU)	T_{C2}	20	95	115
Data Outputs (through ALU)		30	115	140
Delay from 3 State Control to	All Inputs constant			
Low Data Outputs	T_{EA}	10	20	25
High Impedance Outputs	T_{ER}	5	15	20

*The maximum of all possible input and output conditions is specified with outputs sinking maximum current through a resistor to V_{CC} and driving a 30 pF load (15 pF on Shift I/O) to ground.

¹ Typical values are measured at 5.0 V and 25°C.

7

AC Characteristics*—Cont'd.

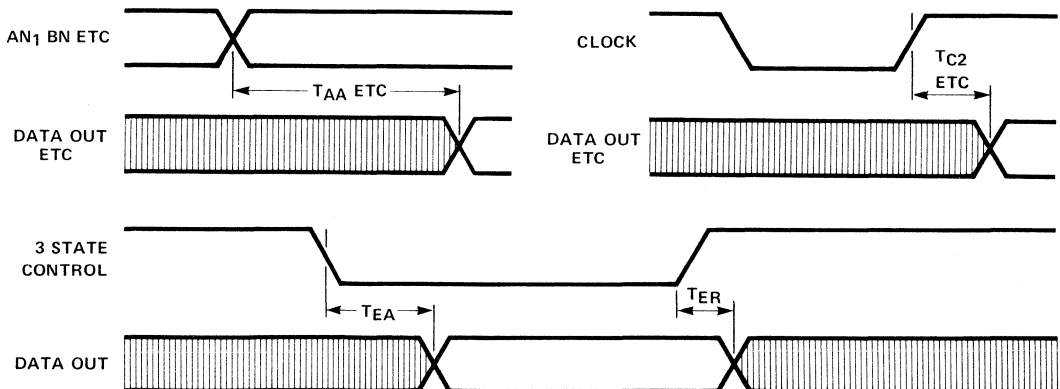
PARAMETER	SYMBOL/CONDITIONS	TIME IN NANOSECONDS		
		5 V ± 5% 0° TO 75°C		
		MIN.	TYP. ¹	MAX.
Setup Time Before the High to Low Transition of Clock	Figure 5B			
A _N	T _{AS}	85	60	
B _N	T _{BS1}	90	60	
I ₀ , I ₁ , I ₂	T _{IS1}	15	5	
Setup Time Before the Low to High Transition of Clock	Figure 5B			
A _N , B _N	T _{BS2}	185	130	
C _N	T _{CNS}	70	45	
I ₃ , I ₄ , I ₅ , I ₆ , I ₇	T _{IS2}	120	90	
Data Inputs (D _{IN})	T _{DS}	70	50	
RAM Shifter Inputs	T _{RS}	45	30	
Q Shifter Inputs	T _{QS}	30	15	
Hold Time After the Low to High Transition of Clock	Figure 5B			
A _N	T _{AH}	-T _{CW} - 15	-T _{CW} - 10	
B _N	T _{BH}	-10	-20	
I ₀ , I ₁ , I ₂	T _{IH1}	-20	-40	
I ₃ , I ₄ , I ₅ , I ₆ , I ₇	T _{IH2}	-30	-60	
C _N	T _{CNH}	-20	-40	
Data Inputs (D _{IN})	T _{DH}	-25	-50	
RAM Shifter Inputs	T _{RH}	-25	-50	
Q Shifter Inputs	T _{QH}	-15	-30	
System Parameters	Figure 5B			
Clock Pulse Width (Low Time)	T _{CW}	50	25	
Minimum Microinstruction Cycle Time	T _{CYCLE} = T _{BS2} + T _{BH}	175	110	∞

*The maximum of all possible input and output conditions is specified with outputs sinking maximum current through a resistor to V_{CC} and driving a 30 pF load (15 pF on Shift I/O) to ground.

¹ Typical values are measured at V_{CC} = 5.0 V and 25°C.

Timing Diagrams

Figure 5A—Delays



LEGEND: Shaded areas indicate "don't care" conditions or permitted timing tolerances.

Timing Diagrams—Cont'd.

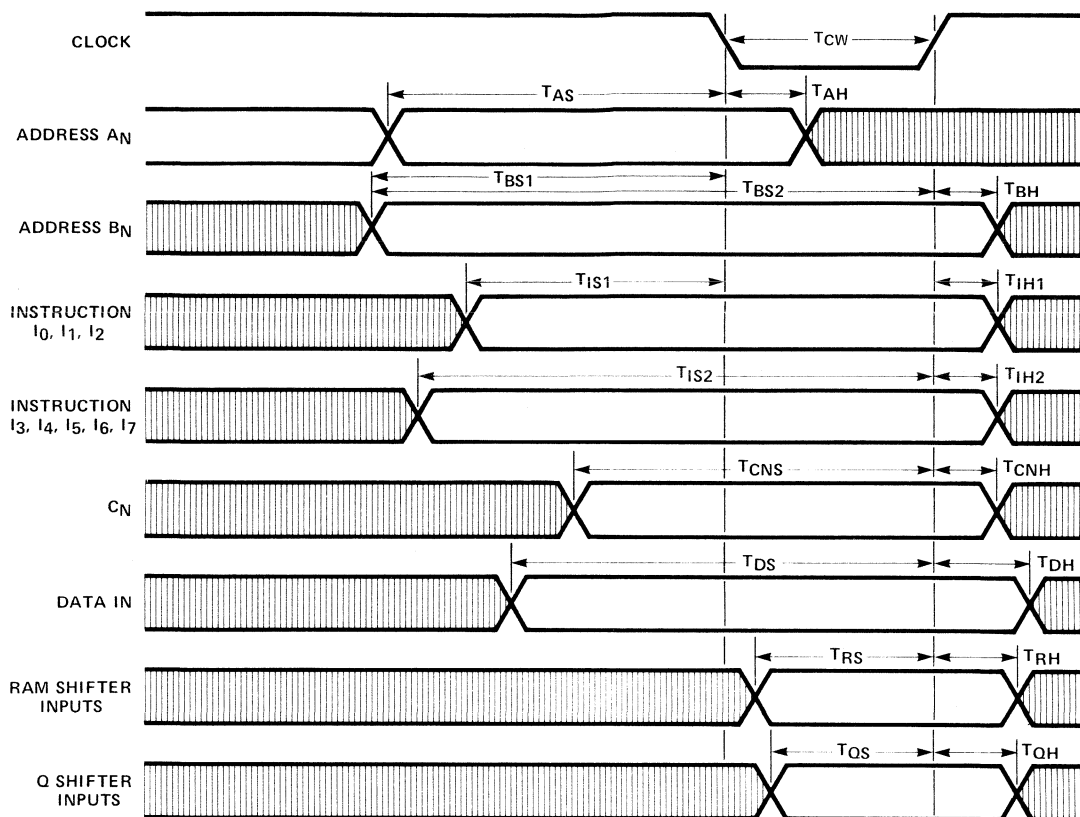


Figure 5B—Set-up and Hold Times

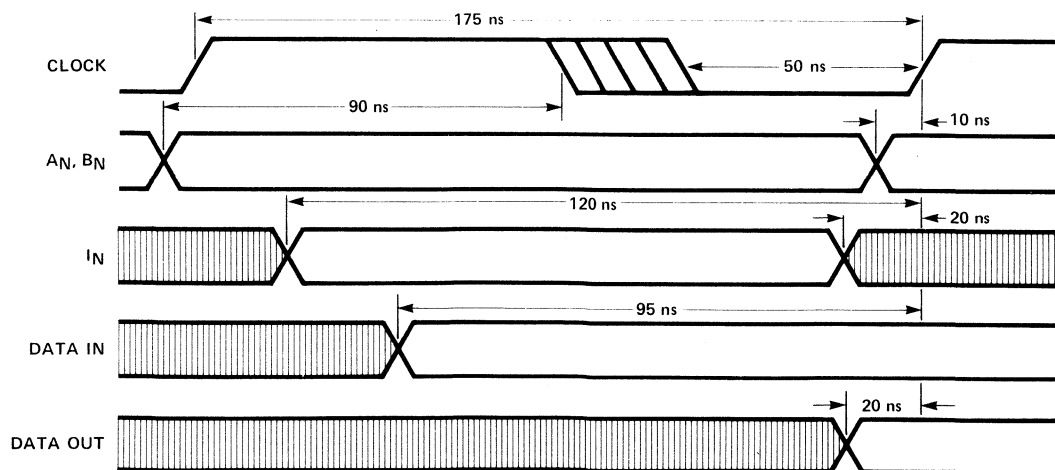


Figure 5C—Sample Minimum Cycle Time for 6701

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Instructions Located in the On-Chip ROMs

Symbol Definitions

- A_I = Any of the 16 four bit registers in the multiport RAM ($I = 0$ to 15)
 B_J = " " " " ($J = 0$ to 15)
 $A_I + B_J$ = A_I plus B_J (arithmetic addition)
 $A_I \nabla B_J$ = A_I exclusive OR'ed with B_J
 $A_I \vee B_J$ = A_I or B_J (logic inclusive or)
 $A_I \wedge B_J$ = A_I and B_J (logic and)
 $\overline{A_I}$ = The complement of A_I
 $A_I \rightarrow Q$ = Transfer A_I to Q, A_I saved, Old Q is lost
 $A_I \rightarrow \text{OUT}$ = Transfer A_I to the output pins, A_I is saved
 $\overrightarrow{A_I}$ = A_I shifted right one bit
 $\overleftarrow{A_I}$ = A_I shifted left one bit
 $B_J - A_I$ = B_J minus $A_I = B_J + \overline{A_I} + C_N = B_J + 2$'s compl. of A_I

Positive (Active High) VS. Negative (Active Low) Logic

The Microcontroller will work with either positive or negative logic. Positive logic defines a TTL High Level ($\approx 3V$) to be a "1" and a Low TTL Level ($\approx \text{GRD}$) to be a "0". Negative logic defines a TTL High to be a "0" and a TTL Low to be a "1". Consider a classical "AND" function in TTL Logic

OUTPUT	INPUTS	
	B	A
L	L	L
L	L	H
L	H	L
H	H	H

in positive logic this becomes

OUTPUT	INPUTS	
	B	A
0	0	0
0	0	1
0	1	0
1	1	1

In negative logic the "AND" becomes an "OR" function since:

OUTPUT	INPUTS	
	B	A
1	1	1
1	1	0
1	0	1
0	0	0

Thus an "AND" in positive logic is an "OR" in negative logic. Similar reasoning yields the following transformations.

POSITIVE LOGIC

AND
 OR
 EXCLUSIVE OR
 EXCLUSIVE NOR
 TRANSFER
 DECREMENT
 INCREMENT
 TRANSFER

NEGATIVE LOGIC

OR
 AND
 EXCLUSIVE NOR
 EXCLUSIVE OR
 DECREMENT
 TRANSFER
 TRANSFER
 INCREMENT

Carry In (C_N)

The carry in pin is high when a carry is desired in positive logic, and a low when a carry is desired in negative logic.

Two ROMs

All of the instructions in the 32×9 ROM can be modified in 8 different ways by the 8×8 ROM. Any instruction for example can be shifted left or right with the data out pins showing A, B, or F and the shifted result stored in the RAM or Q Register or both. If the clock is gated OFF by external logic it will be impossible to load the RAM or Q Register, and the controlled use of C_N in many instructions further raises the instruction count.

Instructions in the 32 x 9 ROM—Positive Logic (1 = H ≈ 3 V) Interpretation

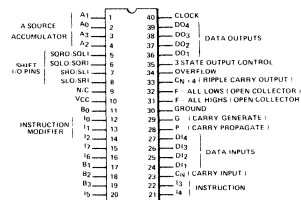
ROM WORD							ALU Instruction (See Pg. 10 for Symbology)	ALU OUTPUT		TYPICAL USES
I ₇	I ₆	I ₅	I ₄	I ₃	Decimal	Octal		No Carry In (C _N = L)	With Carry In (C _N = H)	
L	L	L	L	L	0	00	LLLL + HHHH + C _N	Force 1111	Force 0000	Initialization (Force 1's or 0's)
L	L	L	L	H	1	01	AND A ₁ & B _j	A ₁ ∧ B _j	A ₁ ∧ B _j	AND A ₁ & B _j
L	L	L	H	L	2	02	AND D ₁ & B _j	D ₁ ∧ B _j	D ₁ ∧ B _j	" D ₁ & B _j
L	L	L	H	H	3	03	OR A ₁ & B _j	A ₁ ∨ B _j	A ₁ ∨ B _j	OR A ₁ & B _j
L	L	H	L	L	4	04	OR D ₁ & B _j	D ₁ ∨ B _j	D ₁ ∨ B _j	" D ₁ & B _j
L	L	H	L	H	5	05	Exclusive OR A ₁ & B _j	A ₁ ⊕ B _j	A ₁ ⊕ B _j	Exclusive Or A ₁ & B _j
L	L	H	H	L	6	06	Exclusive OR D ₁ & B _j	D ₁ ⊕ B _j	D ₁ ⊕ B _j	" D ₁ & B _j
L	L	H	H	H	7	07	$\overline{A_1} + HHHH + C_N$	$\overline{A_1} + 1111$	$\overline{A_1}$	Invert A ₁
L	H	L	L	L	8	10	$\overline{D_1} + HHHH + C_N$	$\overline{D_1} + 1111$	$\overline{D_1}$	" D ₁
L	H	L	L	H	9	11	$\overline{B_j} + HHHH + C_N$	$\overline{B_j} + 1111$	$\overline{B_j}$	" B _j
L	H	L	H	L	10	12	$\overline{Q} + HHHH + C_N$	$\overline{Q} + 1111$	\overline{Q}	" Q
L	H	L	H	H	11	13	$\overline{A_1} + LLLL + C_N$	$\overline{A_1}$	$\overline{A_1} + 0001$	2's Complement Of A ₁
L	H	H	L	L	12	14	$\overline{D_1} + LLLL + C_N$	$\overline{D_1}$	$\overline{D_1} + 0001$	" D ₁
L	H	H	L	H	13	15	$\overline{B_j} + LLLL + C_N$	$\overline{B_j}$	$\overline{B_j} + 0001$	" B _j
L	H	H	H	L	14	16	$\overline{Q} + LLLL + C_N$	\overline{Q}	$\overline{Q} + 0001$	" Q
L	H	H	H	H	15	17	A ₁ + LLLL + C _N	A ₁	A ₁ + 0001	Transfer Or Increment A ₁
H	L	L	L	L	16	20	D ₁ + LLLL + C _N	D ₁	D ₁ + 0001	" D ₁
H	L	L	L	H	17	21	B _j + LLLL + C _N	B _j	B _j + 0001	" B _j
H	L	L	H	L	18	22	Q + LLLL + C _N	Q	Q + 0001	" Q
H	L	L	H	H	19	23	A ₁ + HHHH + C _N	A ₁ + 1111	A ₁	Decrement Or Transfer A ₁
H	L	H	L	L	20	24	D ₁ + HHHH + C _N	D ₁ + 1111	D ₁	" D ₁
H	L	H	L	H	21	25	B _j + HHHH + C _N	B _j + 1111	B _j	" B _j
H	L	H	H	L	22	26	Q + HHHH + C _N	Q + 1111	Q	" Q
H	L	H	H	H	23	27	A ₁ + B _j + C _N	A ₁ + B _j	A ₁ + B _j + 0001	Add A ₁ & B _j
H	H	L	L	L	24	30	D ₁ + B _j + C _N	D ₁ + B _j	D ₁ + B _j + 0001	" D ₁ & B _j
H	H	L	L	H	25	31	A ₁ + Q + C _N	A ₁ + Q	A ₁ + Q + 0001	" A ₁ & Q
H	H	L	H	L	26	32	D ₁ + Q + C _N	D ₁ + Q	D ₁ + Q + 0001	" D ₁ & Q
H	H	L	H	H	27	33	A ₁ + $\overline{B_j}$ + C _N	A ₁ - B _j - 0001	A ₁ - B _j	Subtract A ₁ & B _j
H	H	H	L	L	28	34	B _j + $\overline{A_1}$ + C _N	B _j - A ₁ - 0001	B _j - A ₁	" B _j & A ₁
H	H	H	L	H	29	35	D ₁ + $\overline{B_j}$ + C _N	D ₁ - B _j - 0001	D ₁ - B _j	" D ₁ & B _j
H	H	H	H	L	30	36	B _j + $\overline{D_1}$ + C _N	B _j - D ₁ - 0001	B _j - D ₁	" B _j & D ₁
H	H	H	H	H	31	37	D ₁ + \overline{Q} + C _N	D ₁ - Q - 0001	D ₁ - Q	" D ₁ & Q



Instruction Modifiers in the 8 x 8 ROM— Positive Logic (1 = H ≈ 3 V) Interpretation

Rom Word		Rom Word		Load Control		Shift Control			Data Out CLOCK		
I ₂	I ₁	I ₀	Decimal	Load Ram B _j	Load Q	Shift Left	Shift Right	Don't Shift	A Latch	B Latch	ALU Output F
L	L	L	0	X				X			X
L	L	H	1	X				X	X		
L	H	L	2	X				X		X	
L	H	H	3	X		X					X
H	L	L	4	X			X				X
H	L	H	5	X	X	X					X
H	H	L	6	X	X		X				X
H	H	H	7	X	X			X			X

Pin Configuration



Microprogram Controller

57110/67110 Data Sheet

Features/Benefits

- Address 512 Word Pages of Memory
- 8 Control Functions
- Microsubroutine Capability
- On-Chip Loop Counter
- 6 Flag Branch Inputs
- 4-Way Branching

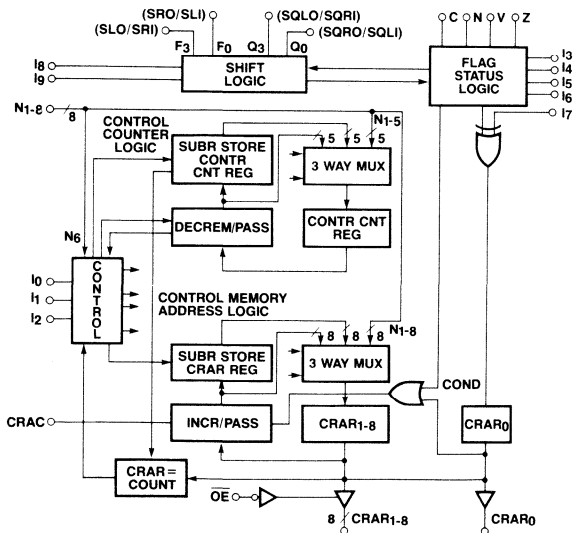
Applications

- LSI Controller Circuit for Control of High Speed Disks, Line Printers, CRT Terminals
- Control of Microprogrammed High Performance Mini-computers with 4-Bit Slice Microprocessors

Ordering Information

TEMPERATURE RANGE	PACKAGE	ORDER NUMBER
0°C to + 75°C	Ceramic	67110D
-55°C to +125°C	Ceramic	57110D

Block Diagram

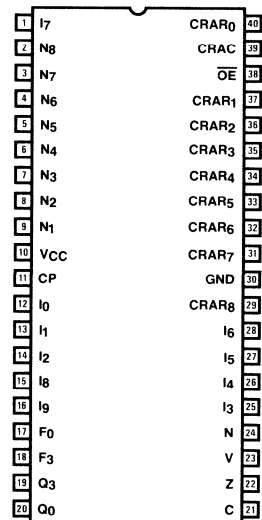


Description

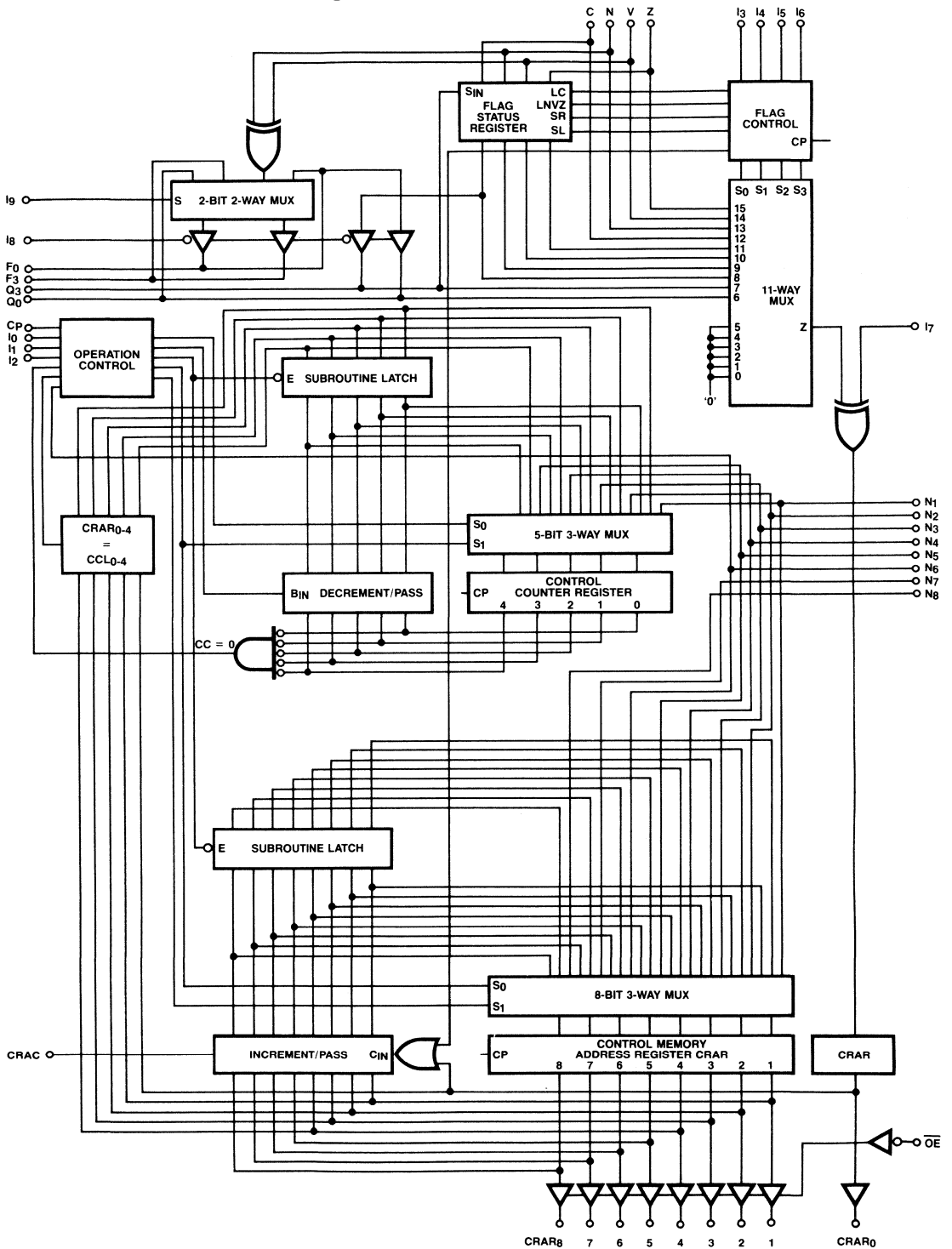
The 57110/67110 Microprogram Controller (MPC) is a member of the 57000/67000 Computer Logic family of high-performance bipolar compatible Schottky TTL components. The device is designed to work in conjunction with 4-Bit Slice Microprocessors and standard ROMs and PROMs for the design of extremely powerful computing systems. The power and flexibility of the MPC also allow it to be used for general purpose control applications. The MPC can directly address up to 512 words of microprogram control memory; larger memories can be accommodated using simple paging techniques.

One of up to six flag signals can be selected from the 5701/6701 4-Bit Slice to provide two-way conditional branching at every step in a microprogram on the value of the flag or its stored value. Four-way conditional branches are possible using an on-chip control counter. The MPC has 8 instructions including continue, conditional and unconditional jumps, conditional and unconditional subroutine jumps to a single level subroutine and subroutine return. Connections are provided to the 5701/6701 for a minimum set of shifting options. The MPC is a synchronous device using a single clock and can operate in systems with less than a 100ns microinstruction period. The device uses a single ± 5 V power supply and is packaged in a standard 40 pin DIP.

Pin Configuration



57110/67110 Detailed Block Diagram



Detailed Description

The MPC is a synchronous machine. All changes visible on external pins except for the combinatorial Shift Logic occur on the single clock Low-to-High transition. Internally there are both dual rank registers (flip-flops) and single rank registers (latches). The latches are enabled when the clock is Low and this, together with some inputs defining information destinations, causes timing constraints such that certain input signals must not change while the clock is Low. These timing constraints are shown in the timing diagrams.

The MPC can be divided up into a number of sections. These sections are the Control ROM Address Register (CRAR₀₋₈) Logic, the Control Counter (CC) Logic, the Flag Status Logic, the Shifting Control for the 5701/6701 and the MPC Control Logic.

CRAR Logic

The CRAR is split up into two sections, an eight-bit section which can remain unchanged, be incremented, loaded from a subroutine temporary storage register latch and loaded from an 8-bit external field N₁₋₈. The one-bit section is the least significant bit of the Address Word and is directly driven from the output of the Flag Status Logic. The output of the Flag Status Logic therefore defines whether the next address is even or odd depending upon the condition of the selected flag signal. This allows two way branching at every clock period.

The eight-bit section of the register passes through a pass/increment unit and back through a 3-way multiplexer. The output of the pass/increment unit can also be stored in a temporary storage register where it may be returned to the CRAR at the end of a microsubroutine. The pass/increment also provides an end of page signal CRAC indicating that the CRAR is at address 510 or 511. Incrementation occurs in the pass/incrementor when the MPC is at an odd address (CRAR₀ = 1) or a Conditional Branch has been selected.

The output of the CRAR passes through buffers to output pins. The eight bit section buffers have three-state outputs so that when the Output Enable (\overline{OE}) is High external signals may drive the Control Memory Address lines.

Control Counter Logic

The Control Counter Logic is 5 bits wide with the logic very similar to the CRAR logic. The logic includes a register, pass/decrement unit, temporary subroutine register and a 3-way input multiplexer which can select information from the external field bits N₁₋₅, the temporary storage register, or the pass/decrement unit. The counter logic is used during the two conditional jump instructions. Each time the MPC encounters a conditional jump instruction, the control counter register is tested for zero and decremented. If the register was zero then the MPC instead of performing a jump instruction continues on to the next address pair. The next time the conditional jump instruction occurs the procedure is repeated, but now the value of the register is one less. The control counter register can be loaded from the N₁₋₅ inputs on receipt of a Continue Load Control Counter instruction.

Flag Status Logic

The Flag Status Logic consists of a loadable Shift Left/Shift Right register, an eleven-way multiplexer, an exclusive OR gate and a small amount of control logic. The shift register can be loaded with four flags C, N, V, Z, with separate loading selection for C and the group NVZ. The register can be shifted one place Left with N going to C, V to N, etc., and a logic zero being pulled into Z. The C register bit is placed on the bidirectional input/output line Q₀ and would most likely in a system enter the least significant bit of the Q register in the 5701/6701. A Right Shift causes C to be loaded from Q₀ this time acting as an input, and what is in C going to N, etc.

The eleven-way multiplexer can be used via the select and control lines I₃₋₆ to select one of the following signals: Stored C, N, V, Z, Present C, N, V, Z, logic 0, Q₀ and Q₃. All of these signals can be inverted by having I₇ = 1, enabling branching on \overline{C} , \overline{N} , etc. The output of the Flag Status Logic Ex Or gate is the input to the least significant CRAR register bit. The Flag Status Logic also provides a signal to the pass/increment unit to indicate that a conditional branch is present and the unit should increment.

Shift Control Logic

The Shift Control Logic provides the connections for a minimum set of useful 5701/6701 shifting options. Two control inputs I_g and I₉ are used to select the desired option. I_g indicates which bidirectional buffers are actively sending information and I₉ selects various signals to apply to the shift lines of the 5701/6701. Provision is made in the shifting logic to provide correct sign information during right arithmetic shifts by an exclusive OR of the N and V signals.

Control Logic

The Control Logic uses the instruction control inputs I₀₋₂, the test zero output of the Control Counter Logic, and the signal which indicates that the Control Counter temporary subroutine storage register contains the same value as the five least significant bits of the CRAR register. These signals are then encoded into the control signals necessary to implement the MPC instructions.

Two flip-flops are included in the control logic. The first remembers that the MPC is in a microsubroutine and when a return is encountered, it is obeyed if the flip-flop is set; if the flip-flop is clear the return is ignored. The second flip-flop indicates that a Preprogrammed Return Subroutine is in progress called by instruction 101, and the MPC should automatically return when equivalence of the CRAR and CC subroutine latch is achieved. Both these flip-flops are automatically cleared during power on if clock is held in the low state and may be reset under microprogram control by loading the Control Counter with N₆ = 1.

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Table I—MPC Control Options

CONTROL CODE			CONTROL ACTION	ADDRESS FIELD DESTINATION
I ₂	I ₁	I ₀		
0	0	0	Continue to next μ instruction	None
0	0	1	Continue to next μ instruction	Control Counter, Clear SRFF if N ₆ = 1
0	1	0	Jump to next μ instruction if Control Counter \neq 0, Decrement Control Counter	None/CRAR (Cond. Jump)
0	1	1	Subroutine Jump to next μ instruction if Control Counter \neq 0, Decrement Control Counter	None/CRAR (Cond. Subr. Jump)
1	0	0*	Return from Subroutine	None
1	0	1**	Jump to next μ instruction Return from Subroutine when Control Counter Subroutine Latch = CRAR ₀₋₄	CRAR (Jump Subroutine)
1	1	0	Jump to next μ instruction	CRAR (Jump)
1	1	1	Subroutine Jump to next μ instruction	CRAR (Jump Subroutine)

* The MPC will only return to the calling program if it entered a Subroutine via a Subroutine Jump instruction; otherwise it will continue to the next μ instruction in sequence.

** This operation allows the MPC to branch to a section of code, perform the operations outlined by the code and return after a preprogrammed CROM address has been reached or if a return is encountered.

Table II—Flag Status Control Options

CONTROL CODE				ACTION		
I ₆	I ₅	I ₄	I ₃	OPERATION	CRAR ₀	BRANCH
0	0	0	0	None	I ₇	Unconditional*
0	0	0	1	Store C	I ₇	Unconditional*
0	0	1	0	Store N, V, Z	I ₇	Unconditional**
0	0	1	1	Store C, N, V, Z	I ₇	Unconditional*
0	1	0	0	Shift Flag Register into Q ₀	I ₇	Unconditional*
0	1	0	1	Shift Flag Register out of Q ₀	I ₇	Unconditional*
0	1	1	0	Instantaneous value of Q ₀ to CRAR ₀	Q ₀ \forall I ₇	Conditional**
0	1	1	1	Instantaneous value of Q ₃ to CRAR ₀	Q ₃ \forall I ₇	Conditional**
1	0	0	0	Stored value of C to CRAR ₀	SC \forall I ₇	Conditional**
1	0	0	1	Stored value of N to CRAR ₀	SN \forall I ₇	Conditional**
1	0	1	0	Stored value of V to CRAR ₀	SV \forall I ₇	Conditional**
1	0	1	1	Stored value of Z to CRAR ₀	SZ \forall I ₇	Conditional**
1	1	0	0	Instantaneous value of C to CRAR ₀	C \forall I ₇	Conditional**
1	1	0	1	Instantaneous value of N to CRAR ₀	N \forall I ₇	Conditional*
1	1	1	0	Instantaneous value of V to CRAR ₀	V \forall I ₇	Conditional**
1	1	1	1	Instantaneous value of Z to CRAR ₀	Z \forall I ₇	Conditional**

Code bit I₇ inverts the status of output line so that the condition is dependent upon \bar{C} , etc. For the first six entries in the table, if I₇ = 0 there is an unconditional branch to X, 0; if I₇ = 1, an unconditional branch to X, 1. SC, SN, SV, SZ are Contents of Carry, Sign, Overflow, and Zero Flip Flops.

* Incrementation of CRAR₁₋₈ occurs if CRAR₀ = 1.

** Incrementation of CRAR₁₋₈ always occurs.

Table III—Shift Control Options

CONTROL CODE		SHIFTING OPERATION	BIDIRECTIONAL SHIFT LINES ACTING AS OUTPUTS			
I ₉	I ₈		F ₃ (SLO/SRI)	F ₀ (SRO/SLI)	Q ₃ (SQLO/SQRI)	Q ₀ (SQRO/SQLI)
0	0	Arithmetic Shift Left	—	Q ₃	—	Flag (SC)
0	1	Arithmetic Shift Right	N \forall V	—	F ₀	—
1	0	Rotate Shift Left	—	F ₃	—	Flag (SC)
1	1	Rotate Shift Right	F ₀	—	F ₀	—

— High Impedance State

SC Contents of Carry Flip Flop

Table IV—Next Address Table

ADDRESSES—In Pairs Even A, 0 etc.
Odd A, 1 etc.

INCREMENT—If Present Address Odd or Conditional

INSTRUCTION	FLAG STATUS	PRESENT ADDRESS	NEXT ADDRESS	COMMENTS
Continue	Unc. '0'	A, 0	A, 0	Locked Loop
	Unc. '1'	A, 0	A, 1	Next Consecutive Address
	Unc. '0'	A, 1	A + 1, 0	Next Consecutive Address
	Unc. '1'	A, 1	A + 1, 1	Skip Over A + 1, 0
	Cond.	A, 0	A + 1, Cond.	Skip Over A, 1
	Cond.	A, 1	A + 1, Cond.	Next Address Pair
Jump	Unc. '0'	A, X	N, 0	Jump to N, 0
	Unc. '1'	A, X	N, 1	Jump to N, 1
	Cond.	A, X	N, Cond.	Jump to N, Cond.
Return	Unc. '0'	A, X	R, 0 or R + 1, 0	Return Address is incremented if CRAR ₀ = 1 or Conditional Branch Subroutine Entry is made
	Unc. '1'	A, X	R, 1 or R + 1, 1	
	Cond.	A, X	R, Cond. or R + 1, Cond.	

X = 0, or 1

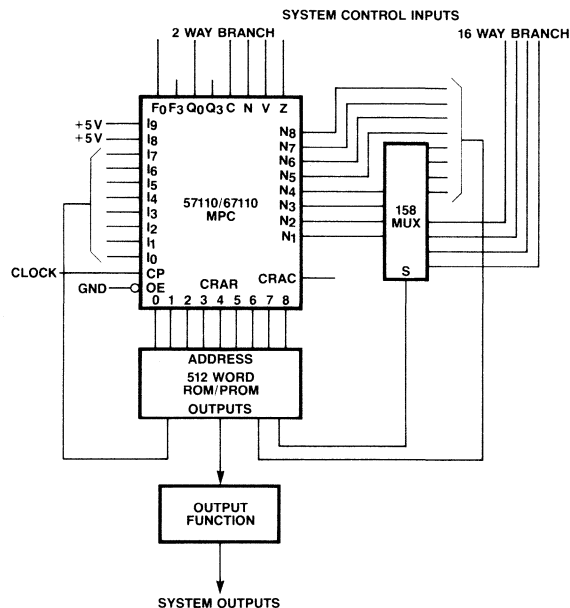
Applications

The 57110/67110 Microprogram controller is a general purpose LSI control element which can be used efficiently in all types of Microprogrammed systems. The device is a powerful microprogrammed sequencer with the additional features of Flag Status multiplexer and storage, an on-chip loop counter with its subroutine register and some shifting connection logic for use with popular Bit-Slice Microprocessors.

The familiar application of such a powerful controller is in the control of microprogrammed high-performance computers. However, the economics of LSI and flexibility of the microprogrammed concept have now made the Microprogram Controller an important and essential concept in all types of high performance digital control. The 57110/67110 is therefore suitable for the central control of disk, tape, CRT and line printers where high data rates and flexibility are necessary.

All of these systems, although they differ in detail, follow the same concept. Inputs from the system to be controlled are sent to the Controller and are examined either through the Flag Status Logic and/or through a Multiplexer connected to the address lines N₁₋₈. The Flag Status inputs allow a two-way branch depending upon the value of the chosen Flag Status input, while the use of a multiplexer at the N inputs allows a 2M way branch on M input variables. The MPC addresses the control memory, some outputs of which are fed back to control the MPC at the next time period, while other outputs of the control memory can form the system outputs either directly or more efficiently via some MSI networks.

Typical Control System Connection



7

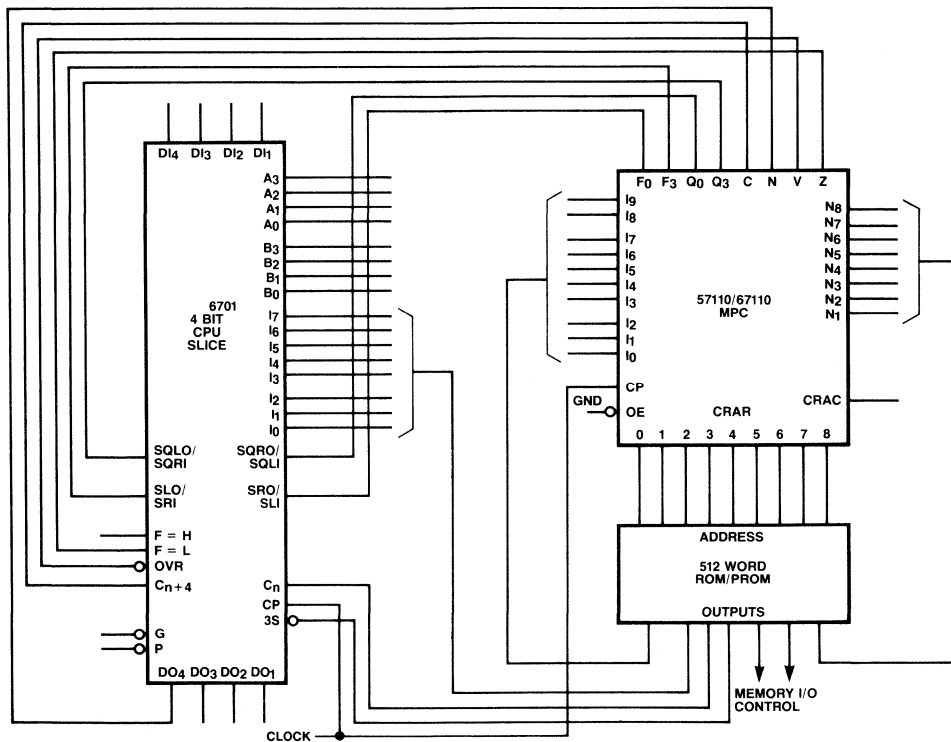
57110/67110 with 4-Bit Slice

The 57110/67110 Microprogram Controller is the ideal LSI element for control of systems which incorporate popular 4-Bit Slice Microprocessors. The 57110/67110 has Flag Status logic which can directly connect to the Flags such as Carry, Sign, Overflow and Zero from the 4-Bit Slice, and allow 2 way branching in the microprogram on the value of one of these Flags. In addition these Flags can be stored for later examination. The extremities of the Q extension register can also be examined by the Flag Status Logic to assist in Multiply and Shifting operations.

The 57110/67110 also has the connections to provide a minimum set of shifting functions which include both double and single length arithmetic shifts and logical end-around shifts.

The Microprogram Controller addresses the control memory which provides the feedback necessary for determining the next operation and control memory address, and also the micro-control signals for the instruction fields of the 4-Bit Slice. The clocks of both the Microprogram Controller and 4-Bit Slice are driven in parallel to make a single clock synchronous system.

**57110/67110
6701
INTERCONNECTIONS**



Electrical Characteristics Over Operating Temperature Range (unless otherwise noted)67110: $V_{CC} = 5V \pm 5\%$, $T_A = 0^\circ C$ to $+75^\circ C$; 57110: $V_{CC} = 5V \pm 10\%$, $T_A = -55^\circ C$ to $+125^\circ C$

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input HIGH Level Voltage		2.0			V
V_{IL}	Input LOW Level Voltage				0.8	V
V_I	Input Clamp Voltage	$V_{CC} = \text{Min}, I_{IN} = -18\text{mA}, T_A = 25^\circ C$		-1.0	-1.5	V
V_{OH}	Output HIGH level Voltage	$V_{CC} = \text{Min}, V_{IH} = 2.0\text{V}, V_{IL} = 0.8\text{V}, I_{OH} = -2.0\text{mA}$	2.4	3.0		V
V_{OL}	Output LOW level Voltage	$V_{CC} = \text{Min}, V_{IH} = 2.0\text{V}, V_{IL} = 0.8\text{V}, I_{OL} = 8\text{mA}$		0.30	0.5	V
I_I	Input Current at Max Input Voltage	$V_{CC} = \text{Max}, V_{IN} = 5.5\text{V}$			1.0	mA
I_{IH}	Input HIGH Level Current I ₀₋₉ , OE, CP N ₁₋₈ , C, N, V, Z Q ₀ , Q ₃ , F ₀ , F ₃	$V_{CC} = \text{Max}, V_{IN} = 2.4\text{V}$			25	μA
		Used as input			50	μA
					100	μA
I_{IL}	Input LOW Level Current I ₀₋₉ , OE, CP N ₁₋₈ , C, N, V, Z Q ₀ , Q ₃ , F ₀ , F ₃	$V_{CC} = \text{Max}, V_{IN} = 0.5\text{V}$			250	μA
		Used as input			1.0	mA
					0.5	mA
I_{OZ}	Output Off State (high impedance) Current CRAC ₁₋₈	$V_{CC} = \text{Max}, V_{OUT} = 0.5\text{V}$			-50	μA
		$V_{CC} = \text{Max}, V_{OUT} = 2.4\text{V}$			50	μA
I_{OS}	Output Short Circuit Current	$V_{CC} = \text{Max}, V_{OUT} = 0\text{V}$	20		90	mA
I_{CC}	Supply Current	$V_{CC} = \text{Max}$		159	254	mA

Switching Characteristics

SYMBOL	PARAMETER	TEST CONDITIONS	57110			67110		
			MIN	TYP	MAX	MIN	TYP	MAX
t_{HZ}, t_{LZ} t_{ZL}, t_{ZH}	Delay from OE to: CRAR ₁₋₈ High Impedance State CRAR ₁₋₈ Active State	$C_L = 15\text{pF}$ See Timing Diagrams	5	12	25	5	12	20
			5	10	25	5	10	20
t_{HZ}, t_{LZ} t_{ZL}, t_{ZH}	Delay from I _g to: F ₀ , F ₃ , Q ₀ , Q ₃ High Impedance State F ₀ , F ₃ , Q ₀ , Q ₃ Active State		5	15	34	5	15	28
			5	18	40	5	18	32
t_{PHL}, t_{PLH}	Delay from I _g to F ₀ , F ₃		5	14	32	5	14	27
t_{PHL}, t_{PLH}	Delay from N, V to F ₃		5	15	32	5	15	27
t_{PHL}, t_{PLH}	Delay from F ₀ to F ₃		4	10	20	4	10	18
t_{PHL}, t_{PLH}	Delay from F ₃ to F ₀		4	10	20	4	10	18
t_{PHL}, t_{PLH}	Delay from Q ₀ to F ₀		4	10	20	4	10	18
t_{PHL}, t_{PLH}	Delay from F ₀ to Q ₃		4	10	20	4	10	18
t_{PHL}, t_{PLH} t_{PHL}, t_{PLH} t_{PHL}, t_{PLH}	Delay from Clock Low to High Transition to: Q ₀ CRAR ₀₋₈ CRARC	$C_L = 30\text{pF}$ S ₁ , S ₂ Closed See Timing Diagrams	15	35	60	15	35	55
			6	17	40	6	17	35
			10	23	48	10	23	42
t_{SI}	Set-Up Time Before the High to Low Transition of Clock: I ₀ , I ₁ , I ₂ , I ₃ , I ₄ , I ₅ , I ₆		5	-5		5	-5	
t_{SD} t_{SD} t_{SD}	Set-Up Time Before the Low to High Transition of Clock: I ₇ C, N, V, Z, Q ₀ , Q ₃ N ₁₋₈		16	6		16	6	
			28	11		20	11	
			30	15		24	15	
t_{HI} t_{HD} t_{HD}	Hold Time After the Low to High Transition of Clock: I ₀ , I ₁ , I ₂ , I ₃ , I ₄ , I ₅ , I ₆ , I ₇ C, N, V, Z, Q ₀ , Q ₃ N ₁₋₈		18	6		15	6	
			25	13		22	13	
		12	5		12	5		
t_{CPL}	Minimum Clock Low Pulse Width		18	40		18	30	
t_{CPH}	Minimum Clock High Pulse Width		45	80		45	70	

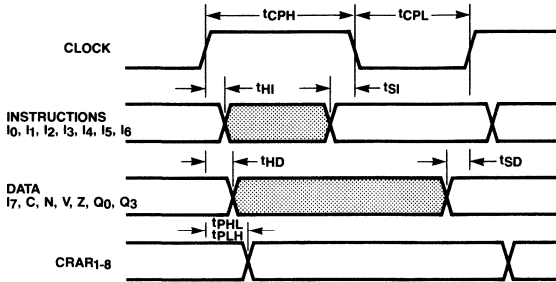
Typical values are at $V_{CC} = 5.0\text{V}$ and $T_A = 25^\circ C$.In order to guarantee that control logic flip flops are reset during power on, the Clock Pulse must be held LOW (0.5V) until V_{CC} is at $V_{CC \text{ min}}$.

Absolute Maximum Ratings

Supply Voltage, VCC	-0.5V to +7V
Input Voltage	-1.5V to +5.5V
Output Current	100mA
Ambient Temperature	-55°C to +125°C
Storage Temperature	-65°C to +125°C

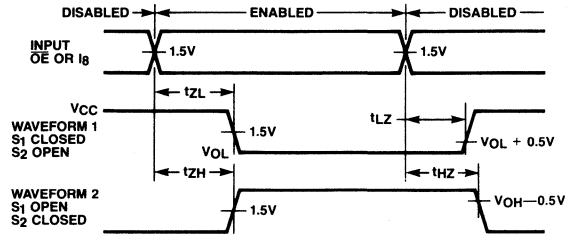
Stresses above and extended time at Absolute Maximum Ratings may cause permanent damage or affect device reliability. Functional operation at these limits is neither guaranteed nor implied.

Timing Diagrams



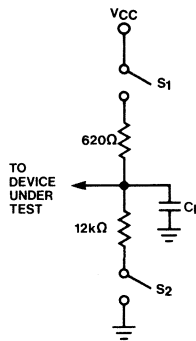
Notes:
 Shaded areas denote DON'T CARE conditions.
 All delays, set-up and hold times measured at 1.5V level.

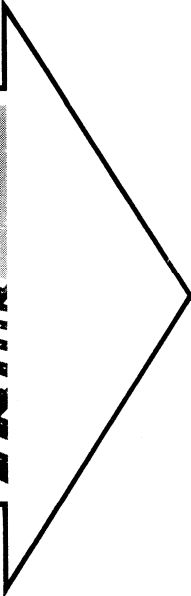
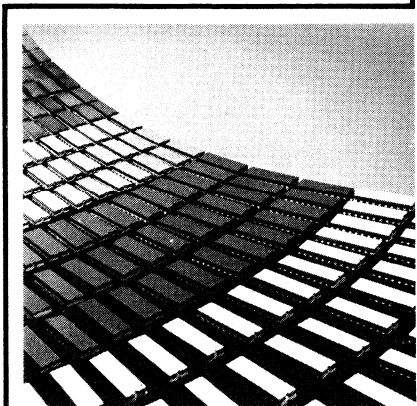
Three State Delays



Notes:
 Waveform 1 requires internal conditions such that the output is LOW except when disabled.
 Waveform 2 requires internal conditions such that the output is HIGH except when disabled.

Standard Test Loads





Introduction	1
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Arithmetic Elements Selection Guide

The following selection guides are designed to simplify the choice of the particular function to fit the specific application.

High Speed Parallel Multipliers

DESCRIPTION	PART NO.	MAX DELAY ¹	PINS	PAGE
8x8 Multiplier	67558-1	125 ns	40	8-5
	57558-1	135 ns	40	
	67558	150 ns	40	
	57558	155 ns	40	
8x8 Pipelined multiplier	67559	65 ns ²	40	†
	57559			
16x16 Pipelined multiplier	MPY-16	140 ns ²	64	†

Sequential Multipliers/Accumulators/Dividers

DESCRIPTION	PART NO.	MAX. MULTIPLICATION TIME ¹	PINS	PAGE
8 Bits	67508	400 ns	22	8-11
	57508			
16 Bits	67516/8	800 ns	24/28	8-11
	57516/8			

Processor-Slice

DESCRIPTION	PART NO.	MIN. CYCLE TIME ¹	PINS	PAGE
4 Bit slice	6701	175 ns	40	7-75
High speed 4 Bit slice	2901A-C	100 ns	40	7-7
	2901A-M	110 ns		

Look-Up Tables

DESCRIPTION	PART NO.	MAX ¹ ACCESS TIME	PINS	PAGE
Sine (0°-90°) Look-Up Table	6086/7	100 ns	24	8-19
	5086/7	150 ns	24	8-19

[†]Data Sheet will appear in a future edition of the LSI Data Book. Contact Application Department for additional information.

MSI Arithmetic Elements

DESCRIPTION	PART NO.	MAX. ADD TIME ¹	MAX. CARRY (OR GENERATE) TIME ⁴	PINS	PAGE
4 Bit ALU	5/74S381	27 ns	20 ns	20	†
4 Bit fast ALU (pin compatible to 74S381)	5/67S581/2	17 ns ²	15 ns ²	20	†
4 Bit adder	5/74LS283 5/74S283	24 ns 18 ns	17 ns 12 ns	16 16	†
4 Group carry-look-ahead generator	5/74S182		7 ns	16	†
8 Group carry-look-ahead generator	5/67S583 5/67S584 5/67S585		12 ns 12 ns 12 ns	28 28 24 ³	†
8 Bit incrementer	5/67S586	15 ns ²		20	†
8 Bit two's complementors	5/67S587	15 ns ²		20	†
8 Bit double incrementer	5/67S588			20	†
8 Bit incrementer, decrementer and two's complementor	5/67S589	20 ns ²		24 ³	†

- NOTES: 1. Over recommended supply and temperature range.
 2. Design goals.
 3. 0.3 inch wide.
 4. At 5 Volt and 25°C.

†Data Sheet will appear in a future edition of the LSI Data Book. Contact Application Department for additional information.

8 x 8 Multiplier

67558/57558
67558-1/57558-1

Features/Benefits

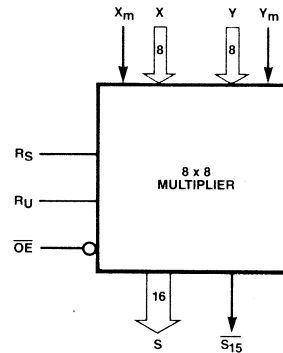
- Unsigned, Signed, or Mixed Multiplication
- Rounding Inputs for Signed or Unsigned Operation
- Inverted Most Significant Output for Signed Expansion
- Three-State Outputs for Bus Operation
- High Speed—125 ns Max

Description

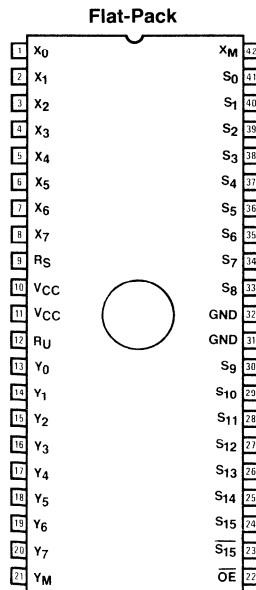
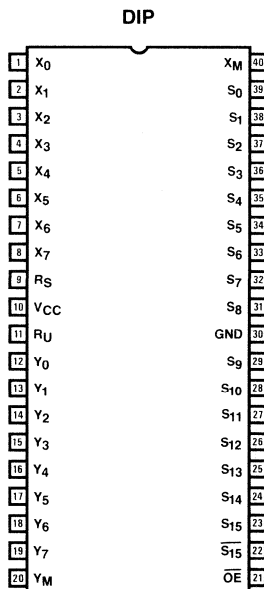
The 57558/67558 is a high speed 8 x 8 combinatorial Multiplier which can multiply two eight-bit unsigned or signed 2s complement numbers and generate the sixteen-bit unsigned or signed product. Each input operand X and Y has an associated Mode control line, X_M and Y_M respectively. When a Mode control line is at a Low logic level the operand is treated as an unsigned eight-bit number while if the Mode control is at a High logic level the operand is treated as an eight-bit signed 2s complement number. Two additional inputs R_S and R_U allow the addition of a bit in the multiplier array at the appropriate bit positions for rounding signed or unsigned fractional numbers. The most significant product bit is available in both True and Complement form to assist in expansion to larger signed multipliers. The product outputs are three-state, controlled by an active Low Output Enable which allows several Multipliers to be connected to a parallel bus or be used in a pipelined system. The device uses a single +5V power supply and is packaged in a standard 40-pin DIP.

PART NUMBER	PACKAGE	TEMPERATURE RANGE
67558, 67558-1	D40	0°C TO +75°C
57558, 57558-1	D40	-55°C TO +125°C
57558, 57558-1	F42	-55°C TO +125°C

Logic Symbol



Pin Configuration

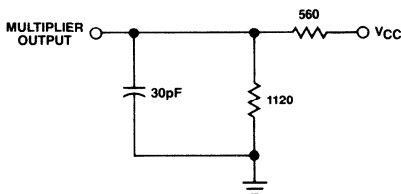


AC Electrical Characteristics

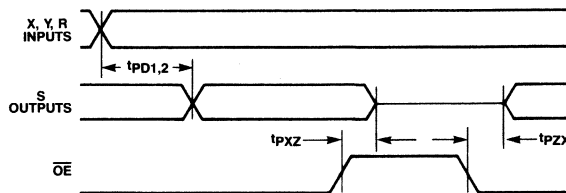
Over Recommended Operating V_{CC} and Temperature Range

SYMBOL	PARAMETER	DEVICE	MIN	TYP	MAX	UNIT
tpXZ	Delay from OE to S High Impedance State	67558		30	40	ns
		57558		30	50	
		67558-1		30	40	
		57558-1		30	50	
tpZX	Delay from OE to S Active State	67558		30	40	ns
		57558		30	50	
		67558-1		30	40	
		57558-1		30	50	
tpD1	Delay from Y, X to S_{0-4}	67558		80	135	ns
		57558		80	140	
		67558-1		80	115	
		57558-1		80	125	
tpD2	Delay from Y, X to S_{5-15} , S_{15}	67558		100	150	ns
		57558		100	155	
		67558-1		100	125	
		57558-1		100	135	

Standard Test Load



Timing Waveform



Functional Description

The 57558/67558 Multiplier is an 8 x 8 combinatorial logic array capable of multiplying numbers in unsigned, signed 2s complement, or mixed notation. Each eight-bit input operand X and Y has associated with it a mode control which determines whether the array treats the number as signed or unsigned. If the mode control is at a High Logic level then the operand is treated as a 2s complement number with the most significant bit having a negative weight, while if the mode control is at a Low Logic level then the operand is treated as an unsigned number.

The multiplier provides all 16 product bits generated by the multiplication. For expansion during signed or mixed multiplication the most significant product bit has both true and complement available. This allows an adder to be used as a

subtractor in many applications and eliminates the need for SSI circuits.

Two inputs, R_5 and R_{1j} , are additional inputs to the array which allow the addition of a bit at the appropriate positions in the array so as to provide rounding to the best signed or unsigned fractional eight-bit result. These inputs can also be used for rounding in larger multipliers.

The product outputs of the multiplier are controlled by an active Low Output Enable control. When this control is at a Low Logic level the multiplier outputs are active, while if the control is at a High Logic level then the outputs are placed in a high-impedance state. This three-state capability allows multipliers to be placed on a common bus and also allows pipelining of multiplications for higher speed systems.

Absolute Maximum Ratings

Supply Voltage V_{CC}	-0.5V to +7.0V
Input Voltage	-1.5V to +5.5V
Input Current	-20 mA to +5 mA
Output Current	100 mA
Storage Temperature Range	-65°C to +150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	57558, 57558-1			67558, 67558-1			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply Voltage	4.5	5.0	5.5	4.75	5.0	5.25	V
T_A	Operating Free Air Temperature				0	25	75	°C
T_C	Operating Case Temperature	55	25	125				°C
I_{OH}	High Level Output Current			-2.0			-2.0	mA
I_{OL}	Low Level Output Current			8			8	mA

DC Electrical Characteristics

Over Recommended Operating Free Air Temperature Range Unless Otherwise Noted

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP ¹	MAX	UNIT
V_{IH}	High Level Input Voltage		2.0			V
V_{IL}	Low Level Input Voltage				0.8	V
V_{IC}	Input Clamp Voltage	$V_{CC} = \text{Min}, I_I = -18 \text{ mA}$		-1.0	-1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = \text{Min}, I_{OH} = -2.0 \text{ mA}$	2.4	3.0		V
V_{OL}	Low Level Output Voltage	$V_{CC} = \text{Min}, I_{OL} = 8 \text{ mA}$		0.3	0.5	V
I_{HZ}	High Level Off-State Output Current	$V_{CC} = \text{Max}, V_O = 2.4 \text{ V}$			100	μA
I_{LZ}	Low Level Off-State Output Current	$V_{CC} = \text{Max}, V_O = 0.5 \text{ V}$			-100	μA
I_I	Maximum Input Current	$V_{CC} = \text{Max}, V_I = 5.5 \text{ V}$			1.0	mA
I_{IH}	High Level Input Current	$V_{CC} = \text{Max}, V_I = 2.4 \text{ V}$			100	μA
I_{IL}	Low Level Input Current	$V_{CC} = \text{Max}, V_I = 0.5 \text{ V}$			-1.0	mA
I_{OS}	Output Short Circuit Current	$V_{CC} = \text{Max}, V_O = 0 \text{ V}$	-10		-90	mA
I_{CC}	Supply Current	$V_{CC} = \text{Max}$		180	280	mA

NOTE: 1. Typical values are at $V_{CC} = 5.0 \text{ V}$, $T_A = 25^\circ \text{C}$

Rounding

Multiplication of two n-bit operands results in 2n-bit product*. Therefore, in n-bit system it is necessary to convert the double-length product into a single-length product. This can be accomplished by truncating or rounding. The following examples, illustrate the difference between the two conversion techniques in decimal arithmetic.

$$\begin{array}{l}
 39.2 \rightarrow 39 \\
 39.6 \rightarrow 39 \\
 \left. \vphantom{\begin{array}{l} 39.2 \\ 39.6 \end{array}} \right\} \text{Truncating} \\
 \\
 39.2 + 0.5 = 39.7 \rightarrow 39 \\
 39.6 + 0.5 = 40.1 \rightarrow 40 \\
 \left. \vphantom{\begin{array}{l} 39.2 + 0.5 \\ 39.6 + 0.5 \end{array}} \right\} \text{Rounding}
 \end{array}$$

Obviously, rounding maintains more precision than truncating, but it may take one more step to implement. The additional step involves adding one-half of the weight of the single length LSB to the MSB of the discarded part e.g. in decimal arithmetic round-

ing 39.28 to one decimal point is accomplished by adding 0.05 to the number and truncating the LSB.

$$39.28 + 0.05 = 39.33 \rightarrow 39.3$$

The situation in binary arithmetic is quite similar, but two cases need to be considered; signed and unsigned data representation. In signed multiplication, the two MSBs are identical (except when both operands are -1) therefore, the best single length product is shifted one position to the right with respect to the unsigned multiplications. Figure 1 illustrates these two cases for the 8x8 multiplier. In the signed case, adding one-half of the S7 weight is accomplished by adding 1 in bit position 6, and in the unsigned case 1 is added to bit position 7. Therefore, the 67558 multiplier has two rounding inputs, R_S and R_U. Thus, to get a rounded single length result the appropriate R input is tied to V_{CC} (logic one) and the other R input is grounded. If double length result is desired both R inputs are grounded.

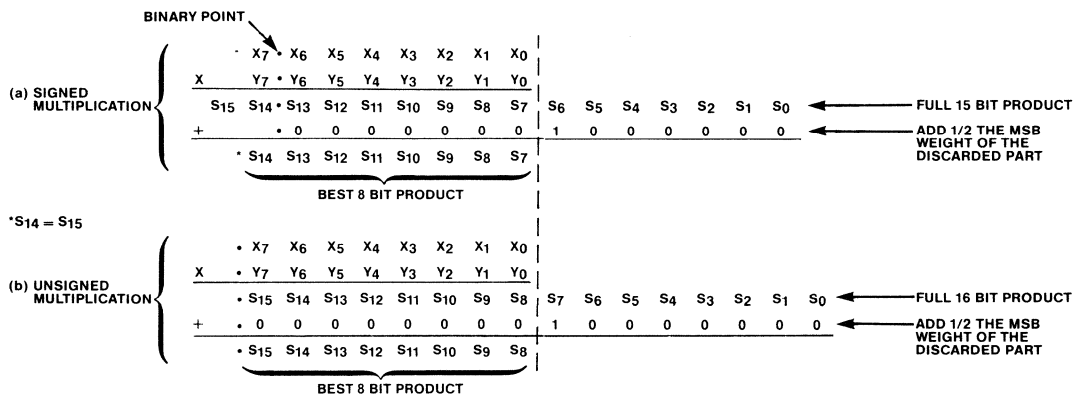


Figure 1. Rounding the Result of Binary Fractional Multiplication.

- (a) In signed (2's complement) notation, the MSB of each operand is the sign bit, and the binary point is to the right of the MSB. The resulting product has a redundant sign bit and the binary point is to the right of the second MSB of the product. The best eight-bit product is from S₁₄ through S₇, and rounding is performed by adding "1" to bit position S₆.
- (b) In unsigned notation the best 8-bit product, is the most significant half of the product, corrected by adding "1" to bit position S₇.

* In general: multiplication of M-bit operand by N-bit operand results in M + N bit product.

Signed Expansion

The most significant product bit has both true and complement outputs available. When building larger signed multipliers the partial products except at the lower stages are signed numbers. These unsigned and signed partial products must be added together to give the correct signed product. Having both the true and complement of the most significant product bit available assists in this addition. For example, say that two signed partial products must be added and MSI adders are used; we then have the situation of adding together the Carry from the previous adder stage plus the addition of the two negative most significant partial product bits. The result of adding these variables must be a positive sum and a negative carry (borrow). The equations for this are:

$$S = A \oplus B \oplus C$$

$$C_0 = AB + BC + CA$$

where C is the Carry In and A and B the sign bits of the two partial products.

Now an adder produces the equations:

$$S = A \oplus B \oplus C$$

$$C_0 = AB + BC + CA$$

Examining these equations it can be seen that if the inversion of A and B are used then the adder produces the inversion of the negative carry since

$$AB + B\bar{C} + \bar{C}A = \overline{\overline{AB} + BC + C\bar{A}},$$

and the sum remains the same.

16 X 16 Two's Complement Multiplication

The 16-bit X operand is broken into two 8-bit operands (X₀-X₇ and X₈-X₁₅), and so is the Y operand. Since the situation is that of a cross product, four partial products are generated as follows:

$$A = X_L * Y_L$$

$$B = X_L * Y_H$$

$$C = X_H * Y_L$$

$$D = X_H * Y_H$$

where the subscript L stands for bits 0-7, and the subscript H stands for bits 8-15.

Expanding in two's complement multiplication requires a sign extension of the B and C partial products. Thus, B₁₅ and C₁₅ need to be extended eight positions to the left (to align with D₁₅). In this approach two more adders are required. But the complement of the MSB (S₁₅) on the 67558 can be used to save these two adders. The Figure shows the implementation of such a 16x16 signed two's complement multiplication.

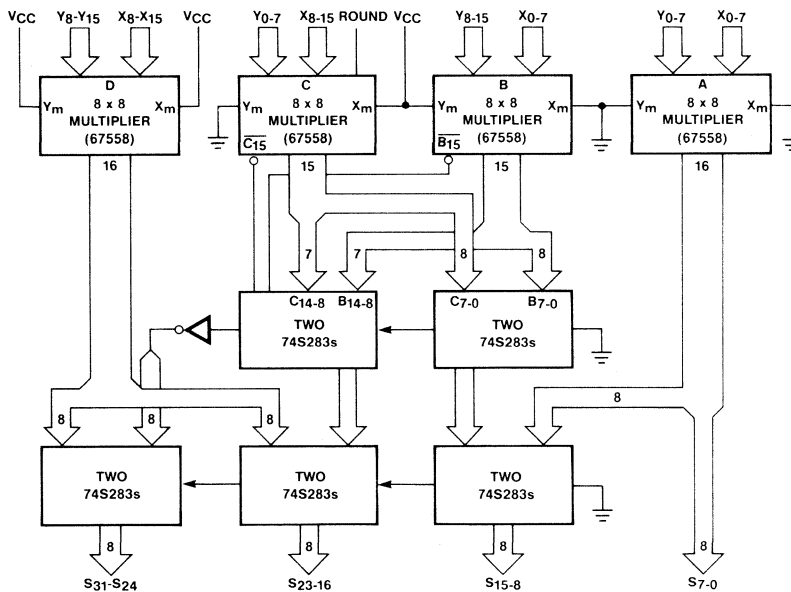


Figure 2. 16 x16 Two's Complement Signed Multiplication.

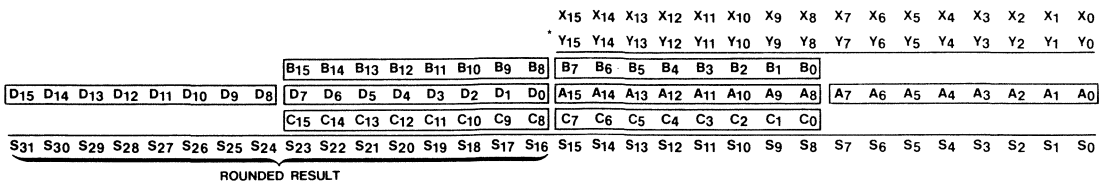


Figure 3. Unsigned Expansions of the 8x8 Multiplier to 16x16 Multiplication.



67516/67518 16 x 16 Multiplier/Divider

67508 8 x 8 Multiplier/Divider

Product Information

67516 16 x 16 (67508 8 x 8) Multiplier/Divider

The 67516 (67508) is a bus organized family of 16 x 16 and 8 x 8 Multiplier/Divider. The device provides both multiplication and division of 2s complement 16 (8) bit numbers at high speed. There are 16 different multiply options including positive and negative multiply, positive and negative accumulation, multiplication by a constant and both single and double length addition in conjunction with the multiplication. Seven different divide options allow single or double length division, division of a previously generated number, division by a constant, and continual division of a remainder or quotient. The 67516 (67508) is a time sequenced device requiring a single clock and loads operands and presents results to a bi-directional 16 (8) bit-bus. The loading of the operands, reading of the results and control of the device is performed by a 3-bit control field. The device has the additional feature that operands and results can be either integers or fractions and when dealing with fractions, automatic scaling occurs. Results can be rounded if required and an Overflow output indicates whenever a result is outside the normally accepted number range. For a simple multiplication of two operands and reading of the double length result the device takes $n/2$ clock periods, a worst case clock period of 100 ns gives a multiplication time of 800 ns worst case for 16 x 16 multiplication and 400 ns for 8 x 8. More complex multiplications will take additional clock periods for loading the additional operands. A simple divide operation will take $n + 4$ clock periods for a worst case time of $2\mu\text{s}$ (32 bits/16 bits) and $1.2\mu\text{s}$ (16 bits/8 bits).

The device uses standard low-power Schottky technology to produce a single +5V supply TTL compatible device. Bus input and control and clock inputs require less than 1mA input current, and bus outputs are three-state sinking 8mA at the low logic level. These devices will be available both in a commercial and military temperature range and packaged in 24 pin (16 x 16) and 16 pin (8 x 8) dual-in-line packages. Power consumption will be approximately 1 watt and 0.75 watts respectively to give a worst case clock period over the military temperature range of 100 ns.

Device Operation

The Multiplier/Divider contains four working registers each of 16 (8) bits. These registers are Y the Multiplier register, X the Multiplicand and Divisor register, W which is the least significant half of a double length accumulator and holds the least significant half of the product after a multiplication or the quotient after a division operation. In addition to the registers, there is a high speed arithmetic unit which performs addition, subtraction and shifting operations in order to generate the required arithmetic functions, a loading sequencer and a PLA control network.

Operands are loaded into the working registers in time sequence at each clock period under the control of a sequencer. A load signal must be low in order for the clock to activate the loading process and continue to the next step in the loading operation. After all the operands are loaded, the device jumps to the multiply or to the divide routine and performs the required operation. After $n/2$ clock periods for a multiply (or $n + 4$ clock periods for a divide), the device is ready to place the result on the bus in time sequence.

Three control inputs $I_{0,1,2}$ select the required function and drive the sequencer from state to state. So the action of the Multiplier/Divider at any clock period is a function of the machine state and the state of the control inputs. Figure 1 shows the Multiply/Divide State Table and all possible operations. After a Read or Round operation the machine is driven back to State 0 and a new sequence of arithmetic operations is assumed. If a chain operation is being performed, such as accumulate products, then State 0 is bypassed and loading of an operand or jumping to the arithmetic operation occurs at the end of the previous arithmetic operation at State 32 for a Multiply, or State 33 for a Divide.

Register X is a dual rank register which allows the loading of operand X during the multiplication or division process. If the machine enters the loading sequence and a new X operand has not been loaded then the machine proceeds with the previously loaded X. This loading while processing allows a cycle to be saved during chain calculations and also allows multiplication and division by a constant.

Figures 2 and 3 show the codes and time taken for the 23 different arithmetic operations possible. These operations can be concatenated in strings to perform complex arithmetic 2s complement operations at high speed. Rounding and reading of results can be performed after any operation.

Figure 4 is a block diagram of the nxn Multiplier/Divider.

Multiplication

The 67516 (67508) provides 2s complement 16 (8) bit multiplication, and can also accumulate previously generated double products. No time penalty is incurred for accumulation since the machine accumulates while the multiplication operation is proceeding. In addition to accumulation the device can add in to a product either a single length or double length number. It can also use a previously loaded operand as a constant so that constant multiplication and accumulation is possible.

One key feature is the ability to perform both positive and negative multiplications again without any speed penalty. This feature allows complex multiplications to be programmed simply. Another important feature is the ability to work in fractions or integers.

Division

The 67516 (67508) also provides a range of division operations. A double length number in Z,W is divided by X, and the result Q is stored in Z and the remainder R in W. Again all numbers are in the 2s complement number representation with the most significant bit of an operand, whether double or single length, having a negative weight. In order to facilitate repeated division and have a multiple length quotient keep the same sign, the remainder is always the same sign as the dividend. Fractional or integer operation is possible and division and multiplication operations can be concatenated. For example, the operations $(A \times B)/C$, $(A/B) \times C$ can easily be performed. The dividend can be any previously generated result, product, quotient, remainder, or a double or single length signed operand.

Reading Results

Results of an arithmetic operation, or string of operations, can be read onto the 16 (8) bit bus if the machine is at the end of an operation or at the start of a new sequence. The read operation requires that the load signal is held Low whereby the information is read out onto the bi-directional bus when Code 7 is specified. (See Figure 5) Since there is a double length accumulator Z,W reading can take two time periods. First register Z is read out, this could be the most significant half of a product, or the quotient during a division operation. After a clock has been received and Code 7 is still present, the least significant half of the product from the W register is placed on the bus, or the remainder if a division operation was performed.

If the machine is asked to perform a read during the loading sequence then the sequence is broken and the machine is forced back to state 0 ready to start the sequence again. Continual read operations at state 0 just swap the contents of register Z and W.

Initialization of the 67516 Multiplier/Divider can easily be performed by continually calling out Code 7 which after a maximum of 21 (13) clock periods forces the machine back to State 0. The 67508/18 have a direct Reset line.

Integer and Fractional Arithmetic

The 67516 (67508) can work in either fractional or integral number representations. When working with integers all numbers are scaled from the least significant end and the least significant bit is assumed to have a weight of 2^0 . For integer multiplication, accumulation, and division, all numbers are scaled from this least significant weight, and results are correct if interpreted in this manner. The double length register Z,W can therefore hold numbers in the range -2^{31} to $+2^{31}-1$ (-2^{15} to $+2^{15}-1$) and the operands X and Y and single length results are in the range -2^{15} to $+2^{15}-1$ (-2^7 to $+2^7-1$).

When working with fractions, the machine automatically performs scaling so that input operands and result have a consistent format. All numbers in the fractional representation are scaled from the most significant end which has a weight of 2^0 and is negative. The binary point is one place to the right of this most significant bit, so that the next bit has a weight of 2^{-1} . The double length register Z,W therefore holds numbers in the range -1 to $+1 - 2^{-31}$ (2^{-15}) and the operand X and Y and single length results are in the range -1 to $+1 - 2^{15}$ (2^7). Since

automatic scaling occurs, the product of two numbers always has the least significant bit as a 0 unless an accumulation is performed with the least significant bit as a 1.

During a chain operation with the partial results not being read onto the bus, the machine will stay in either the fractional or integer mode. At the start of a sequence of operations, integer or fraction operation is designated by loading operands with Code 6 or Code 5 respectively.

Mixed fraction and integer working is possible by re-defining the weight of the least or most significant bit. Care, however, must be exercised due to the automatic scaling feature when fractional arithmetic is programmed.

Rounding

Rounding can be performed on the result of a multiplication or division. Generally rounding would only be called out during fractional operation but nothing in the machine precludes forming a rounded result during integer working.

Rounding for multiplication provides the best single length most significant half of the product. Rounding occurs at the end of a multiplication and is performed instead of a Load or Read operation. The machine looks at the most significant bit of the least significant half of the product (W_{15} or W_7) and adds 1 to the most significant half of the product at the least significant end if W_{15} (W_7) is a 1. After the operation the machine is in state 0 so that the rounded product can be read, and the W register is clear.

Division rounding is performed by forcing the least significant bit of the quotient in Z to a 1 unless the division is exact (remainder is zero). This method of rounding causes a slightly higher variance in the result than having an additional iterative division operation, but is considerably easier to perform. Again after rounding the machine goes to state 0 so that a read operation can be performed, and the W register is clear.

Overflow

The machine has an overflow output which is cleared prior to an operation and is set during an operation if the product or quotient goes outside the normally accepted range.

For multiplication, overflow can only occur if the most negative number in the operand range is used. $-1 \times -1 = +1$ which cannot be held in the machine. Overflow can more easily occur during accumulation of products either positively or negatively. For fractional working, if the product or accumulation goes outside the range of -1 to $+1 - 2^{-31}$ then the overflow flip-flop will be set.

Division overflow also occurs if the quotient goes outside the generally accepted number range of -1 to $+1 - 2^{-15}$ (2^{-7}) during fractional operation. This would occur if the divisor is less than the dividend or equal to the dividend if a positive quotient is being generated. For integer working the numbers must be scaled by 2^{15} (2^7).

Timing

General timing waveforms are shown in Figure 6. Specific examples are shown in Figures 7 and 8.

67518 16 x 16, 67508 8 x 8 Multiplier/Divider

CODE 1 ₂ 1 ₁ 1 ₀	STATE 0	1	2	3	MULTIPLY	DIVIDE	END MULTIPLY	END DIVIDE
0 0 0	X ₁ Y SM	XY	XY + Z	XY + Z, W	MULTIPLY	DIVIDE	X ₁ Y	X ₁ Y
LOAD								
MULT CLR POS								
0 0 1	-X ₁ Y SM	-XY	-XY + Z	-XY + Z, W	MULTIPLY	DIVIDE	-X ₁ Y	-X ₁ Y
LOAD								
MULT CLR NEG								
0 1 0	X, Y + KZ, KW SM	XY + KZ, KW	XY + KZ ² - ¹⁵	XY + Wsig.	MULTIPLY	DIVIDE	X ₁ Y + KZ, KW	X ₁ Y + KZ, KW
LOAD								
MULT POS								
0 1 1	-X, Y + KZ, KW SM	-XY + KZ, KW	-XY + KZ ² - ¹⁵	-XY + Wsig.	MULTIPLY	DIVIDE	-X ₁ Y + KZ, KW	-X ₁ Y + KZ, KW
LOAD								
MULT NEG								
1 0 0	$\frac{KZ, KW}{X_1}$ SD	$\frac{KW}{X}$	$\frac{Z, W}{X}$	$\frac{Wuns.}{X}$	MULTIPLE	DIVIDE	$\frac{KZ, KW}{X_1}$	$\frac{KZ, KW}{X_1}$
LOAD								
DIVIDE								
1 0 1	LOAD FR S1	$\frac{KZ}{X}$	$\frac{Z}{X}$	$\frac{Wsig.}{X}$	MULTIPLY	DIVIDE	ROUND MULTIPLY	ROUND DIVIDE
LOAD FR. & DIVIDE & RND.								
1 1 0	LOAD INT S1	LOAD	LOAD	LOAD	MULTIPLE	DIVIDE	LOAD	LOAD
LOAD INT.								
1 1 1	READ S0	READ	READ	READ	MULTIPLY	DIVIDE	READ	READ
READ								

KZ, KW PREVIOUSLY GENERATED Z, W
X₁ PREVIOUSLY LOADED X

Table 1 67516 (16 x 16) and 67508 (8 x 8) Multiplier/Divide State Table & Operations

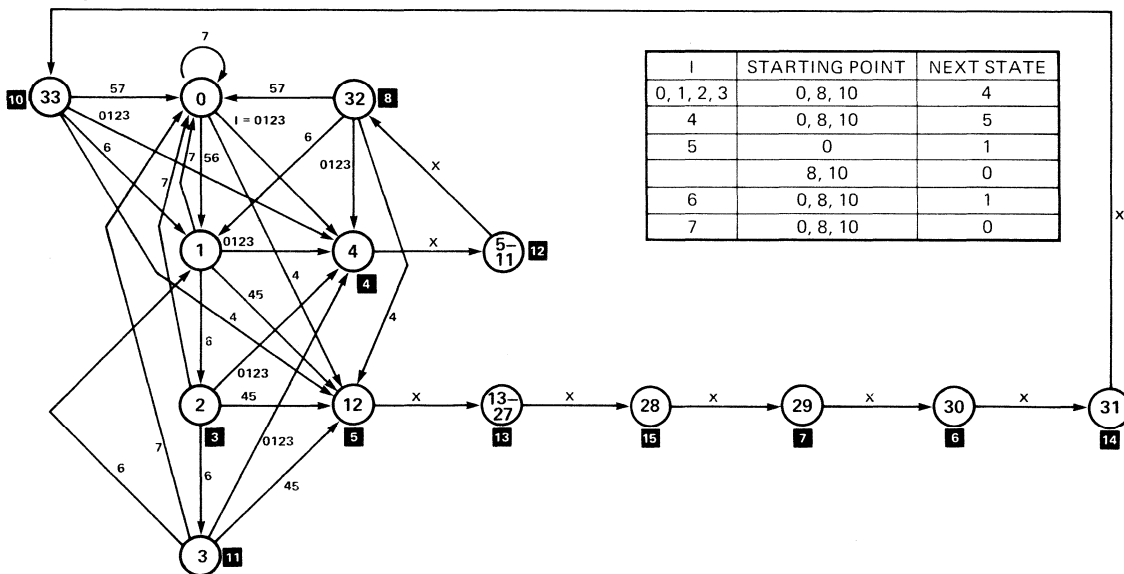


Figure 1 Transition Table Multiplier/Divider

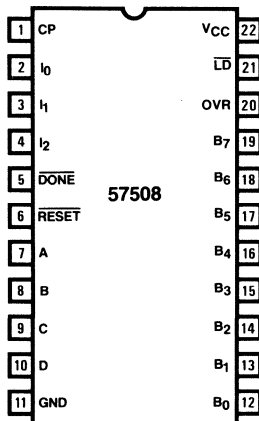
67518 16 x 16, 67508 8 x 8 Multiplier/Divider

OPERATION		TIME SLOT											
		1	2	3	4	5	6	7	8	9	10	11	12
X, Y	INS CODE	0											
	BUS	Y											
		MULTIPLY											
-X, Y	INS CODE	1											
	BUS	Y											
		MULTIPLY											
X, Y + K _Z , K _W	INS CODE	2											
	BUS	Y											
		MULTIPLY											
-X, Y + K _Z , K _W	INS CODE	3											
	BUS	Y											
		MULTIPLY											
XY	INS CODE	5/6	0										
	BUS	X	Y										
		MULTIPLY											
-XY	INS CODE	5/6	1										
	BUS	X	Y										
		MULTIPLY											
XY + K _Z , K _W	INS CODE	5/6	2										
	BUS	X	Y										
		MULTIPLY											
-XY + K _Z , K _W	INS CODE	5/6	3										
	BUS	X	Y										
		MULTIPLY											
XY + Z	INS CODE	5/6	6	0									
	BUS	X	Z	Y									
		MULTIPLY											
-XY + Z	INS CODE	5/6	6	1									
	BUS	X	Z	Y									
		MULTIPLY											
XY + K _Z 2 ⁻⁽ⁿ⁻¹⁾	INS CODE	5/6	6	2									
	BUS	X	-	Y									
		MULTIPLY											
-XY + K _Z 2 ⁻⁽ⁿ⁻¹⁾	INS CODE	5/6	6	3									
	BUS	X	-	Y									
		MULTIPLY											
XY + Z, W	INS CODE	5/6	6	6	0								
	BUS	X	Z	W	Y								
		MULTIPLY											
-XY + Z, W	INS CODE	5/6	6	6	1								
	BUS	X	Z	W	Y								
		MULTIPLY											
XY + Wsign	INS CODE	5/6	6	6	2								
	BUS	X	-	W	Y								
		MULTIPLY											
-XY + Wsign	INS CODE	5/6	6	6	3								
	BUS	X	-	W	Y								
		MULTIPLY											

- NOTES:
- 1) X1 IS CONTENTS OF 1ST RANK OF X REGISTER (EITHER OLD X OR A NEW X).
 - 2) K_Z2⁽ⁿ⁻¹⁾ IS A SINGLE LENGTH SIGNED NUMBER THE MOST SIGNIFICANT HALF OF THE PREVIOUS PRODUCT ADDED IN AT THE LEAST SIGNIFICANT END.
 - 3) W SIGN IS A SINGLE LENGTH SIGNED NUMBER.
 - 4) INTEGER OR FRACTIONAL WORKING IS SPECIFIED BY HAVING THE LAST BUT ONE OPERAND LOADED WITH A 6 OR 5 RESPECTIVELY.

Figure 2 Multiplication Codes and Times for 16 x 16 (For 8 x 8 Timing is Reduced by 4 Cycles)

8 x 8 Multiplier/Divider Pin-out



16 x 16 Multiplier/Divider Pin-out

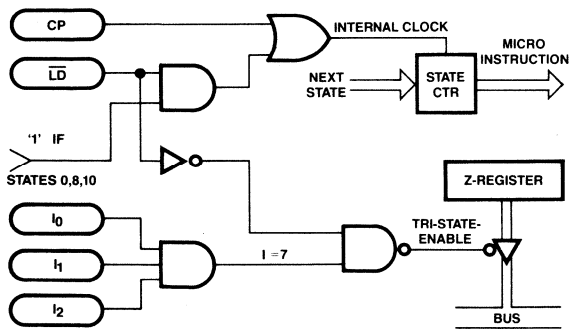
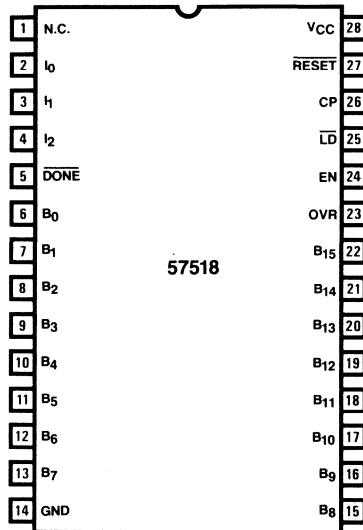
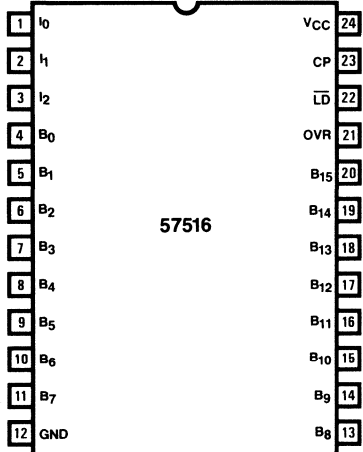


Figure 5. 67516/08 Internal Circuitry of "Load" Line and Tri-State-Enable.

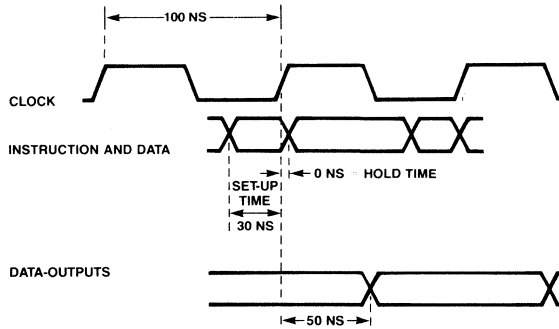


Figure 6. Timing Diagram 67516/67508 (Preliminary)

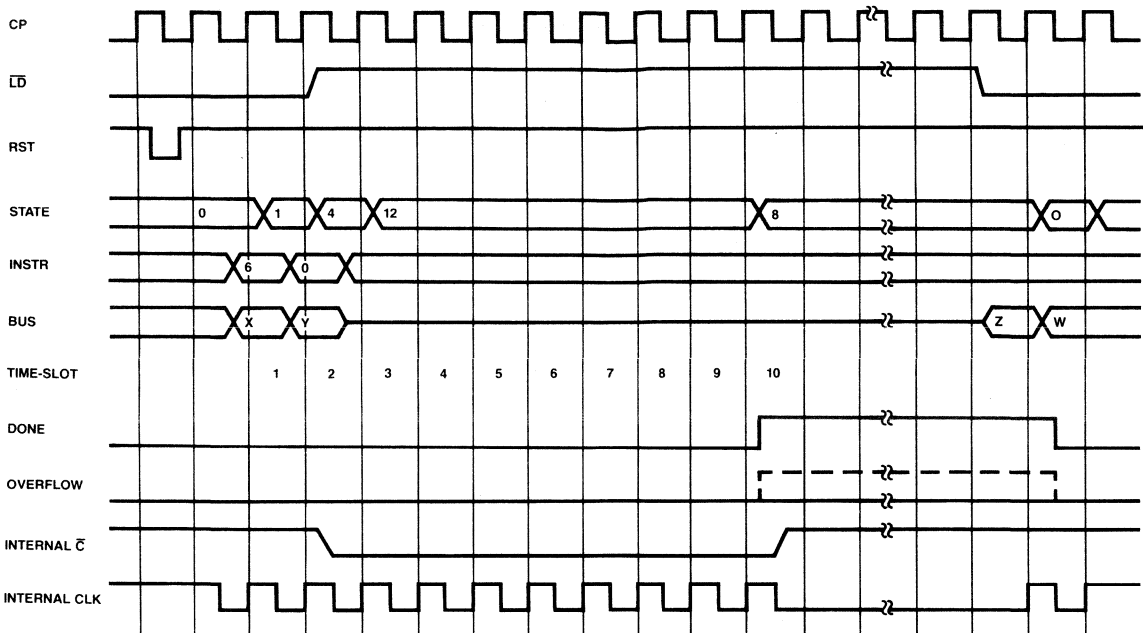


Figure 7. Example #1 Load X, Load Y, Multiply, Wait, Read Z, Read W.

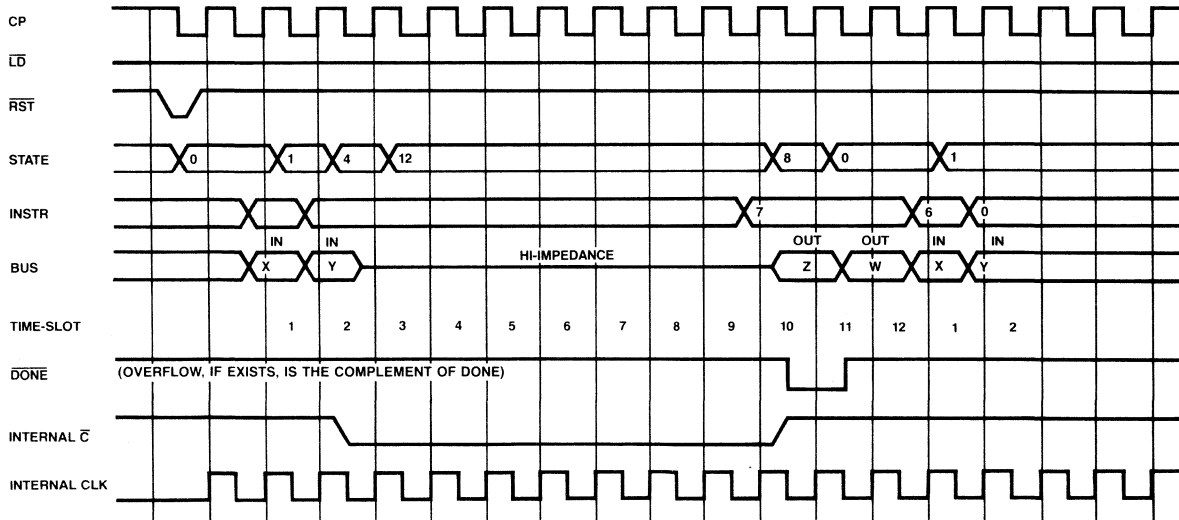


Figure 8. Example #2: Repeat: "Load X, Load Y, Multiply, Read Z, Read W".

Sine (0° to 90°) Look Up Table Using a 1024 X 10 ROM (5/6255, 5/6256) 5/6086, 5/6087

Features/Benefits

- Input angle increments of $90^\circ/1024 = .0879^\circ$
- 10 bit binary outputs
- Low power dissipation. Typically 500 mw
- Fast access time 100 ns max.
- DTL and TTL compatible
- Two enable inputs
- Advanced Schottky processing

PART NUMBER	PACKAGE	TEMPERATURE RANGE
6086/87N	N24	0°C to +70°C
6086/87J	J24	0°C to +70°C
5086/87J	J24	-55°C to +125°C

Description

The 5255/6255, 1024 words by 10 bits Read Only Memory has been customized to make a sine θ look up table (5086/6086) for $0^\circ \leq \theta < 90^\circ$. The address inputs are used to divide the first 90° quadrant into angles increments of $90^\circ/1024$ words or $.0879^\circ$ /word. The memory outputs should be interpreted as binary

weighted fractions where output 1 has a weight of 1/2 or .500, output 2 has a weight of 1/4 or .250, and so on until output 10 which has a weight of 1/1024 or .000976. The 10 bit output code has not been rounded off so that output error will always be positive and less than 1/1024 or .0009765. Round off error, in approximating the ROM input word, must be added or subtracted to the output error.

EXAMPLE 1:

Find the sine 45°

Let X = the ROM word where sine 45° is stored

$$\frac{X}{1024 \text{ words}} = \frac{45^\circ}{90^\circ}$$

X = word 512

Word 511 has the following stored data and interpretation:

Output #	0 ₁	0 ₂	0 ₃	0 ₄	0 ₅	0 ₆	0 ₇	0 ₈	0 ₉	0 ₁₀	
Stored Data	H	L	H	H	L	H	L	H	L	L	(H = TTL HIGH)
Binary Weight	$\frac{1}{2}$	$\frac{1}{4}$	$\frac{1}{8}$	$\frac{1}{16}$	$\frac{1}{32}$	$\frac{1}{64}$	$\frac{1}{128}$	$\frac{1}{256}$	$\frac{1}{512}$	$\frac{1}{1024}$	

Adding the fractions wherever an "H" appears given.

$$\frac{1}{2} + \frac{1}{8} + \frac{1}{16} + \frac{1}{64} + \frac{1}{256} = .50000 + .12500 + .06250 + .01562 + .00391 = .70507$$

Handbook Value = .70711

Our Error = .70711 - .70703 = .00008

EXAMPLE 2:

Find the sine 210°

This value is in quadrant three, therefore, $\theta' = 210^\circ - 180^\circ$ or 30°

Let X = the ROM word where sine 30° is stored $\frac{X}{1024 \text{ words}} = \frac{30^\circ}{90^\circ}$

X = word 341.33 (round off to word 341)

Word 341's stored data = 0₁ 0₂ 0₃ 0₄ 0₅ 0₆ 0₇ 0₈ 0₉ 0₁₀ ◀ Output

Binary Weight = $\frac{1}{2}$ $\frac{1}{4}$ $\frac{1}{8}$ $\frac{1}{16}$ $\frac{1}{32}$ $\frac{1}{64}$ $\frac{1}{128}$ $\frac{1}{256}$ $\frac{1}{512}$ $\frac{1}{1024}$ ◀ Stored Data Not Presented

= .49902

The sine 210° , therefore, = -.49902 with the sign generated by external logic. Note that the address 341 to which we rounded off is actually the sine 29.97° .

8

Absolute Maximum Ratings

Supply voltage V_{CC}	-0.5V to +7.0V
Input voltage	-1.5V to +5.5V
Input current	-20 mA to +5 mA
Output current	-100 mA to +100 mA
Storage temperature range	-65°C to +150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.75	5.00	5.25	V
I_{OL}	Low level operating current			6			6	mA
T_A	Operating free air temperature	-55	25	125	0	25	75	°C

Electrical Characteristics

Over Recommended Operating Free Air Temperature Range (Unless Otherwise Noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High level input voltage		2.0			V
V_{IL}	Low level input voltage				0.8	V
V_{IC}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18\text{mA}$		-1.0	-1.5	V
V_{OL}	Low level output voltage	$V_{CC} = \text{MIN}, I_{OL} = \text{MAX}$.45	V
I_I	Maximum input current	$V_{CC} = \text{MAX}, V_I = 5.5\text{V}$			1.0	mA
I_{IH}	High level input current	$V_{CC} = \text{MAX}, V_I = 2.4\text{V}$			40	μA
I_{IL}	Low level input current	$V_{CC} = \text{MAX}, V_I = 0.45\text{V}$			-250	μA
C_I	Input capacitance	$V_{CC} = 5.0\text{V}, f = 1\text{MHz}, V_I = 2.0\text{V}$		7		pF
C_O	Output capacitance	$T_A = 25^\circ\text{C}, V_O = 2.0\text{V}$		8		
I_{CC}	Supply current	$V_{CC} = \text{MAX}$, all inputs grounded, all outputs open			165	mA

OPEN COLLECTOR OUTPUT CURRENT

I_{CEX}	Output leakage current	$V_{CC} = \text{MAX}, V_O = 2.4\text{V}$	100	mA
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THREE STATE OUTPUT ONLY

V_{OH}	High level output voltage	$V_{CC} = \text{MIN}, I_{OH} = \text{MAX}$	2.4	3.2		V
I_{HZ}	High level off State output current	$V_{CC} = \text{MAX}, V_O = 2.4\text{V}$			50	μA
I_{LZ}	Low level off State output current	$V_{CC} = \text{MAX}, V_O = 0.5\text{V}$			-50	μA
I_{OS}	Output short circuit current	$V_{CC} = 5.0\text{V}, V_O = 0\text{V}$	-20	-50	-90	mA

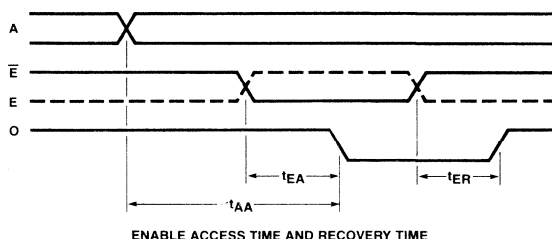
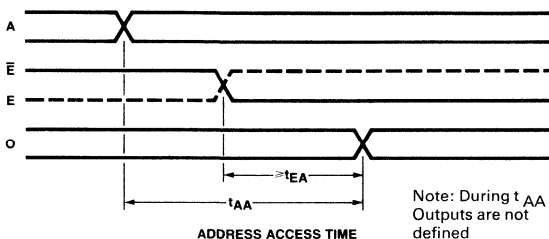
Switching Characteristics

Over Recommended Ranges of T_A and V_{CC}

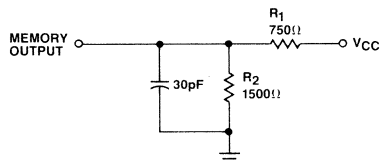
SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY*		COMMERCIAL*		UNIT
			MIN	MAX	MIN	MAX	
T_{AA}	Address access time	Any address reading "0" or "1"		150		100	ns
T_{ER}	Enable recovery time	Word addressed is storing a low		45		40	ns
T_{EA}	Enable access time	Word addressed is storing a low		80		70	ns

* All limits apply for $5V \pm 5\%$, $0^\circ C$ to $+75^\circ C$ for Commercial. All limits apply for $5V \pm 10\%$, $-55^\circ C$ to $+125^\circ C$ for Military.

Definition of Waveforms



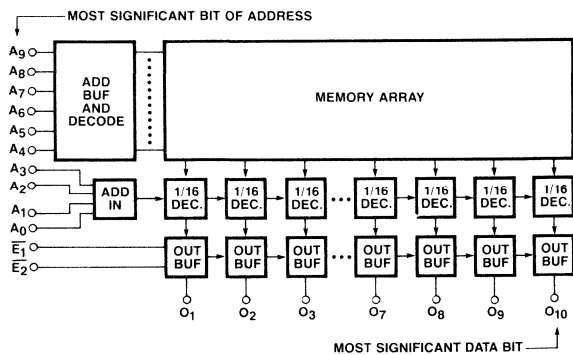
Standard Test Load



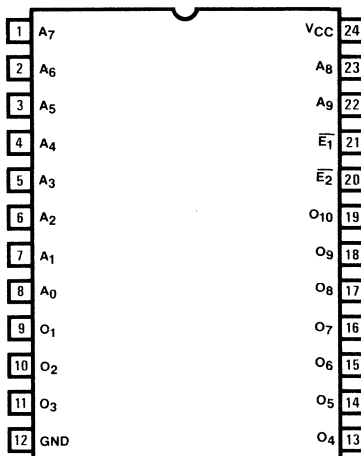
Input pulse amplitude 3.0V
 Input rise and fall times 5ns from 1.0V to 2.0V
 Measurements made at 1.5V

Block Diagram:

1024 words X 10 bits memory

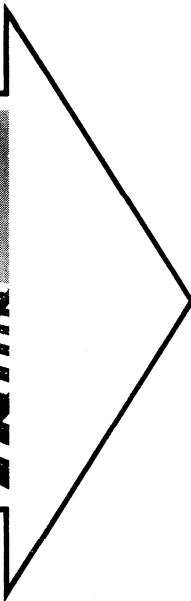
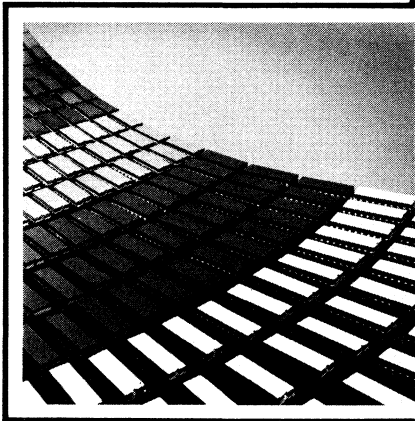


Pin Configuration



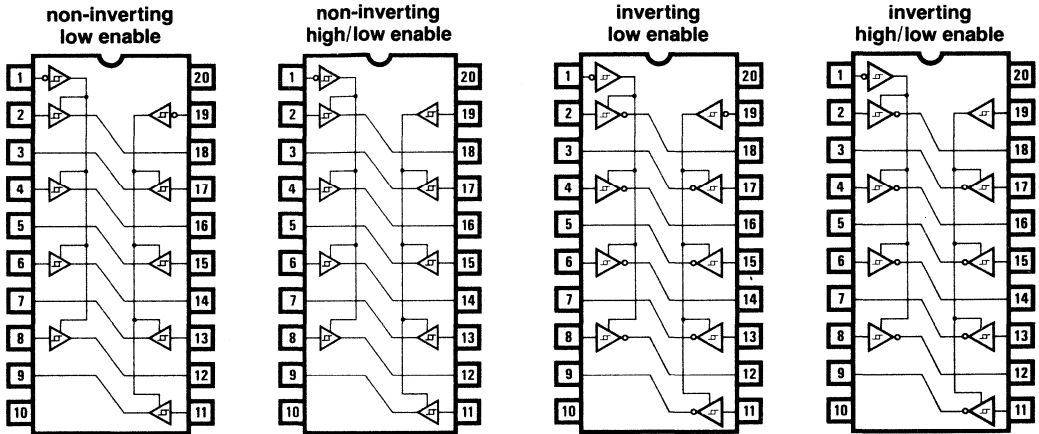
ENABLE = \bar{E}_1 LOW AND \bar{E}_2 LOW



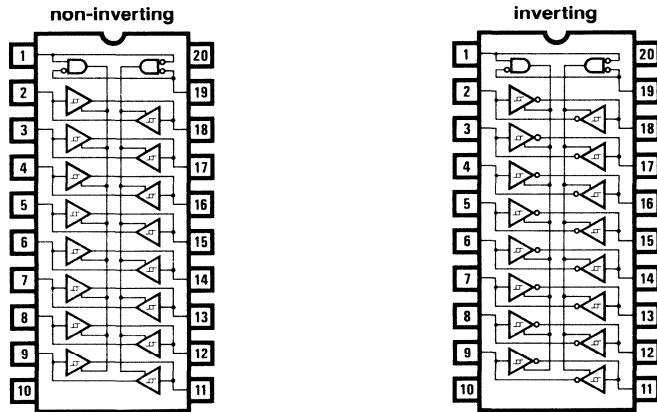


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PROMS	2
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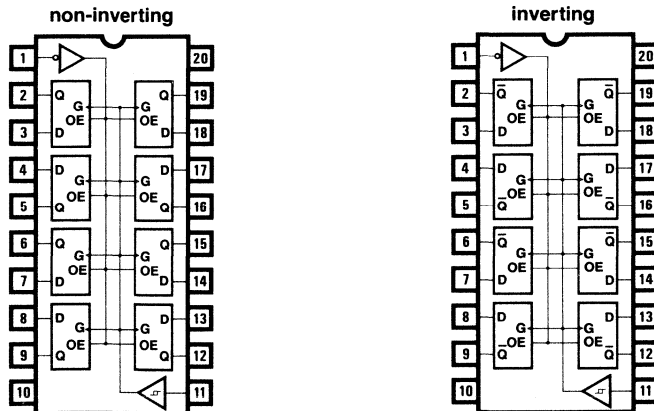
Octal Buffers



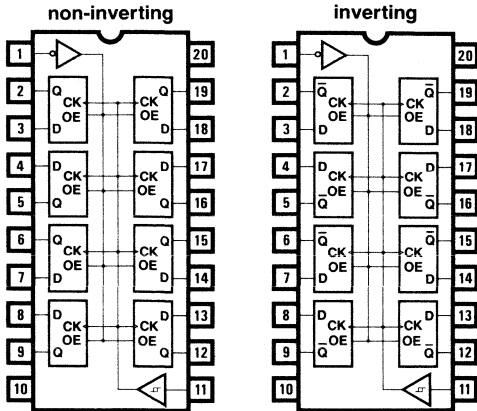
Octal Transceivers



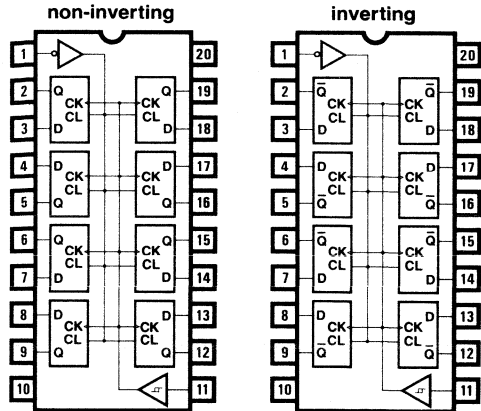
Octal Latches



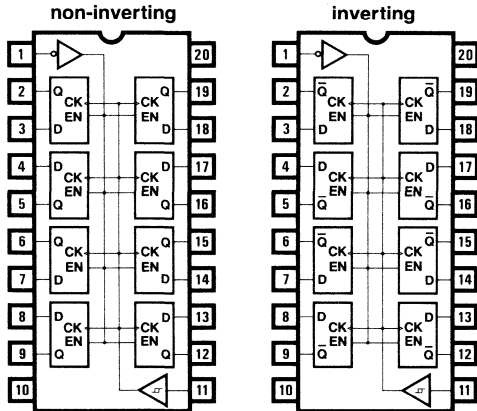
Octal Registers with Three-state Page 9-14



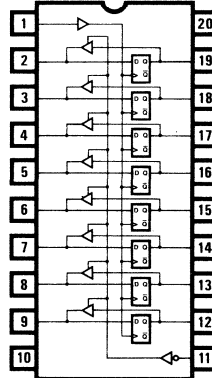
Octal Registers with Clear Page 9-18



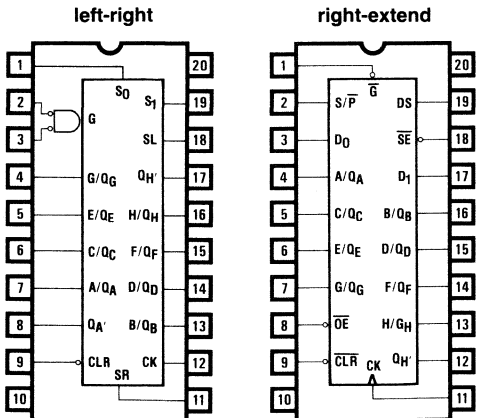
Octal Registers with Clock Enable Page 9-18



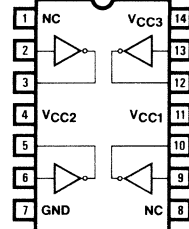
Octal Registers with I/O Page 9-21



Octal Shift Registers Page 9-22



Quad Power/Logic Strobe Page 9-26



Octal Buffers

Features/Benefits

- 3-state outputs drive bus lines
- Schmitt trigger guarantees high noise margin
- Low current PNP inputs reduce loading
- 20-pin Skinny DIP™ saves space
- 8-bits matches byte boundaries
- Ideal for microprocessor interface

PART NUMBER	PKG	TEMP.	ENABLE	POLARITY	THRESH-OLD	POWER
SN74LS240 SN54LS240	N,J J	com mil	LOW	Invert	Hysteresis	LS
67LS306 57LS306	N,J J	com mil	LOW-HIGH			
SN74LS244 SN54LS244	N,J J	com mil	LOW	Non-invert		
SN74LS241 SN54LS241	N,J J	com mil	LOW-HIGH			
67LS300 57LS300	N,J N	com mil	LOW	Invert	Schmitt trigger	
67LS307 57LS307	N,J N	com mil	LOW-HIGH			
67LS304 57LS304	N,J N	com mil	LOW	Non-invert		
67LS301 57LS301	N,J N	com mil	LOW-HIGH			
SN74S240 SN54S240	N,J N	com mil	LOW	Invert	Hysteresis	S
67S306 57S306	N,J N	com mil	LOW-HIGH			
SN74S244 SN54S244	N,J N	com mil	LOW	Non-invert		
SN74S241 SN54S241	N,J N	com mil	LOW-HIGH			
67S300 57S300	N,J N	com mil	LOW	Invert	Schmitt trigger	
67S307 57S307	N,J N	com mil	LOW-HIGH			
67S304 57S304	N,J N	com mil	LOW	Non-Invert		
67S301 57S301	N,J N	com mil	LOW-HIGH			

Description

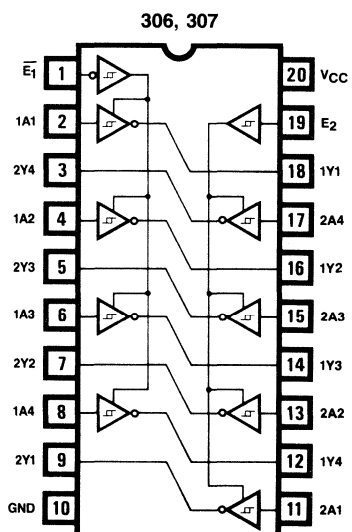
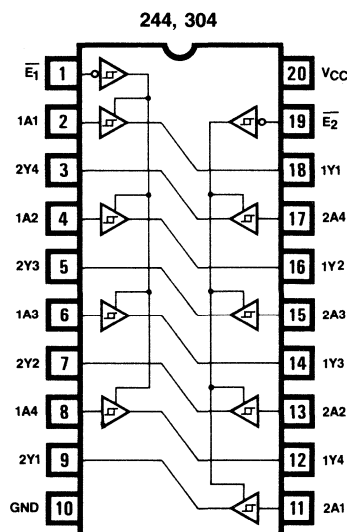
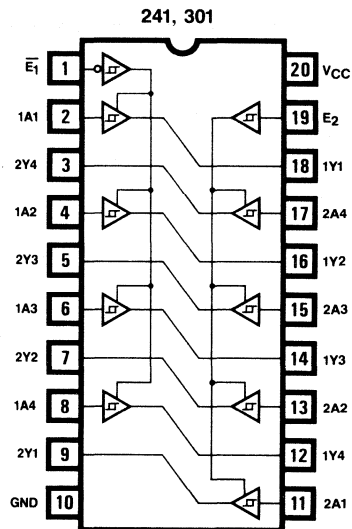
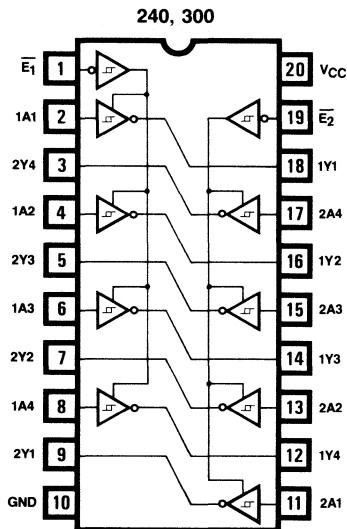
The Octal Buffers provide high speed and high current interface capability for bus organized Digital Systems. The three-state drivers will source a termination to ground (up to 133Ω) or sink a pull-up to V_{CC} as in the popular 220Ω/330Ω computer peripheral termination. The PNP inputs provide improved fan-in with 0.2 mA I_{IL} on the Low Power Schottky buffers and 0.4 mA I_{OC} on the Schottky buffers.

The 240 and 244 provide inverting and non-inverting outputs with active low enables. The 241 and 306 provide inverting and non-inverting outputs with both active low and active high enables allowing transceiver operation.

In addition to the standard Schottky and Low Power Schottky Octal Buffers, Monolithic Memories provides a full hysteresis with "a true" Schmitt trigger circuit. The improved performance characteristics are designed to be consistent with the SN54/74LS14 Hex Schmitt trigger and guarantee a full 400 mV noise immunity.

The Schmitt Trigger operation makes the LS buffers ideal for bus receivers in a noisy environment. The Schmitt Trigger operation on the S buffers acts as a safeguard against feedback oscillation and prevents slow transitions through the threshold region, insuring fast transitions and reducing I_{CC} spikes.

Logic Symbols



Absolute Maximum Ratings

Supply Voltage, V _{CC}	7V
Input Voltage	7V
Off-State Output Voltage	7V
Storage Temperature Range	-65°C to +150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I _{OH}	High-level output current			-12			-15	mA
I _{OL}	Low-level output current			12			24	mA
T _A	Operating free-air temperature	-55		125	0		70	°C

Electrical Characteristics Over Recommended Operating Free Air Temperature Range

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.7			0.8	V
V _{IC}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
	Hysteresis (V _{T+} - V _{T-})	V _{CC} = MIN	0.2	0.4		0.2	0.4		V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, I _{OH} = -3mA	2.4	3.4		2.4	3.4		V
		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.5 V, I _{OH} = MAX	2			2			
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} MAX, I _{OL} = 12 mA			0.4			0.4	V
		I _{OL} = 24 mA					0.5		
I _{OZH}	Off-state output current	V _{CC} , V _{IL} = MAX, V _{IH} = 2 V	V _O = 2.7 V			20			μA
I _{OZL}			V _O = 0.4 V			-20			
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 7 V			0.1			0.1	mA
I _{IH}	High-level input current, any input	V _{CC} = MAX, V _I = 2.7 V			20			20	μA
I _{IL}	Low-level input current	V _{CC} = MAX, V _{IL} = 0.4 V			-0.2			-0.2	mA
I _{OS}	Short-circuit output current	V _{CC} = MAX	-40		-225	-40		-225	mA
I _{CC}	Supply current	V _{CC} = MAX	Outputs high	All	13	23	13	23	mA
				'LS240, 'LS306	26	44	26	44	
			Outputs low	'LS241, 'LS244	27	46	27	46	
				'LS240, 'LS306	29	59	29	50	
All outputs disabled	Outputs open	'LS241, 'LS244	32	54	32	54			

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS	LS240, LS306			LS241, LS244			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH}	Propagation delay, low-to-high	C _L = 45 pF, R _L = 667 Ω, See Page 10-4	9	14		12	18		ns
t _{PHL}	Propagation delay, high-to-low		12	18		12	18		ns
t _{pZL}	Output enable time to low level		20	30		20	30		ns
t _{pZH}	Output enable time to high level		15	23		15	23		ns
t _{PLZ}	Output disable time from low level		C _L = 5 pF, R _L = 667 Ω, See Page 10-4	15	25		15	25	
t _{PHZ}	Output disable time from high level		10	18		10	18		ns

THIS IS NOT A FINAL DESIGN. THE INFORMATION CONTAINED HEREIN IS SUBJECT TO CHANGE WITHOUT NOTICE.

Absolute Maximum Ratings

Supply Voltage, VCC	7V
Input Voltage	7V
Off-state output voltage	7V
Storage temperature range	-65°C to +150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
VCC	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
IOH	High-level output current			-12			-15	mA
IOL	Low-level output current			12			24	mA
TA	Operating free-air temperature	-55		125	0		70	°C

Electrical Characteristics Over Recommended Operating Free Air Temperature Range

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY			COMMERCIAL			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX		
VT+	Positive-going threshold voltage	VCC = 5V	1.5	1.7	2.0	1.5	1.7	2.0	V	
VT-	Negative-going threshold voltage	VCC = 5V	0.6	0.9	1.1	0.6	0.9	1.1	V	
VIC	Input clamp voltage	VCC = MIN, I _I = -18 mA			-1.5			-1.5	V	
	Hysteresis (VT+ - VT-)	VCC = 5V	0.4	0.8		0.4	0.8		V	
VOH	High-level output voltage	VCC = MIN, VIH = 2 V, VIL = MAX, IOH = -3mA VCC = MIN, VIH = 2 V, VIL = 0.5 V, IOH = MAX	2.4	3.4		2.4	3.4		V	
VOL	Low-level output voltage	VCC = MIN, VIH = 2 V, VIL = VIL MAX IOL = 12 mA IOL = 24 mA			0.4			0.4	V	
IOZH	Off-state output current	VCC, VIL = MAX VIH = 2 V	VO = 2.7 V			20			μA	
IOZL			VO = 0.4 V			-20				
II	Input current at maximum input voltage	VCC = MAX, VI = 7 V			0.1			0.1	mA	
IIH	High-level input current, any input	VCC = MAX, VI = 2.7 V			20			20	μA	
IIL	Low-level input current	VCC = MAX, VIL = 0.4 V			-0.2			-0.2	mA	
IOS	Short-circuit output current	VCC = MAX	-40		-225	-40		-225	mA	
ICC	Supply current	Outputs high	VCC = MAX	LS300, LS307	13	23	13	23	mA	
				LS301, LS304	18	31	18	31		
		Outputs low		LS300, LS307	26	44	26	44		
				LS301, LS304	32	46	32	46		
		All outputs disabled		Outputs open	LS300, LS307	29	59	29		50
					LS301, LS304	34	54	34		54



Switching Characteristics VCC = 5 V, TA = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS	LS300, LS307			LS301, LS304			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
tPLH	Propagation delay, low-to-high	CL = 45 pF, RL = 667 Ω, See Page 10-4	19			19			ns
tPHL	Propagation delay, high-to-low		19			19			ns
tpZL	Output enable time to low level		37			26			ns
tpZH	Output enable time to high level		26			26			ns
tPLZ	Output disable time from low level		CL = 5 pF, RL = 667 Ω, See Page 10-4	19			22		
tPHZ	Output disable time from high level	19			22			ns	

Absolute Maximum Ratings

Supply Voltage, V _{CC}	7V
Input Voltage	5.5V
Off-state output voltage	5.5V
Storage temperature range	-65°C to +150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I _{OH}	High-level output current			-12			-15	mA
I _{OL}	Low-level output current			48			64	mA
T _A	Operating free-air temperature	-55		125*	0		70	°C

*The SN54S241/244J operating at free air temperature above 116°C requires a heat sink such that R_{θCA} is not more than 40°C/W

Electrical Characteristics Over Recommended Operating Free Air Temperature Range

SYMBOL	PARAMETER		CONDITIONS	S240, S306			S241, S244			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V _{IH}	High-level input voltage			2			2			V
V _{IL}	Low-level input voltage			0.8			0.8			V
V _{IC}	Input clamp voltage		V _{CC} = MIN, I _I = -18mA	-1.2			-1.2			V
	Hysteresis (V _{T+} - V _{T-})		V _{CC} = MIN	0.2	0.4		0.2	0.4		V
V _{OH}	High-level output voltage	V _{CC} = MIN V _{IH} = 2V	74S	V _{IL} = 0.8V, I _{OH} = -1mA		2.7		2.7		V
			54S 74S	V _{IL} = 0.8V, I _{OH} = -3mA		2.4	3.4	2.4	3.4	
			54S 74S	V _{IL} = 0.5V, I _{OH} = MAX		2		2		
V _{OL}	Low-level output voltage		V _{CC} = MIN, V _{IH} = 2V V _{IL} = 0.8V, I _{OL} = MAX	0.55			0.55			V
I _{OZH}	Off-state output current		V _{CC} = MAX V _{IH} = 2V V _{IL} = 0.8V	V _O = 2.4V	50		50		μA	
I _{OZL}				V _O = 0.5V	-50		-50			
I _I	Maximum input current		V _{CC} = MAX, V _I = 5.5V	1			1			mA
I _{IH}	High-level input current		V _{CC} = MAX, V _I = 2.7V	50			50			μA
I _{IL}	Low-level input current	Any A	V _{CC} = MAX, V _I = 0.5V	-400			-400			μA
		Any E		-2			-2			mA
I _{OS}	Short circuit output current ¹		V _{CC} = MAX	-50	-225		-50	-225	mA	
I _{CC}	Supply current	Outputs high	V _{CC} = MAX Outputs Open	Military	80	123	95	147	mA	
				Commercial	80	135	95	160		
		Outputs low		Military	100	145	120	170		
				Commercial	100	150	120	180		
		Outputs disabled		Military	100	145	120	170		
				Commercial	100	150	120	180		

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS	S240, S306			S241, S244			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH}	Data to output delay	C _L = 50 pF R _L = 90Ω	4.5	7		6	9	ns	
t _{PHL}			4.5	7		6	9	ns	
t _{PZL}	Output enable delay	See Page 10-4	10	15		10	15	ns	
t _{PZH}			6.5	10		8	12	ns	
t _{PLZ}	Output disable delay	C _L = 5 pF See R _L = 90Ω Page 10-4	10	15		10	15	ns	
t _{PHZ}			6	9		6	9	ns	

Absolute Maximum Ratings

Supply Voltage, VCC	7V
Input Voltage	5.5V
Off-state output voltage	5.5V
Storage temperature range	-65°C to +150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
VCC	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
IOH	High-level output current			-12			-15	mA
IOL	Low-level output current			48			64	mA
TA	Operating free-air temperature	-55		125*	0		70	°C

*The SN54S241/244J operating at free air temperature above 116°C requires a heat sink such that RθCA is not more than 40°C/W

Electrical Characteristics Over Recommended Operating Free Air Temperature Range

SYMBOL	PARAMETER		CONDITIONS	S300, S307,			S301, S304			UNIT	
				MIN	TYP	MAX	MIN	TYP	MAX		
VT+	Positive going threshold voltage		VCC = 5V	1.5	1.7	1.9	1.5	1.7	1.9	V	
VT-	Negative-going threshold voltage		VCC = 5V	0.7	0.9	1.1	0.7	0.9	1.1	V	
VIC	Input clamp voltage		VCC = MIN, I _I = -18mA			-1.2			-1.2	V	
	Hysteresis (VT+ - VT-)		VCC = MIN 5V	0.4	0.8		0.4	0.8		V	
VOH	High-level output voltage	VCC = MIN VIH = 2V	74S VIL = 0.8V, IOH = -1mA	2.7			2.7			V	
			54S 74S VIL = 0.8V, IOH = -3mA	2.4	3.4		2.4	3.4			
			54S 74S VIL = 0.5V, IOH = MAX	2			2				
VOL	Low level output voltage		VCC = MIN, VIH = 2V VIL = 0.8V, IOL = MAX			0.55			0.55	V	
IOZH	Off state output current		VCC = MAX VIH = 2V VIL = 0.8V	VO = 2.4V				50		50	μA
IOZL					VO = 0.5V				-50		
II	Maximum input current		VCC = MAX, VI = 5.5V			1			1	mA	
IIH	High level input current		VCC = MAX, VI = 2.7V			50			50	μA	
IIL	Low level input current	Any A	VCC = MAX, VI = 0.5V				-400		-400	μA	
		Any E					-400		-400		
IOS	Short circuit output current ¹		VCC = MAX	-50		-225	-50		-225	mA	
ICC	Supply current	Outputs high Outputs low Outputs disabled	VCC = MAX Outputs Open	Military			123		147	mA	
				Commercial			135		160		
				Military	100	145		120	170		
				Commercial	100	150		120	180		
				Military	100	145		120	170		
				Commercial	100	150		120	180		



Switching Characteristics VCC = 5 V, TA = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS	S300, S307			S301, S304			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
tPLH	Data to output delay	CL = 50 pF RL = 90Ω							ns
tPHL									ns
tPZL	Output enable delay	See Page 10-4							ns
tPZH									ns
tPLZ	Output disable delay	CL = 5 pF See RL = 90Ω Page 10-4							ns
tPHZ									ns

Octal Transceiver

SN74LS245, SN54LS245

67LS305, 67LS310, 57LS305, 57LS310

Features/Benefits

- 3-state outputs drive bus lines
- Schmitt trigger guarantees high noise margin
- Low current PNP inputs reduce loading
- 20 pin Skinny DIP™ saves space
- 8 bits matches byte boundaries
- Ideal for microprocessor interface

Description

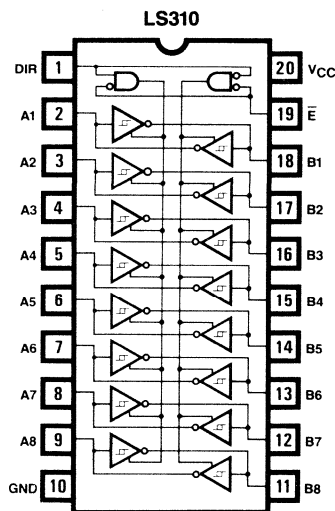
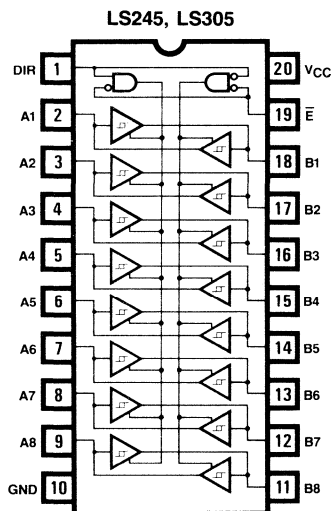
These Octal Bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input (\bar{E}) can be used to disable the device so that the buses are effectively isolated.

In addition to the standard Octal transceivers, Monolithic Memories provides a full hysteresis with "a true" Schmitt Trigger circuit. The improved performance characteristics are designed to be consistent with the SN54/74LS14 Hex Schmitt Trigger and guarantee a full 400 mV noise immunity.

The Schmitt Trigger operation makes these LS transceivers ideal for noisy bus environments.

Logic Symbols



PART NUMBER	PKG	TEMP	POLARITY	THRESHOLD
SN74LS245 SN54LS245	N,J J	com mil	Non-invert	Hysteresis
67LS305* 57LS305*	N,J J	com mil	Non-invert	Schmitt trigger
67LS310* 57LS310*	N,J J	com mil	Invert	

Function Table LS245, LS305

ENABLE \bar{E}	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

Function Table LS310

ENABLE \bar{E}	DIRECTION CONTROL DIR	OPERATION
L	L	\bar{B} data to A bus
L	H	\bar{A} data to B bus
H	X	Isolation

Absolute Maximum Ratings

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Off-State Output Voltage	7V
Storage Temperature Range	-65°C to +150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current			-12			-15	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

Electrical Characteristics

Over Recommended Operating Free Air Temperature Range

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY			COMMERCIAL			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IC}	Input clamp voltage		$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
	Hysteresis ($V_{T+} - V_{T-}$) A or B input		$V_{CC} = \text{MIN}$	0.2	0.4		0.2	0.4		V
V_{OH}	High-level output voltage		$V_{CC} = \text{MIN}, V_{IH} = 2V, V_{IL} = V_{IL \text{ max}}$ $I_{OH} = -3 \text{ mA}$ $I_{OH} = \text{MAX}$	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		$V_{CC} = \text{MIN}, V_{IH} = 2V, V_{IL} = V_{IL \text{ max}}$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$		0.4			0.4		V
I_{OZH}	Off-state output current		$V_{CC} = \text{MAX}, \bar{E}$ at 2 V		10			10		μA
I_{OZL}				200		200				
I_I	Input current at maximum input voltage	A or B DIR, \bar{E}	$V_{CC} = \text{MAX}, V_I = 5V$ $V_I = 7V$		0.1			0.1		mA
I_{IH}	High-level input current		$V_{CC} = \text{MAX}, V_{IH} = 2.7 V$		20			20		μA
I_{IL}	Low-level input current		$V_{CC} = \text{MAX}, V_{IL} = 0.4 V$		-0.2			-0.2		mA
I_{OS}	Short-circuit output current		$V_{CC} = \text{MAX}$	-40	-225		-40	-225		mA
I_{CC}	Supply current	Total, outputs high	$V_{CC} = \text{MAX},$ Outputs open	48	70		48	70		mA
		Total, outputs low		68	90		88	90		
		Outputs at Hi-Z		64	95		64	95		

Switching Characteristics $V_{CC} = 5 V, T_A = 25^\circ\text{C}$

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay, low-to-high	$C_L = 45 \text{ pF}, R_L = 667 \Omega,$ See Page 10-4				ns
t_{PHL}	Propagation delay, high-to-low					ns
t_{PZL}	Output enable time to low-level					ns
t_{PZH}	Output enable time to high-level					ns
t_{PLZ}	Output disable time from low-level	$C_L = 5 \text{ pF}, R_L = 667 \Omega,$ See Page 10-4				ns
t_{PHZ}	Output disable time from high-level					ns

Absolute Maximum Ratings

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Off-State Output Voltage	7V
Storage Temperature Range	-65°C to +150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current			-12			-15	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

Electrical Characteristics

Over Recommended Operating Free Air Temperature Range

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{T+}	Positive-going threshold voltage	$V_{CC} = 5V$	1.5	1.7	1.9	1.5	1.7	1.9	V
V_{T-}	Negative-going threshold voltage	$V_{CC} = 5V$	0.7	0.9	1.1	0.7	0.9	1.1	V
V_{T-}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
	Hysteresis ($V_{T+} - V_{T-}$) A or B input	$V_{CC} = \text{MIN}$	0.4	0.8		0.4	0.8		V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2V, V_{IL} = V_{IL \text{ max}}$	$I_{OH} = -3 \text{ mA}$	2.4	3.4		2.4	3.4	V
			$I_{OH} = \text{MAX}$	2			2		
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2V, V_{IL} = V_{IL \text{ max}}$	$I_{OL} = 12 \text{ mA}$		0.4			0.4	V
			$I_{OL} = 24 \text{ mA}$					0.5	
I_{OZH}	Off-state output current	$V_{CC} = \text{MAX}, \bar{E} \text{ at } 2 \text{ V}$	$V_O = 2.7 \text{ V}$		10			10	μA
I_{OZL}			$V_O = 0.4 \text{ V}$		-200			-200	
I_I	Input current at maximum Input voltage	A or B DIR, \bar{E}	$V_{CC} = \text{MAX}, V_I = 5.5V, V_I = 7V$		0.1			0.1	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_{IH} = 2.7 \text{ V}$			20			20	μA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_{IL} = 0.4 \text{ V}$			-0.2			-0.2	mA
I_{OS}	Short-circuit output current	$V_{CC} = \text{MAX}$	-40		-225	-40		-225	mA
I_{CC}	Supply current	Total, outputs high	$V_{CC} = \text{MAX},$ Outputs open						mA
		Total, outputs low		62	90		62	90	
		Outputs at Hi-Z		64	95		64	95	

Switching Characteristics $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

SYMBOL	PARAMETER	TEST CONDITIONS	CS305, LS310			LS310			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay, low-to-high	$C_L = 45 \text{ pF}, R_L = 667 \Omega$ See Page 10-4							ns
t_{PHL}	Propagation delay, high-to-low								ns
t_{PZL}	Output enable time to low-level								ns
t_{PZH}	Output enable time to high-level								ns
t_{PLZ}	Output disable time from low-level	$C_L = 5 \text{ pF},$ See $R_L = 667 \Omega$ Page 10-4							ns
t_{PHZ}	Output disable time from high-level								ns

Octal Latches, Octal Registers With Three-State Outputs

Features/Benefits

- Inverting and Non-Inverting Outputs
- Up to 32 mA I_{OL}
- 3-State Outputs Drive Bus Lines
- 20 Pin Skinny DIP™ Saves Space
- 8 Bits Matches Byte Boundaries
- Hysteresis Improves Noise Margin
- Low Current PNP Inputs Reduce Loading
- Ideal for Microprocessor Interface

Latch Function Table

\overline{OE}	G	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

Register Function Table

\overline{OE}	CK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

Inverting Latch Function Table

\overline{OE}	G	D	\overline{Q}
L	H	H	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

Inverting Register Function Table

\overline{OE}	CK	D	\overline{Q}
L	↑	H	L
L	↑	L	H
L	L	X	Q_0
H	X	X	Z

PART NUMBER	PKG	TEMP	I_{OL}	POLARITY	TYPE	POWER
SN74LS373	N,J	com mil	24mA	Non-invert	Latch	LS
SN54LS373	J	com mil	12mA	Invert		
67LS380	N,J	com mil	24mA	Non-invert	Register	
57LS380	J	com mil	12mA			
SN74LS374	N,J	com mil	24mA	Invert	Register	
SN54LS374	J	com mil	12mA			
67LS376	N,J	com mil	24mA	Non-invert	Latch	S
57LS376	J	com mil	12mA			
SN74S373	N,J	com mil	20mA	Non-invert	Latch	
SN54S373	J	com mil	12mA			
67S373	N,J	com mil	32mA	Invert	Register	
57S373	J	com mil	20mA			
67S380	N,J	com mil	20mA	Non-invert	Register	
57S380	J	com mil	32mA			
67S382	N,J	com mil	32mA	Non-invert	Register	
57S382	J	com mil	20mA			
SN74S374	N,J	com Mil	20mA	Invert	Register	
SN54S374	J	com mil	32mA			
67S374	N,J	com mil	20mA	Non-invert	Register	
57S374	J	com mil	32mA			
67S376	N,J	com mil	20mA	Invert	Register	
57S376	J	com mil	32mA			
67S378	N,J	com mil	20mA	Non-invert	Register	
57S378	J	com mil	32mA			

Description

The latch passes eight (octal) bits of data from the inputs (D) to the outputs (Q) when the gate (G) is high. The data is "latched" when the gate (G) goes low. The register loads eight (octal) bits of input data and passes it to the output on the "rising edge" of the clock.

The three state outputs are active when OE is low, and high impedance when OE is high. Schmitt-trigger buffers at the gate/clock inputs improve system noise margin by providing typically 400 mV of hysteresis.

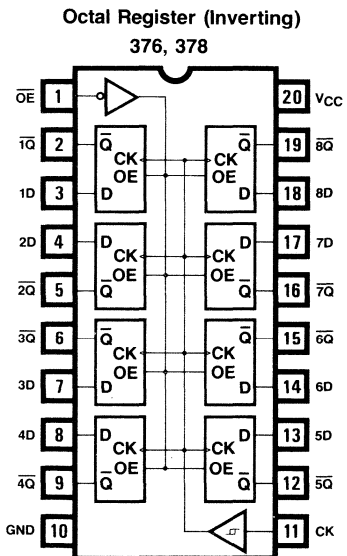
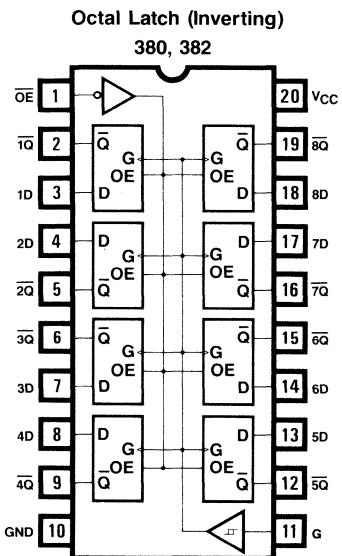
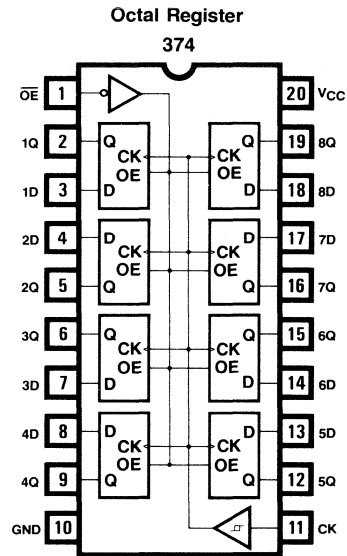
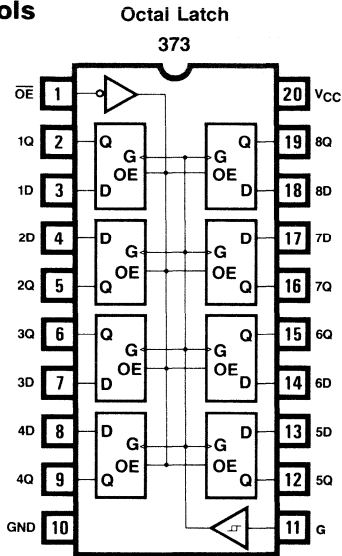
In addition to the standard S and LS latches and Registers, Monolithic Memories provides these enhancements:

- 1) Increased output sink current (I_{OL}) from the standard Schottky I_{OL} of 20 mA to an improved 32 mA.
- 2) Inverting outputs instead of the standard non-inverting outputs.

The higher I_{OL} is intended for upgrading systems which presently satisfy 32 mA requirements with SN54/74365, 366, 367, 368, Hex Buffers. The inverting outputs are intended for bus applications that require inversion as in interfacing the Am2901A 4-Bit Slice to an active low bus.

All of the octal devices are packaged in the popular 20 in. Skinny DIP.[™]

Logic Symbols



Absolute Maximum Ratings

Supply Voltage, V _{CC}	7V
Input Voltage	5.5V
Off-State Output Voltage	5.5V
Storage Temperature Range	-65°C to +150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX		
V _{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V	
V _{OH}	High Level Output Voltage			5.5			5.5	V	
I _{OH}	High Level Output Current			-1			-2.6	mA	
t _w	Width of Clock/Gate	High		15			15	ns	
		Low		15			15		
t _{SU}	Set Up Time	'LS373		0↓			0↓	ns	
		'LS374		20↑			20↑		
t _H	Hold Time	'LS373		10↓			10↓	ns	
		'LS374		0↑			0↑		
T _A	Operating Free Air Temperature			-55		125	0	70	°C

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY			COMMERCIAL			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX		
V _{IH}	High-level input voltage		2			2			V	
V _{IL}	Low-level input voltage				0.8			0.8	V	
V _{IC}	Input clamp voltage	V _{CC} = MIN, I _I = -18mA			-1.5			-1.5	V	
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} MAX, I _{OH} = MAX	2.4	3.4		2.4	3.1		V	
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} MAX	I _{OL} = 12 mA	0.25	0.4	0.25	0.4	V		
			I _{OL} = 24 mA			0.35	0.5			
I _{OZH}	High off-state current	V _{CC} = MAX, V _{IH} = 2V, V _O = 2.7 V			20			20	μA	
I _{OZL}	Low off-state current	V _{CC} = MAX, V _{IH} = 2 V, V _O = 0.4 V			-20			-20	μA	
I _I	Input current at max V _I	V _{CC} = MAX, V _I = 7 V			0.1			0.1	mA	
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7 V			20			20	μA	
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.4 V			-0.4			-0.4	mA	
I _{OS}	Short-circuit current	V _{CC} = MAX			-30			-130	mA	
I _{CC}	Supply current	V _{CC} MAX	Latch		24	40		24	40	mA
			Register		27	40		27	40	

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	LATCH			REGISTER			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f _{MAX}	Maximum Clock Frequency	C _L = 45pF R _L = 667Ω See Page 10-4				35	50		MHz
t _{PLH}	Data to Output Delay			12	18				ns
t _{PHL}				12	18				
t _{PLH}	Clock/Gate to Output Delay			20	30		15	28	ns
t _{PHL}				18	30		19	28	
t _{PZH}	Output Enable Delay			15	28		20	28	ns
t _{PZL}				25	36		21	28	
t _{PHZ}	Output Disable Delay		C _L = 5pF See R _L = 667Ω Page 10-4		12	20		12	20
t _{PLZ}				15	25		14	25	

Absolute Maximum Ratings

Supply Voltage, V_{CC}	7V
Input Voltage	5.5V
Off-State Output Voltage	5.5V
Storage Temperature Range	-65°C to +150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OH}	High Level Output Current			-2			-6.5	mA
t_W	Width of Clock/Gate	High	6		6			ns
		Low	7.3		7.3			ns
t_{SU}	Set Up Time	Latch	0↓		0↓			ns
		Register	5↑		5↑			ns
t_H	Hold Time	Latch	10↓		10↓			ns
		Register	2↑		2↑			ns
T_A	Operating Free Air Temperature	-55	125		0	70		°C

Electrical Characteristics Over Recommended Operating Free Air Temperature Range

SYMBOL	PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT	
V_{IH}	High Level Input Voltage			2			V	
V_{IL}	Low Level Input Voltage					0.8	V	
V_{IC}	Input Clamp Voltage		$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2	V	
V_{OH}	High Level Output Voltage		$V_{CC} = \text{MIN}, V_{IH} = 2V, I_{OH} = \text{MAX}$ $V_{IL} = 0.8V$	2.4	3.1		V	
V_{OI}	Low Level Output Voltage	SN54/74S373 57/67S380	$V_{CC} = \text{MIN}$ $V_{IL} = 0.8V$ $V_{IH} = 2V$	$I_{OL} = 20 \text{ mA}$		0.5	V	
		SN54/74S374 57/67S376						
		57/67S373 57/67S382		$I_{OL} = 32 \text{ mA}$				
		57/67S374 57/67S378						
I_{HZ}	High Level Off-State Output Current		$V_{CC} = \text{MAX}, V_O = 2.4V, V_{IH} = 2V$			50	μA	
I_{LZ}	Low Level Off-State Output Current		$V_{CC} = \text{MAX}, V_O = 0.5V, V_{IH} = 2V$			-50	μA	
I_I	Input Current at MAX V_I		$V_{CC} = \text{MAX}, V_I = 5.5V$			1	mA	
I_{IH}	High Level Input Current		$V_{CC} = \text{MAX}, V_I = 2.7V$			50	μA	
I_{IL}	Low Level Input Current		$V_{CC} = \text{MAX}, V_I = 0.5V$			-250	μA	
I_{OS}	Output Short Circuit Current		$V_{CC} = \text{MAX}$	-40		-100	mA	
I_{CC}	Supply Current	Latch	$V_{CC} = \text{MAX}$			105	160	mA
		Register	$V_{CC} = \text{MAX}$			90	140	mA

Switching Characteristics $V_{CC} = 5V, T_A = 25^\circ\text{C}$

SYMBOL	PARAMETER	CONDITIONS	LATCH			REGISTER			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{MAX}	Maximum Clock Frequency	$C_L = 15 \text{ pF}$ $R_L = 280\Omega$ See Page 10-4				75	100		MHz
t_{PLH}	Data to Output Delay		5	9					ns
t_{PHL}			9	13					ns
t_{PLH}	Clock/Gate to Output Delay		7	14		8	15		ns
t_{PHL}			12	18		11	17		ns
t_{PZH}	Output Enable Delay		8	15		8	15		ns
t_{PZL}			11	18		11	18		ns
t_{PHZ}	Output Disable Delay	$C_L = 5\text{pF}$ See	6	9		5	9		ns
t_{PLZ}		$R_L = 280\Omega$ Page 10-4	8	12		7	12		ns



Octal Registers With Clear and Clock Enable

Features

- Inverting and non-inverting outputs
- Slim 20-pin Skinny DIP™ saves space
- 8 bits matches byte boundaries
- Ideal for microprogram instruction register
- Ideal for microprocessor interface

Description

These Octal registers contain 8 D-type flip-flops and feature very low I_{CC} (17 mA typ). The LS273 and LS313 registers are loaded on the rising edge of the clock (CK) and asynchronously cleared whenever the CLEAR line is low. The LS377 and LS314 are loaded on the rising edge of the clock provided the clock enable line, CK EN is low.

PART NUMBER	PKG	TEMP	POLARITY	CONTROL OPTION
SN74LS273	N,J	com	Non-invert	Clear
SN54LS273	J	mil	Invert	
67LS313	N,J	com	Invert	
57LS313	J	mil	Invert	Clock Enable
SN74LS377	N,J	com	Non-invert	
SN54LS377	J	mil	Non-invert	
67LS314	N,J	com	Invert	
57LS314	J	mil	Invert	

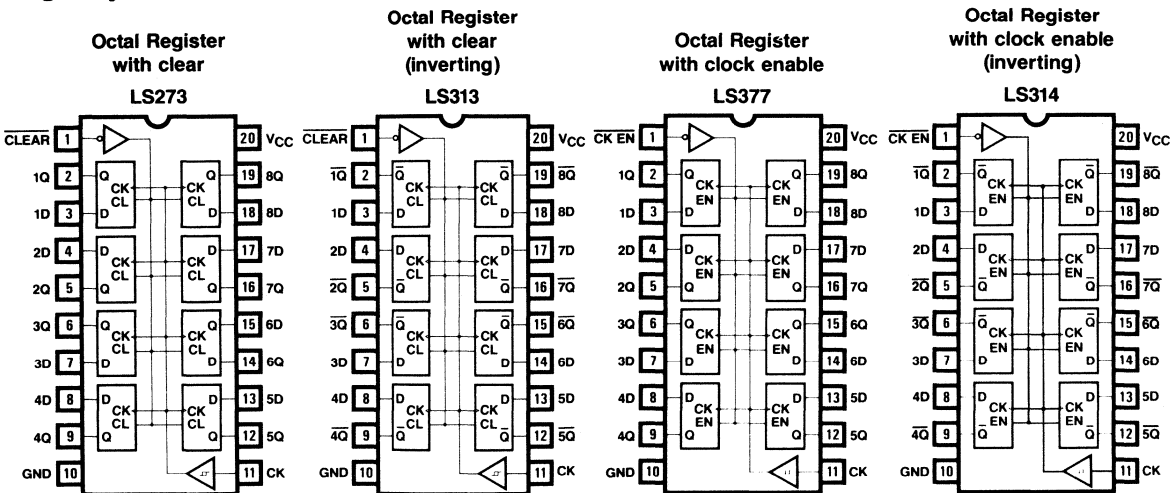
Function Table LS273, LS313

INPUTS			OUTPUT	
CLEAR	CLOCK	D	Q	\bar{Q}
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	\bar{Q}_0

Function Table LS377, LS314

INPUTS			OUTPUTS	
CK EN	CLOCK	DATA	Q	\bar{Q}
H	X	X	Q_0	\bar{Q}_0
L	↑	H	H	L
L	↑	L	L	H
X	L	X	Q_0	\bar{Q}_0

Logic Symbols



Absolute Maximum Ratings

Supply Voltage, V _{CC}	7V
Input Voltage	7V
Off-State Output Voltage	7V
Storage Temperature Range	-65°C to +150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I _{OH}	High-level output current			-400			-400	μA
I _{OL}	Low-level output current			4			8	mA
f _{clock}	Clock frequency	0		30	0		30	MHz
t _w	Width of clock or clear pulse	20			20			ns
t _{su}	Set-up time	Data input		20↑		20↑		ns
		Clear inactive state		25↑		25↑		
		Enable active state		25↑		25↑		
		Enable inactive state		10↑		10↑		
t _h	Data hold time	5↑			5↑			ns
T _A	Operating free-air temperature	-55		125	0		70	°C

Electrical Characteristics

Over Recommended Operating Free-Air Temperature Range

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY			COMMERCIAL			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX		
V _{IH}	High-level input voltage		2			2			V	
V _{IL}	Low-level input voltage				0.8			0.8	V	
V _{HC}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V	
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{ILMAX} , I _{OH} = -400 μA	2.5	3.4		2.7	3.4		V	
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{ILMAX}			0.25	0.4	0.25	0.4	V	
		I _{OL} = 4 mA I _{OL} = 8 mA					0.35	0.5		
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 7 V			0.1			0.1	mA	
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7 V			20			20	μA	
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = -0.4 V			-0.4			-0.4	mA	
I _{OS}	Short-Circuit output current	V _{CC} = MAX	-20		-100	-20		-100	mA	
I _{CC}	Supply current	V _{CC} = MAX,	LS273						mA	
			LS315		17	27		17		27
			LS377							
			LS314		17	28		17		28



Switching Characteristics, V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{MAX}	Maximum clock frequency		30	40		MHz
t _{PHL}	Propagation delay time, high-to-low-level output from clear	C _L = 15 pF, R _L = 2 kΩ, See Page 10-4		18	27	ns
t _{PLH}	Propagation delay time, low-to-high-level output from clock			17	27	ns
t _{PHL}	Propagation delay time, high-to-low-level output from clock			18	27	ns

Octal Register with I/O

67LS315 57LS315

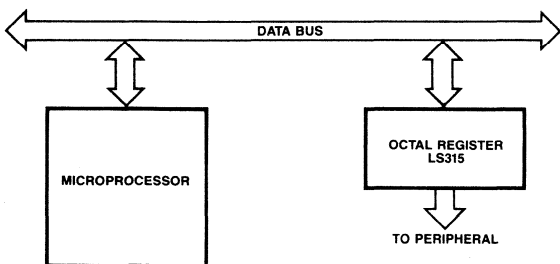
Features/Benefits

- I/O port enables output data back to input bus
- 20 pin skinny DIP saves space
- 8 bits matches byte boundaries
- Ideal for microprocessor I/O ports

PART NUMBER	PACKAGE	TEMPERATURE
67LS315	N,J	com
57LS315	J	mil

Description

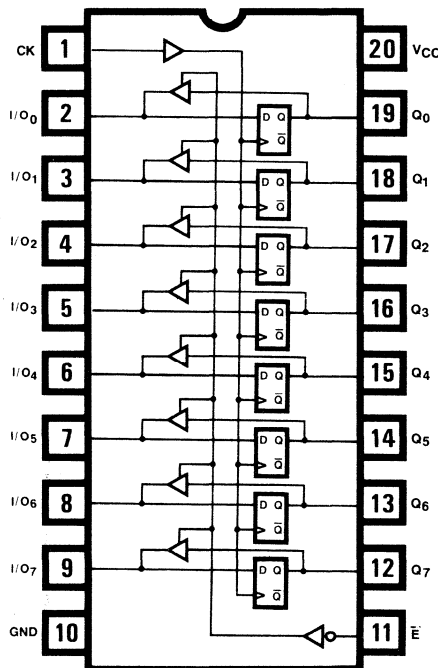
The Octal register with I/O is designed for use on a microprocessor bus where it is necessary to read the output data back on to the input bus.



This operation is important in control algorithms which make decisions based on previous status of output controls. Rather than keeping a redundant copy of the output control data in memory, the 57/67LS15 allows the control data to be quickly retrieved by simply reading the register as an I/O port.

The register is similar to the S54/74LS374 as 8 bit data is loaded on the low to high transition of the clock. When the enable line \bar{E} is lowered, the output data (which is always enabled to the output port) is then enabled back on the I/O port. The driving characteristics of the I/O port are consistent with the SN54/74LS240.

Logic Symbol



Function Table

\bar{E}	CK	I/O	Q
H	↑	L	L
H	↑	H	H
L	x	L	L
L	x	H	H

x either high or low, not in transition

Octal Shift Registers

SN74LS299, SN74LS322, SN74LS323, SN54LS299, SN54LS322, SN54LS323

Features/Benefits

- 3-state outputs drive bus lines
- 20 pin skinny DIP saves space
- 8 bits matches byte boundaries
- Synchronous or asynchronous clear
- Sign extend
- Ideal for microprocessor interface

PART NUMBER	PKG	TEMP	CLEAR	TYPE
SN74LS299 SN54LS299	N,J J	com mil	Async	Left- Right
SN74LS323 SN54LS323	N,J J	com mil	Sync	
SN74LS322 SN54LS322	N,J J	com mil	Async	Right- Extend

Description

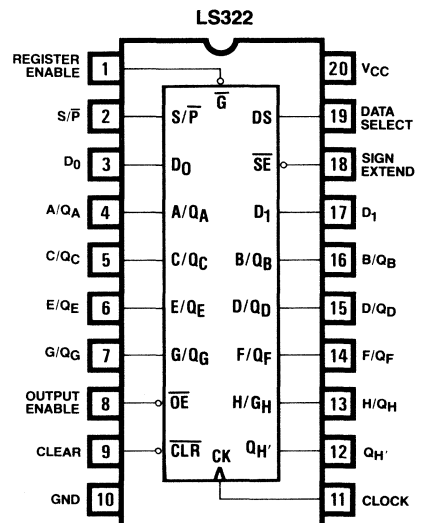
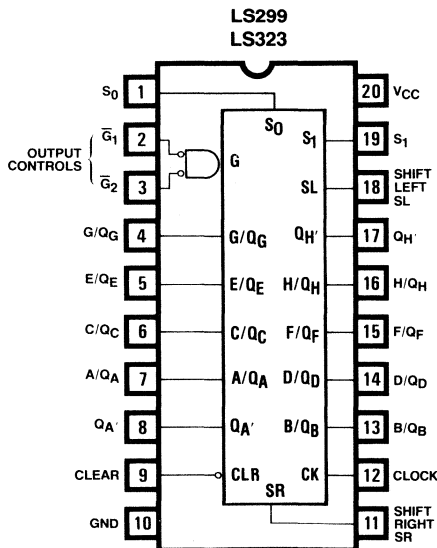
These Low Power Schottky Octal Registers feature a multiplexed I/O bus to achieve full eight-bit data handling in a single 20 pin skinny dip. Function selects and output controls are used to choose the modes of operation listed in the function table.

Synchronous parallel loading occurs on the low to high transition of the clock when appropriate levels are applied to the func-

tion select. A low on the clear input will synchronously clear the LS323 and asynchronously clear the LS299 and LS322.

Synchronous shifting occurs on the low to high transition of the clock when appropriate levels are applied to the function select. The LS299 and LS323 shift either left or right. The LS322 shifts only right where the shift-in data is D₀, D₁ or sign. The sign shift allows an arithmetic shift on the most significant data byte.

Logic Symbols



Function Table LS299

MODE	INPUTS						INPUTS/OUTPUTS								OUTPUTS			
	CLEAR	FUNCTION SELECT		OUTPUT CONTROL		CLOCK	SERIAL		A/Q _A	B/Q _B	C/Q _C	D/Q _D	E/Q _E	F/Q _F	G/Q _G	H/Q _H	Q _A '	Q _H '
		S ₁	S ₀	G ₁ ¹	G ₂ ¹		SL	SR										
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
Hold	H	L	L	L	L	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{E0}	Q _{F0}	Q _{G0}	Q _{H0}	Q _{A0}	Q _{H0}
	H	X	X	L	L	L	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{E0}	Q _{F0}	Q _{G0}	Q _{H0}	Q _{A0}	Q _{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	H	Q _{Gn}
	H	L	H	L	L	↑	X	L	L	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	L	Q _{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	Q _{Hn}	H	Q _{Bn}	H
	H	H	L	L	L	↑	L	X	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	Q _{Hn}	L	Q _{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

¹When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

Function Table LS323

MODE	INPUTS						INPUTS/OUTPUTS								OUTPUTS			
	CLEAR	FUNCTION SELECT		OUTPUT CONTROL		CLOCK	SERIAL		A/Q _A	B/Q _B	C/Q _C	D/Q _D	E/Q _E	F/Q _F	G/Q _G	H/Q _H	Q _A '	Q _H '
		S ₁	S ₀	G ₁ ¹	G ₂ ¹		SL	SR										
Clear	L	X	L	L	L	↑	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	↑	X	X	L	L	L	L	L	L	L	L	L	L
Hold	H	L	L	L	L	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{E0}	Q _{F0}	Q _{G0}	Q _{H0}	Q _{A0}	Q _{H0}
	H	X	X	L	L	L	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{E0}	Q _{F0}	Q _{G0}	Q _{H0}	Q _{A0}	Q _{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	H	Q _{Gn}
	H	L	H	L	L	↑	X	L	L	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	L	Q _{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	Q _{Hn}	H	Q _{Bn}	H
	H	H	L	L	L	↑	L	X	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	Q _{Hn}	L	Q _{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

¹When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.



Function Table LS322

MODE	INPUTS							INPUTS/OUTPUTS				OUTPUT Q _H
	CLEAR	REGISTER ENABLE	S/P	SIGN EXTEND	DATA SELECT	OUTPUT ENABLE	CLOCK	A/Q _A	B/Q _B	C/Q _C	H/Q _H	
Clear	L	H	X	X	X	L	X	L	L	L	L	L
	L	X	H	X	X	L	X	L	L	L	L	L
Hold	H	H	X	X	X	L	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{H0}	Q _{H0}
Shift Right	H	L	H	H	L	L	↑	D ₀	Q _{An}	Q _{Bn}	Q _{Gn}	Q _{Gn}
	H	L	H	H	H	L	↑	D ₁	Q _{An}	Q _{Bn}	Q _{Gn}	Q _{Gn}
Sign Extend	H	L	H	L	X	L	↑	Q _{An}	Q _{An}	Q _{Bn}	Q _{Gn}	Q _{Gn}
Load	H	L	L	X	X	X	↑	a	b	c	h	h

When the output enable is high, the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected. If both the register enable input and the S/P input are low while the clear input is low, the register is cleared while the eight input/output terminals are disabled to the high-impedance state.

Absolute Maximum Ratings

Supply Voltage, V _{CC}	7V
Input Voltage	7V
Off-State Output Voltage	7V
Storage Temperature Range	-65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MILITARY			COMMERCIAL			UNIT	
			MIN	NOM	MAX	MIN	NOM	MAX		
V _{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V	
I _{OH}	High-level output current	Q _A thru Q _H	-1			-2.6			mA	
		Q _H '	-0.4			-0.4				
I _{OL}	Low-level output current	Q _A thru Q _H	12			24			mA	
		Q _H '	4			8				
f _{clock}	Clock frequency		0	35		0	35		MHz	
t _w (clock)	Width of clock pulse	LS322	Clock high	14		14		ns		
			Clock low	14		14				
		LS299 LS323	Clock high	20		20		ns		
			Clock low	20		20				
t _w (clear)	Width of clear pulse		Clear low		20		20		ns	
t _{su}	Setup time	Data select		30↑		30↑		ns		
		High-level data		20↑		20↑				
		Low-level data		20↑		20↑				
		Clear inactive-state		20↑		20↑				
t _h	Hold time	Data select		10↑		10↑		ns		
		Data		0↑		0↑				
T _A	Operating free-air temperature		-55		125		0		70	°C

Electrical Characteristics

Over Recommended Operating Free-Air Temperature Range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.7			0.8	V
V _{IC}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5			-1.5	V
V _{OH}	High-level output voltage	Q _A thru Q _H	V _{CC} = MIN, V _{IH} = 2 V,	2.4	3.2	2.4	3.1		V
		Q _H '	V _{IL} = V _{ILMAX} , I _{OH} = MAX	2.7	3.4	2.7	3.4		
V _{OL}	Low-level output voltage	Q _A thru Q _H	V _{CC} = MIN, I _{OL} = 12 mA		0.25	0.4	0.25	0.4	V
			V _{IH} = 2 V, I _{OL} = 24 mA				0.35	0.5	
		Q _H '	V _{IL} = V _{ILMAX} , I _{OL} = 4 mA		0.25	0.4	0.25	0.4	
			I _{OL} = 8 mA				0.35	0.5	
I _{OZH}	Off-state output current, high-level voltage applied	Q _A thru Q _H	V _{CC} = MAX, V _O = 2.7 V, V _{IH} = 2 V,		40		40		μA
I _{OZL}	Off-state output current, low-level voltage applied	Q _A thru Q _H	V _{CC} = MAX, V _O = 0.4 V, V _{IH} = 2 V,		-400		-400		μA
I _I	Input current at maximum input voltage	A thru H	V _{CC} = MAX	V _I = 5.5 V		0.1		0.1	mA
		Data select		V _I = 7 V		0.2		0.2	
		Sign extend		V _I = 7 V		0.3		0.3	
		Any other		V _I = 7 V		0.1		0.1	
I _{IH}	High-level input current	A thru H, DS	V _{CC} = MAX, V _I = 2.7 V			40		40	μA
		Sign extend				60		60	
		Any other				20		20	
I _{IL}	Low-level input current	Data select	V _{CC} = MAX, V _I = 0.4 V			-0.8		-0.8	mA
		Sign extend				-1.2		-1.2	
		Any other				-0.4		-0.4	
I _{OS}	Short-circuit output current	Q _A thru Q _H	V _{CC} = MAX		-30	-130	-30	-130	mA
		Q _H			-20	-100	-20	-100	
I _{CC}	Supply current		V _{CC} = MAX		35	60	35	60	mA

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{MAX}				35	50		MHz
t _{PLH}	Clock	Q _A ' or Q _H '	C _L = 15 pF, R _L = 2 kΩ, See Page 10-4		15	25	ns
t _{PHL}					15	25	
t _{PHL}	Clear	Q _A ' or Q _H '			20	35	ns
t _{PLH}					15	25	
t _{PHL}	Clock	Q _A thru Q _H	C _L = 45 pF, R _L = 665Ω, See Page 10-4		15	25	ns
t _{PHL}					15	25	
t _{PHL}	Clear	Q _A thru Q _H			20	35	ns
t _{PZH}					20	35	
t _{PZL}	Output enable	Q _A thru Q _H			20	35	ns
t _{PZL}					20	35	
t _{PHZ}	Output enable	Q _A thru Q _H	C _L = 5 pF, R _L = 665Ω, See Page 10-4		15	25	ns
t _{PLZ}					15	25	



Quad Power/Logic Strobe

HD1-6600-5/HD1-6605-5
HD1-6600-2/HD1-6605-2

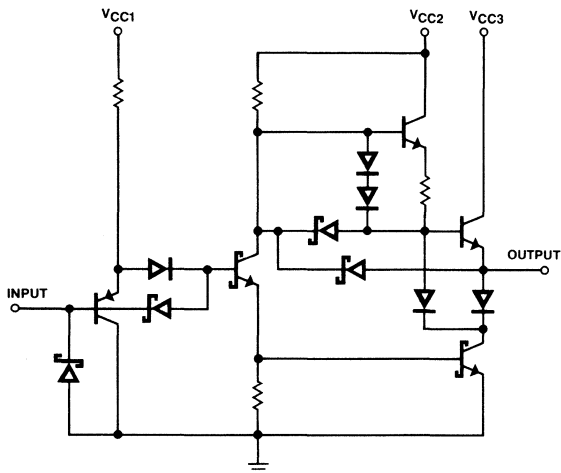
Features/Benefits

- High Drive Current—200 ma
- High Speed—40 ns typical
- Low fan-in (250 μ a Max), TTL COMPATIBLE
- Low Power Standby 30 mw/circuit
Active 120 mw/circuit

Description

The HD-6600 Quad Power strobe and the HD-6605 Quad Logic strobe are four high current drivers used for Power Down mode of ROM/PROM and other Logic devices. V_{CC} can be removed from nonactive devices and reduce total system power.

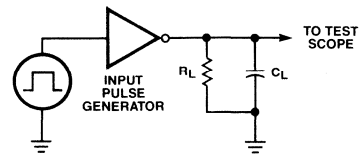
Block Diagram



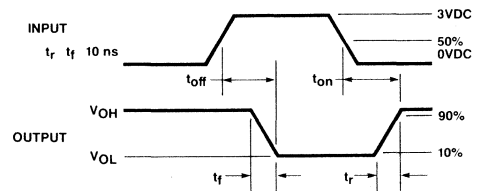
PART NUMBER	PACKAGE	TYPE	TEMPERATURE RANGE
HD1-6600-5	J14	Power	0°C to +75°C
HD1-6605-5	J14	Logic	0°C to +75°C
HD1-6600-2	J14	Power	-55°C to +125°C
HD1-6605-2	J14	Logic	-55°C to +125°C

Parts suffixed -8 are equivalent to parts suffixed -2 screened in accordance with MIL-STD 883 method 5004, Class B.

Test Load

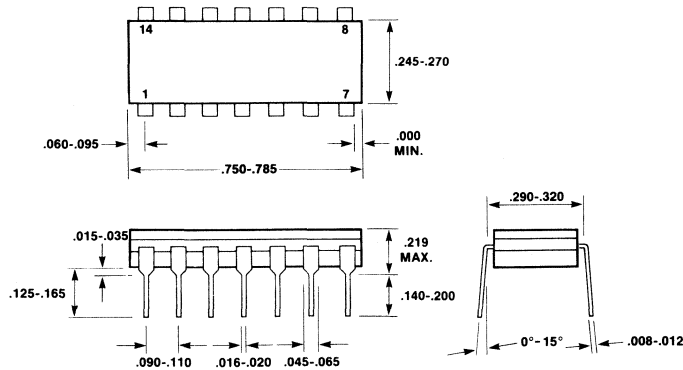


Test Waveform



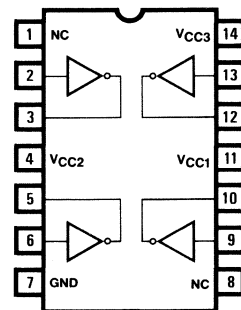
Package Drawing

14J Ceramic DIP



UNLESS OTHERWISE SPECIFIED:
 ALL DIMENSIONS MIN.-MAX. IN INCHES.
 ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.

Pin Configuration



Absolute Maximum Ratings

Supply voltage, VCC1	+8V
VCC2	+18V (HD-6600), +14V (HD-6605)
VCC3	+18V (HD-6600), +8V (HD-6605)
Input voltage	-1.5V to +5.5V
Input current	-25 mA to +5 mA
Output current	-300 mA
Storage temperature range	-65° to +150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	HD1-6600-2			HD1-6605-2			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
VCC1	Supply Voltage 1	4.5	5	5.5	4.5	5	5.5	V
VCC2	Supply Voltage 2	10	12	13.8	10	12	13.8	V
VCC3	Supply Voltage 3	4.5	5	5.5	4.75	5	5.5	V
IOH	High Level output current		-150	-200		-150	-200	mA
tA	Operating Free Air Temperature	-55		125	0		75	°C

Electrical Characteristics

Over Recommended Operating Free Air Temperature Range VCC2 = 12.0V VCC3 = 5.0V

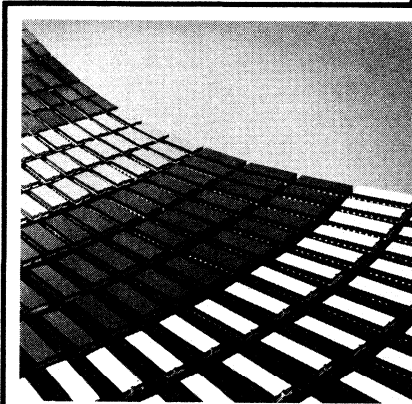
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
IIR IIF	Input Current	VIN = 2.4V VIN = 0.4V VCC1 = 5.5V		-80	30 -250	μA
VIH VIL	Input Threshold Voltage	VCC1 = 4.5V	2.0		0.8	V
VOH	Output Voltage (One strobe enabled)	VCC1 = 5.0V VIN = 0.4V IL = -150mA	4.75	4.85		V
VOL		VCC1 = 5.0V VIN = 2.4V IL = 500μA		0.7	1.0	V
ICC1	Supply Current (All strobes enabled)	VCC1 = 5.5V VIN = 2.4V		4	6.0	mA
ICC1		VCC1 = 5.5V VIN = 0.4V		4	6.4	mA
ICC2		VCC1 = 5.5V VIN = 0.4V IL = -150 mA		40	60	mA
ICC2		VCC1 = 5.5V VIN = 2.4V IL = 0		8	12	mA



Switching Characteristics

VCC2 = 12.0V VCC3 = 5.0V

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
ton	Turn On Delay	TA = 25°C VCC1 = 5.0V VCC2 = 12V VCC3 = 5.0V RL = 31.6Ω CL = 620 pF		40	75	ns
toff	Turn Off Delay			40	75	ns
tr	Rise Time			40	65	ns
tf	Fall Time			40	65	ns



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Setup Time

Setup time, t_{su}

The time interval between the application of a signal that is maintained at a specified input terminal and a consecutive active transition at another specified input terminal.

- NOTES: 1. The setup time is the actual time between two events and may be insufficient to accomplish the setup. A minimum value is specified that is the shortest interval for which correct operation of the logic element is guaranteed.
2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the logic element is guaranteed.

Voltage

High-level input voltage, V_{IH}

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the least positive value of high-level voltage for which operation of the logic element within specification limits is guaranteed.

High-level output voltage, V_{OH}

The voltage at an output terminal with input conditions applied that according to the product specification will establish a high level at the output.

Input clamp voltage, V_{IC}

An input voltage in a region of relatively low differential resistance that serves to limit the input voltage swing.

Low-level input voltage, V_{IL}

An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.

NOTE: A maximum is specified that is the most positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

Low-level output voltage, V_{OL}

The voltage at an output terminal with input conditions applied that according to the product specification will establish a low level at the output.

Negative-going threshold voltage, V_T^-

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{T+} .

Positive-going threshold voltage, V_{T+}

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{T-} .

Truth Table Explanations

H	= high level (steady-state)
L	= low level (steady-state)
↑	= transition from low to high level
↓	= transition from high to low level
X	= irrelevant (any input, including transitions)
Z	= off (high-impedance) state of a 3-state output
a..h	= the level of steady-state inputs at inputs A through H respectively
Q_0	= level of Q before the indicated steady-state input conditions were established
\bar{Q}_0	= complement of Q_0 or level of \bar{Q} before the indicated steady-state input conditions were established
Q_n	= level of Q before the most recent active transition indicated by ↓ or ↑

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0 , or \bar{Q}_0), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output.

Clock Frequency

Maximum clock frequency, f_{max}

The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

Current

High-level input current, I_{IH}

The current into * an input when a high-level voltage is applied to that input.

High-level output current, I_{OH}

The current into * an output with input conditions applied that according to the product specification will establish a high level at the output.

High-level output current, I_{CEX}

The high-level leakage current of an open collector output.

Low-level input current, I_{IL}

The current into * an input when a low-level voltage is applied to that input.

Low-level output current, I_{OL}

The current into * an output with input conditions applied that according to the product specification will establish a low level at the output.

Off-state (high-impedance-state) output current (of a three-state output), I_{OZ}

The current into * an output having three-state capability with input conditions applied that according to the product specification will establish the high-impedance state at the output.

Short-circuit output current, I_{OS}

The current into * an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

Supply current, I_{CC}

The current into * the V_{CC} supply terminal of an integrated circuit.

* Current out of a terminal is given as a negative value.

Hold Time

Hold time, t_H

The interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

- NOTES: 1. The hold time is the actual time between two events and may be insufficient to accomplish the intended result. A minimum value is specified that is the shortest interval for which correct operation of the logic element is guaranteed.
2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of data and the active transition) for which correct operation of the logic element is guaranteed.

Output Enable and Disable Time

Output enable time (of a three-state output) to high level, $tpZH$ (or low level, $tpZL$)

The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high (or low) level.

Output enable time (of a three-state output) to high or low level, $tpZX$

The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low).

Output disable time (of a three-state output) from high level, $tpHZ$ (or low level, $tpLZ$)

The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high (or low) level to a high-impedance (off) state.

Output disable time (of a three-state output) from high or low level, $tpXZ$

The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

t_{EA} is the output enable access time of memory devices.

t_{ER} is the output disable (enable recovery) time of memory devices.

Propagation Time

Propagation delay time, tpd

The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level.

Propagation delay time, low-to-high-level output, $tpLH$

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

Propagation delay time, high-to-low-level output, $tpHL$

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_{AA} is the address (to output) access time of memory devices.

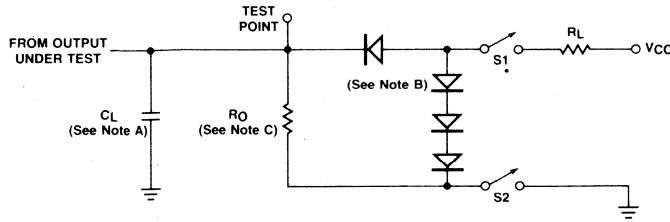
10

Pulse Width

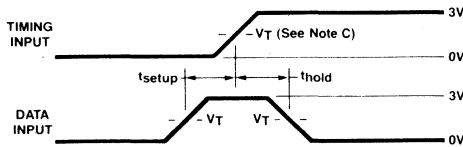
Pulse width, t_w

The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

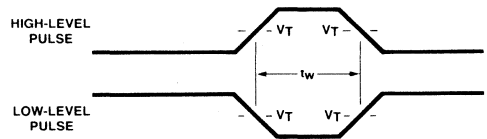
Standard Test Load



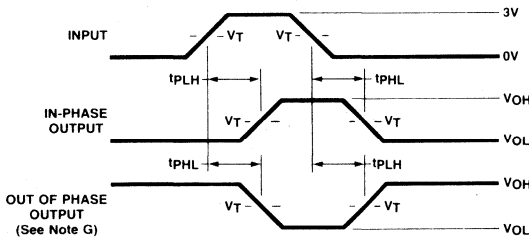
Test Waveforms



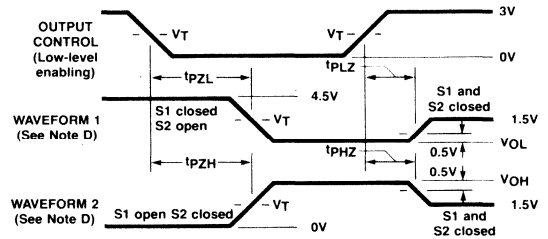
Setup and Hold



Pulse Width



Propagation Delay



Enable and Disable

- NOTES: A. C_L includes probe and jig capacitance.
 B. All diodes are 1N916 or 1N3064.
 C. For Series 54/74S, 57/67S, and PALS, $R_O = 1K$, $V_T = 1.5V$
 For Series 54/74LS and 57/67LS, $R_O = 5K$, $V_T = 1.2V$
 D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
 F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_{out} = 50\Omega$ and:
 For Series 54/74S and 57/67S, $t_r \leq 2.5$ ns $t_f \leq 2.5$ ns
 For Series 54/74LS and 57/67LS, and PALS, $t_r \leq 15$ ns $t_f \leq 6$ ns
 G. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

Programming Input Formats

MMI can program your ROM or PROM from input data in any of several types: truth table, punched cards, paper tape or pre-programmed ROM or PROM. However, the preferred input data for PROMS is paper tape and for ROMS punched cards.

Truth Table Inputs

Devices are programmed at our facility from MMI truth table forms (available on request). For customers desiring to make their own forms, examples are shown below:

4-BIT OUTPUT	WORD NUMBER	PIN	OUTPUTS			
			10	11	12	13
	0		O ₄	O ₃	O ₂	O ₁
	1		H	H	H	L

	255		L	H	H	H

8-BIT OUTPUT	WORD NUMBER	PIN	OUTPUTS							
			17	16	15	14	13	11	10	9
	0		O ₈	O ₇	O ₆	O ₅	O ₄	O ₃	O ₂	O ₁
	1		H	H	H	L	H	L	H	H

	511		L	H	H	H	H	H	H	L

NOTE: A high voltage on the data out lines is signified by an "H." A low voltage on the data out lines is signified by an "L." The word number assumes positive logic on the address pins, so for example, word 1023 = HHHHHHHHHH.

Paper Tape Format Inputs

Truth tables can also be sent to MMI in an ASCII tape in either a 7 or 8 level format. Send information air mail or TWX 910-339-9224. The tape reading equipment at MMI only recognizes ASCII characters S, B, H, L, F and E and interprets them respectively

The required heading information at the beginning of the tape is as follows:

CUSTOMER'S NAME AND PHONE _____	TRUTH TABLE NUMBER _____
CUSTOMER'S TWX NUMBER _____	NUMBER OF TRUTH TABLES _____
PURCHASE ORDER NUMBER _____	TOTAL NUMBER OF PARTS _____
MMI PART NUMBER _____	NUMBER OF PARTS OF EACH TRUTH TABLE _____
CUSTOMER SYMBOLIZED PART NUMBER _____	25 BELL OR RUBOUT CHARACTERS _____

An example is shown below for a 256 x 4 PROM (6300)

SCOTT ELECTRONICS 408 426-6134

TWX 911-338-9225

PO142

6300

0431

12

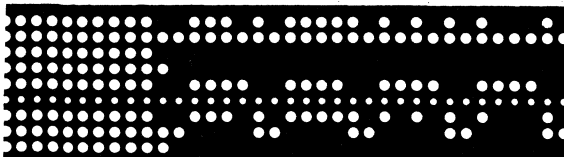
1

3

3

SBLLHF BLLLLF BLHLHF BLHHHF BLLHHF BHHHFF BLLLHF BLHLHF BLLLLF
 BLLLLF BLHLHF BLLHHF BHHHFF BHHLLF BLLHHF BHHLLF BLLHHF BLHLHF

8 level
TWX

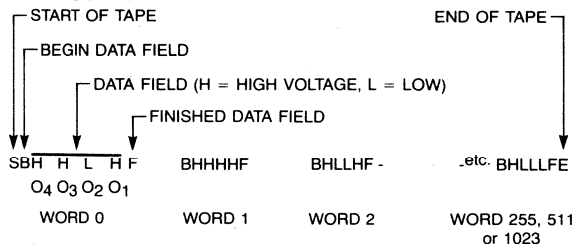


as Start, Begin a word, High data, Low data, Finish a word, and End of tape. All other characters such as carriage returns, line feeds, etc. are ignored so that comments and spaces may be sent in the data field to improve readability. Comments, however, should not use the characters S, B, H, L, F, E. Word addresses must begin with zero and count sequentially to word 31, 255, 511 or 1023 respectively.

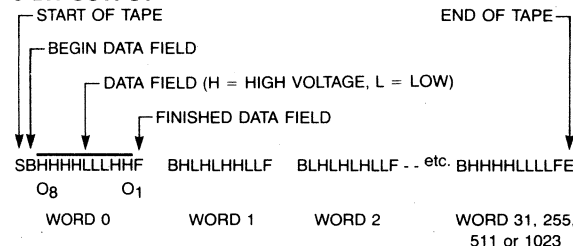
In order to assist the machine operator in determining where the heading information stops and the data field begins, 25 bell characters or rubout characters should precede the start of the truth table. Any type of 8 level paper tape (mylar, fanfold, etc.) is acceptable. Channel 1 is the most significant bit and channel 8 (parity) is ignored. Sprocket holes are located between channels 3 and 4. Note that the order of the outputs between characters B and F is O₄, O₃, O₂, O₁, not O₁, O₂, O₃, O₄.

A typical list of characters and their machine interpretations is shown below:

4-BIT OUTPUT



8-BIT OUTPUT



ROM Programming Punched Card

ROMs can be programmed using several input methods. These are truth table, punched cards in the format shown below, paper tape in the same format as cards, and paper tape in the ASCII BHLF format of the equivalent PROM.

Punched Card or Tape Input

First card or line (80 columns max.): enter Company Name, Part Number, Data, Number of "L's" in Pattern.

(Free Form Entry: no commas; Paper Tape Format: terminate each line with carriage return and linefeed).

Hexadecimal Format

In this format the heading required is identical to the BHLF format but the data is different. Instead of an "S," the hexadecimal data begins with the SOH character (control A). The data is then represented by the hexadecimal character (0-9 and A-F) which represents the output data of address 0, followed by a space. Next comes the output data of address 1 followed by a space, etc. The character ETX (control C) is used to end the data. Carriage return and the line feed may be included to format the data when the tape is printed.

CARD 1

COMPANY NAME CX 1816—2052 7—12—70 L = 796

2nd Card Or Line thru Last (80 Columns Max.)

ENTER WORD ADDRESS OF FIRST DATA FIELD IN COLUMNS 1 THRU 5

Enter First Data Field (O₁₀—O₁) in Columns 8 thru 17

Enter Second Data Field (O₁₀—O₁) in Columns 19 thru 28

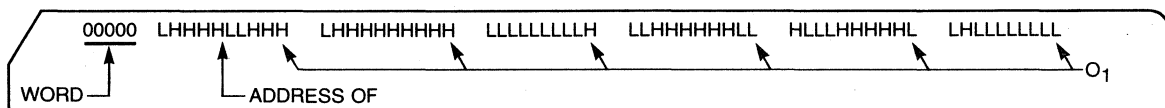
Enter Third Data Field (O₁₀—O₁) in Columns 30 thru 39

Enter Fourth Data Field (O₁₀—O₁) in Columns 41 thru 50

Enter Fifth Data Field (O₁₀—O₁) in Columns 52 thru 61

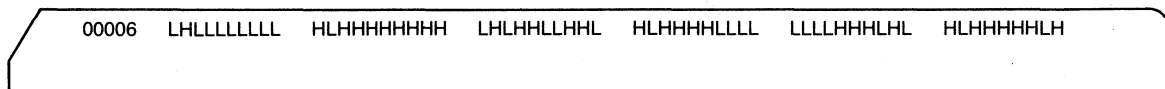
Enter Sixth Data Field (O₁₀—O₁) in Columns 63 thru 72

CARD 2

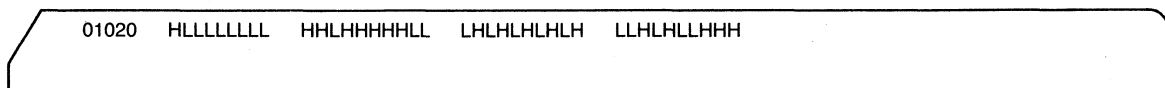


NOTE: Output 1 (O₁) is always in cols. 17,28,39,50,61,72

CARD 3



LAST CARD



NOTES:

1. Leading edge zeroes in the word number may be eliminated. Columns 73 thru 80 are for comments.
2. Regardless of the number of outputs which a particular ROM has, the data for a specific output always goes in a specific column.

Output 1 (01)	Columns 17, 28, 39, 50, 61, 72
Output 2 (02)	Columns 16, 27, 38, 49, 60, 71
Output 3 (03)	Columns 15, 26, 37, 48, 59, 70
Output 4 (04)	Columns 14, 25, 36, 47, 58, 69

- | | |
|----------------|--------------------------------|
| Output 5 (05) | Columns 13, 24, 35, 46, 57, 68 |
| Output 6 (06) | Columns 12, 23, 34, 45, 56, 67 |
| Output 7 (07) | Columns 11, 22, 33, 44, 55, 66 |
| Output 8 (08) | Columns 10, 21, 32, 43, 54, 65 |
| Output 9 (09) | Columns 9, 20, 31, 42, 53, 64 |
| Output 10 (10) | Columns 8, 19, 30, 41, 52, 63 |

3. 0 and 1 may replace L and H, but the customer must define for MMI whether 0 = L or 0 = H.

Application Notes

- *A Powerful Microprogram Controller the 67110*, October '76
- *First-In First-Out Memories... Operations and Applications*, March '77
- *How to Design Your Own Microprocessor*
- *Registered PROM's Impact Computer Architecture*, February '77

Handbooks

- *PAL™ Programmable Array Logic Handbook*

Manuals

- *Micro-Aid Micro-Assembler User's Manual*
- *Product Assurance Manual*,

Reliability Reports

- *Plastic Reliability Report*, RR8/March '78
- *PROM Reliability Report II*, April 1, '74
- *-1 Series Schottky Reliability Report*, R1-3-6/75
- *24-Pin CER-DIP Reliability Report*, R2-2-3/76

Custom Circuit Capability

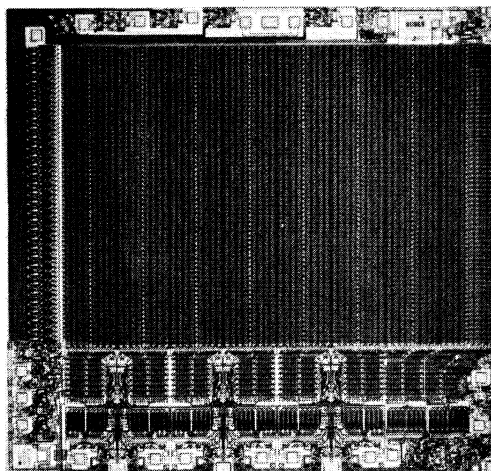
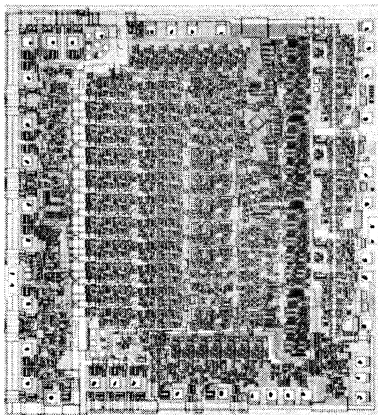
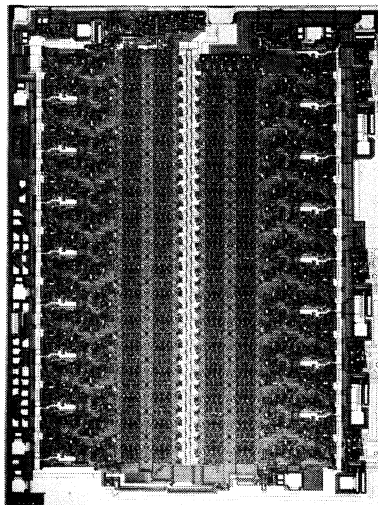
If the product you need hasn't appeared in this handbook you may be interested in Monolithic Memories Inc. custom circuit capability. We have a proven High Speed Schottky technology at your disposal which uses a combination of composite and redundant masking to attain some of the highest circuit densities (gate/MIL²) in the industry. This is not a process tailored to just memories. We can tackle a complex logic device of over a thousand gate complexity on chips up to 60,000+ MIL² on our new 100 MM (4") wafer fabrication line. Projection printing using low defect masks allows yields unheard of before.

We can also help you with your logic design from task conception to actual circuit implementation. Our computerized design aids will allow us to generate for you a complete AC and DC circuit analysis, logic simulation, test vector generation and final tapes for the pattern generator. Whether you already have a logic design or photo masks we can supply you with your choice of wafers, die or packaged devices, screened and tested to your special requirements.

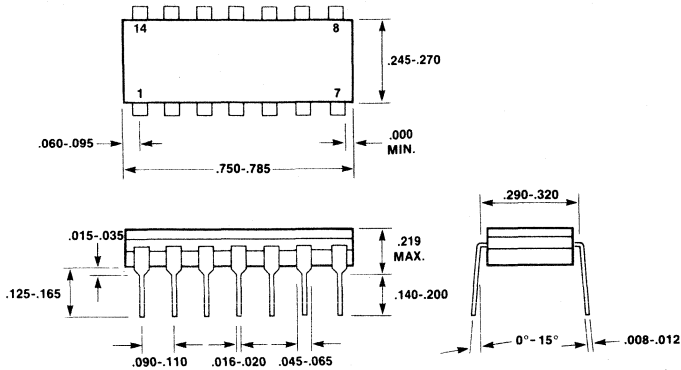
Processes Available

- EPI—3 μ m
- Ion implantation (Low Power Schottky)
- Dual layer metalization
- Deep collector "sinker" diffusion (for reduced RCS and VSAT)
- Platinum silicide Schottky technology using a titanium-tungsten diffusion barrier
- Washed emitters
- For programmable fuse structures nichrome or titanium-tungsten thin films
- Thin film nichrome resistors for radiation hardening
- Composite masking to reduce mask to mask misalignment tolerances
- I²L technology

For more information contact your factory representative.

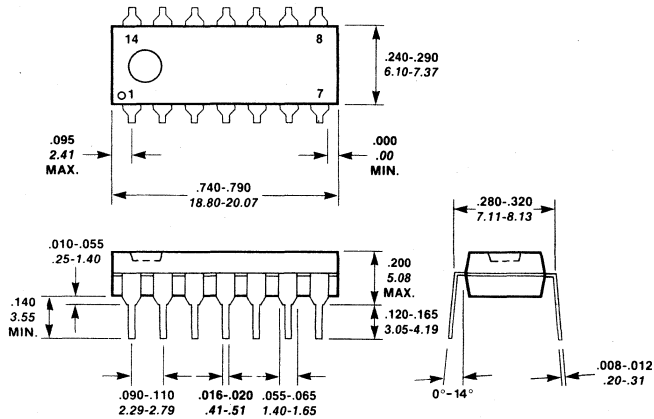


J14 Ceramic DIP



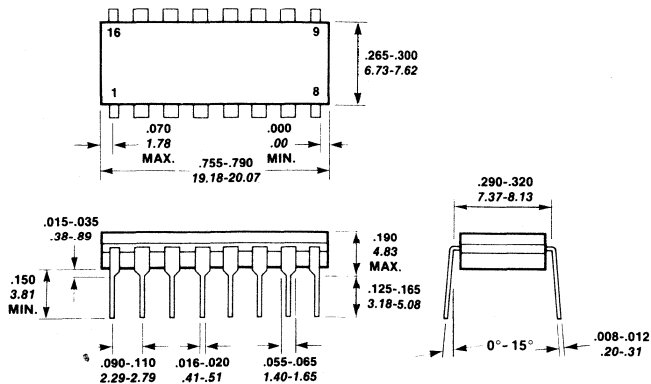
UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES.
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.

N14 Plastic Kool DIP™



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J16 Ceramic DIP

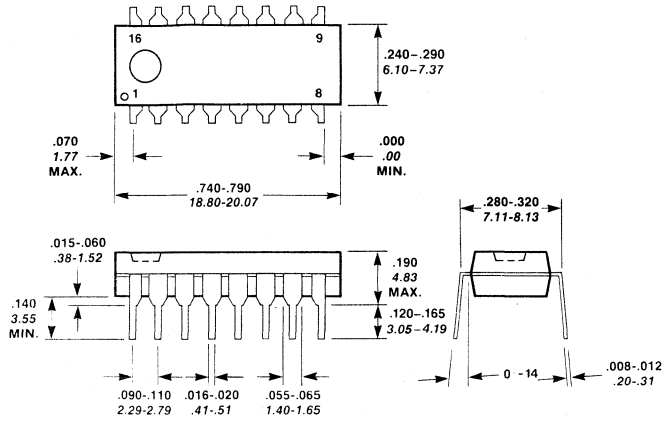


UNLESS OTHERWISE SPECIFIED:
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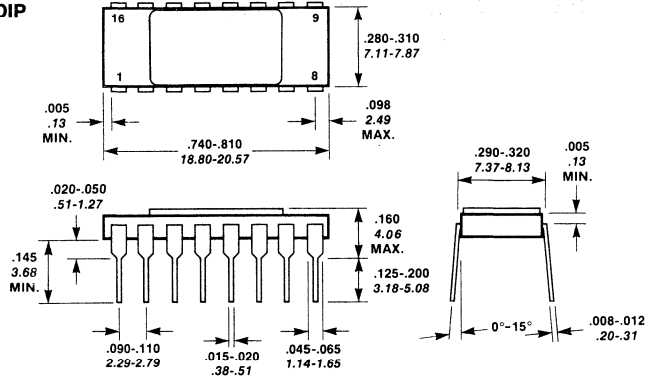
™Kool DIP is a trademark of Monolithic Memories.

N16 Plastic Kool DIP™



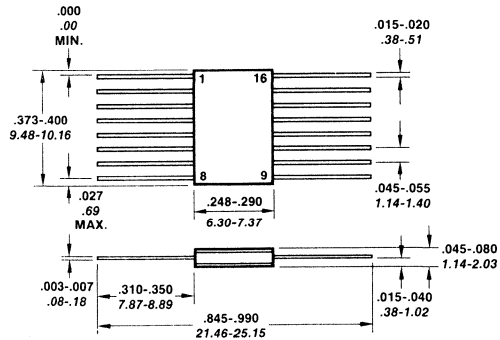
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D16 Side Brazed Ceramic DIP



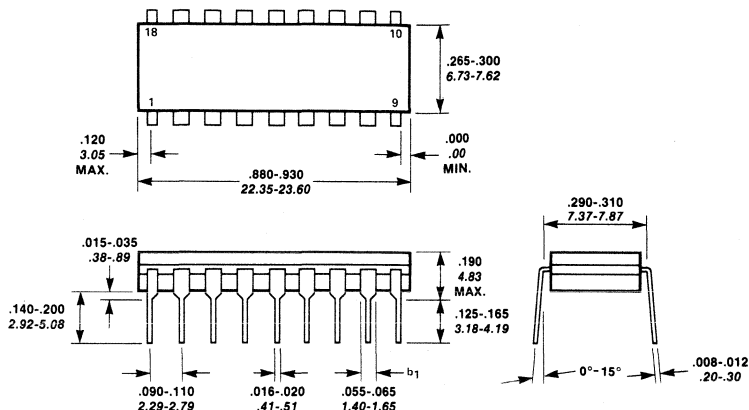
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ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.

F16 Flat Pack (Eutectic Seal)



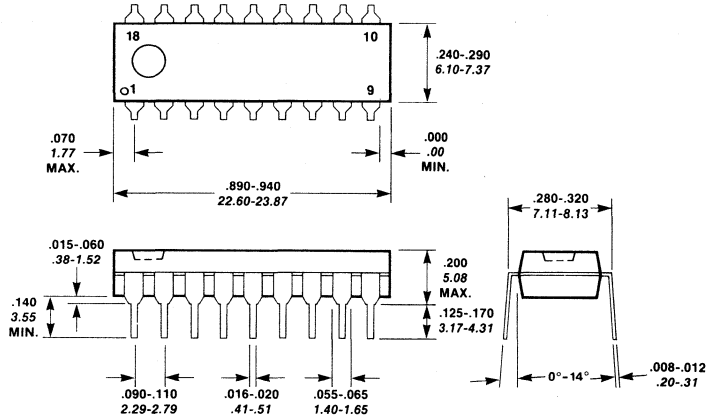
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J18 Ceramic DIP



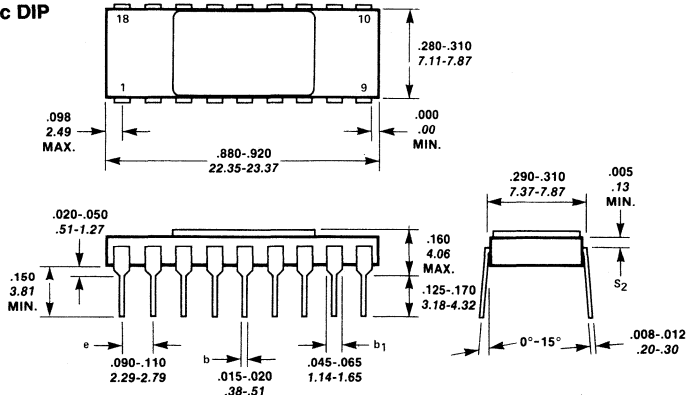
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ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.

N18 Plastic Kool DIP™



UNLESS OTHERWISE SPECIFIED:
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ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.

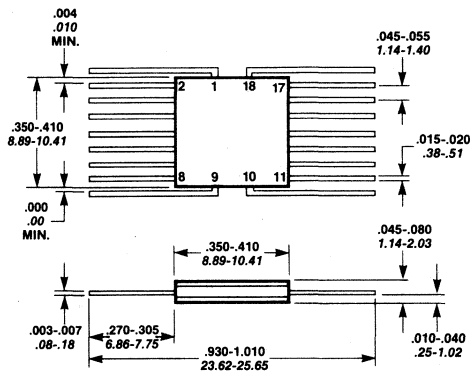
D18 Side Brazed Ceramic DIP



UNLESS OTHERWISE SPECIFIED:
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ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.

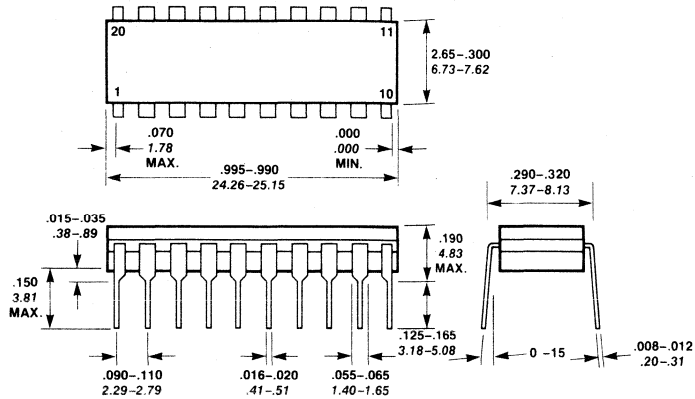
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F18 Flat Pack (Eutectic Seal)



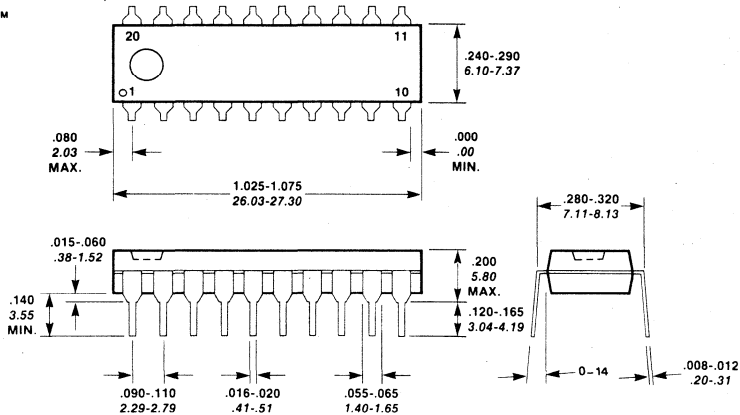
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J20 Ceramic DIP



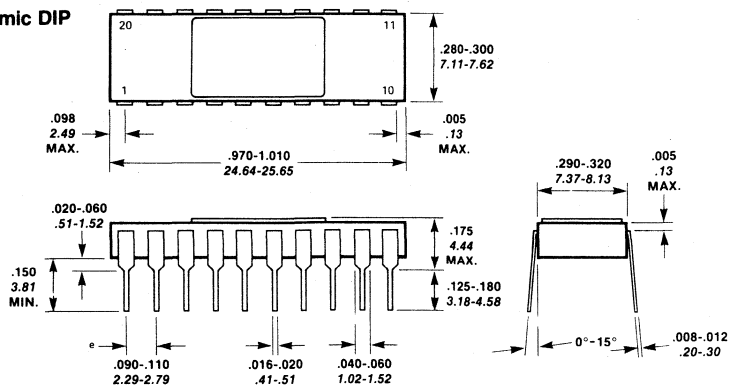
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ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.

N20 Plastic Kool DIP™



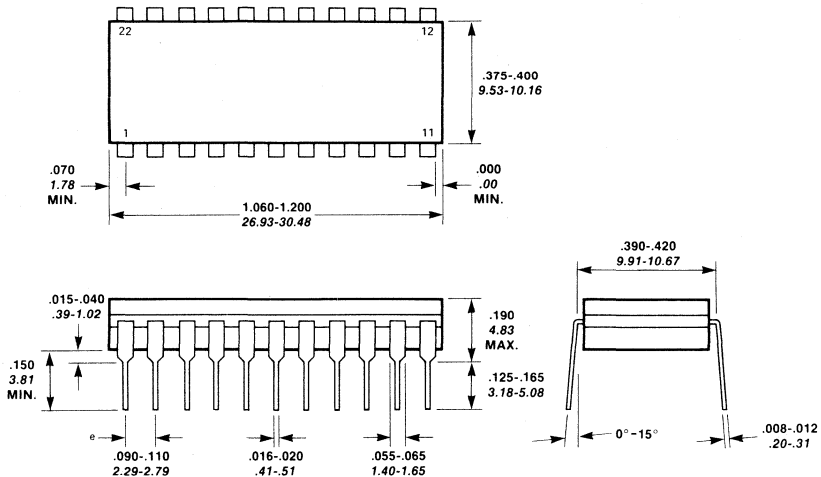
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D20 Side Brazed Ceramic DIP



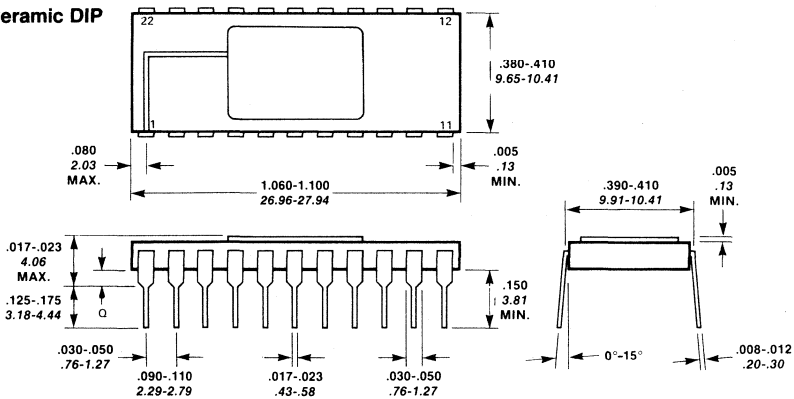
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J22 Ceramic DIP



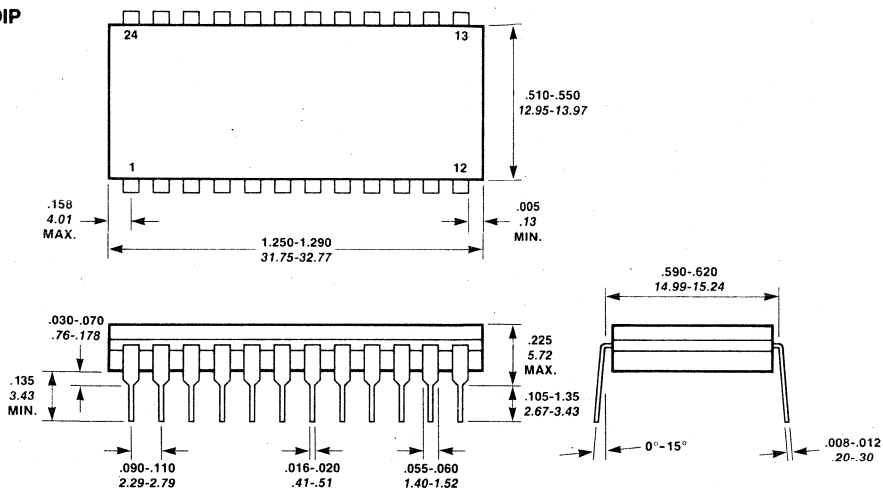
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D22 Side Brazed Ceramic DIP



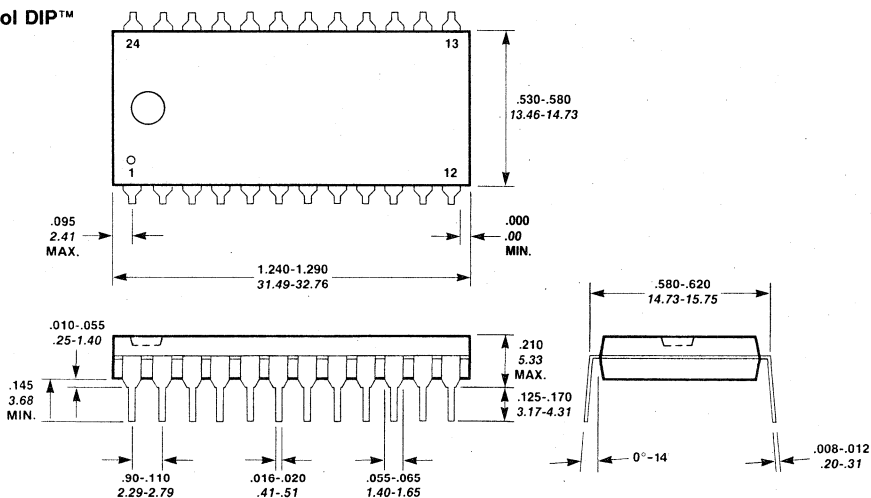
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J24 Ceramic DIP



UNLESS OTHERWISE SPECIFIED:
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ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS

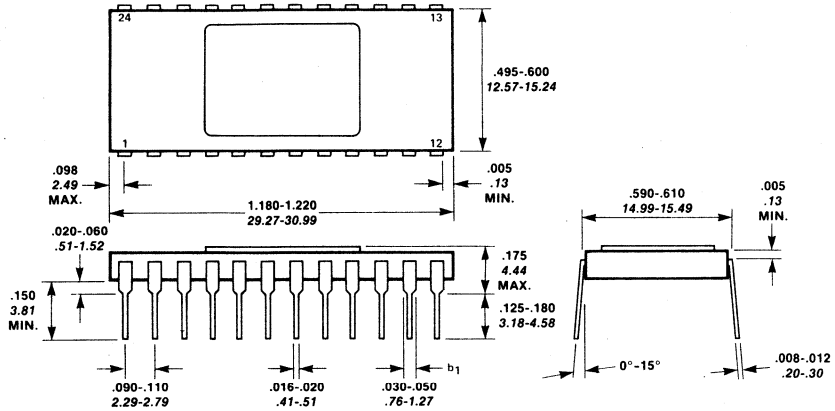
N24 Plastic Kool DIP™



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ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.

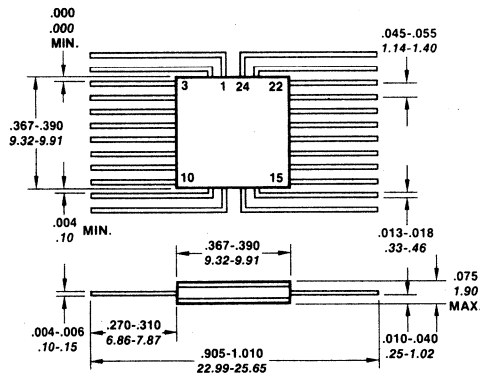


**D24 Side Brazed
Ceramic DIP**



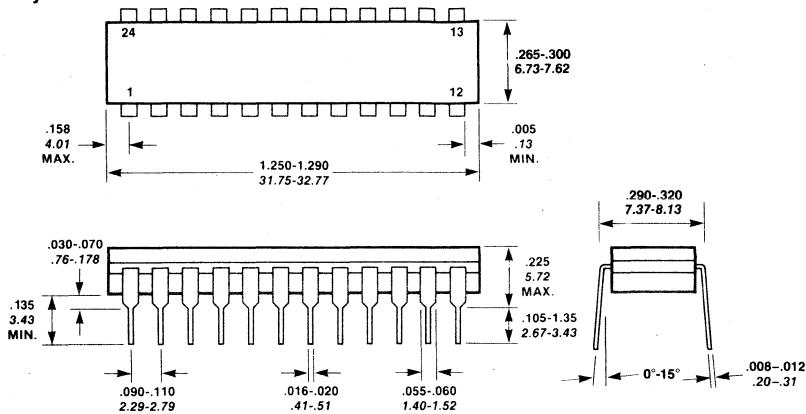
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F24 Flat Pack (Eutectic Seal)



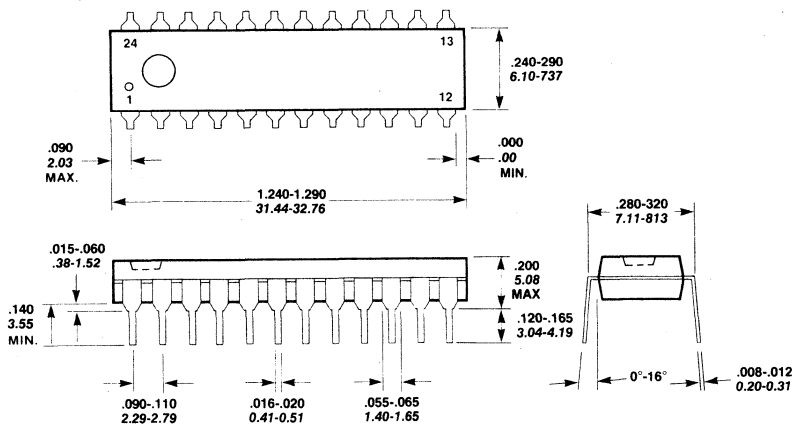
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ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.

J24S Ceramic "Skinny" DIP™



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES.
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS

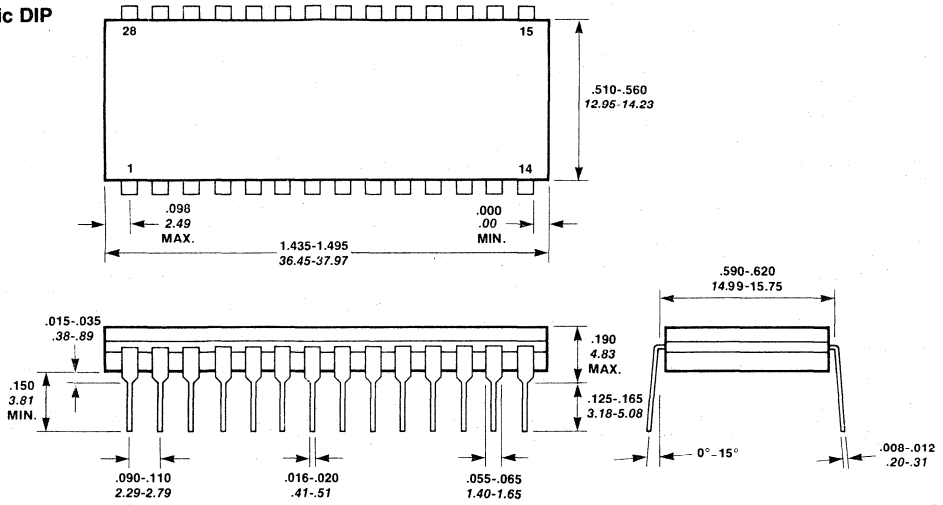
N24S Plastic Kool™ "Skinny" DIP™



UNLESS OTHERWISE SPECIFIED:
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ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.

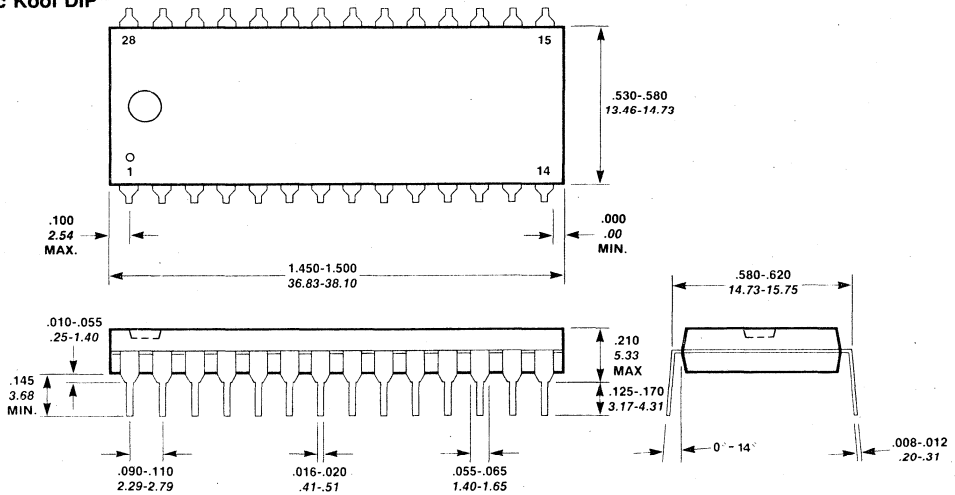
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J28 Ceramic DIP



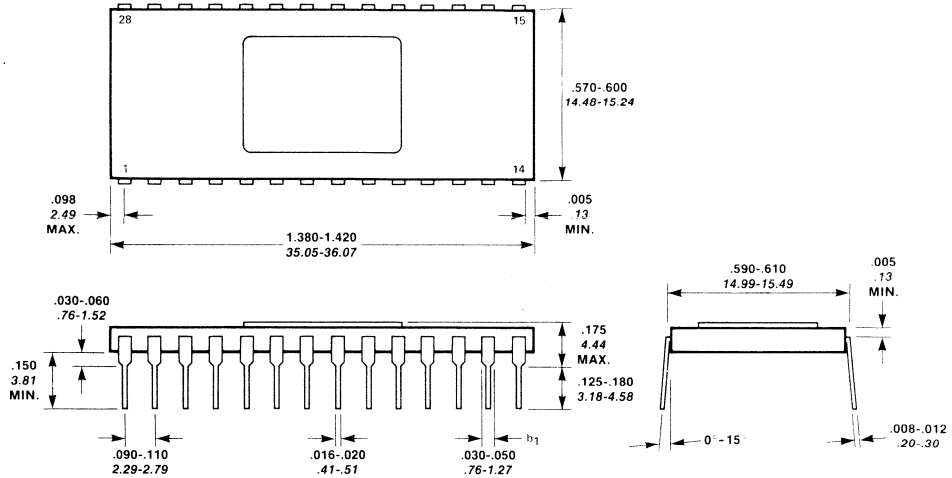
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ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.

N28 Plastic Kool DIP™



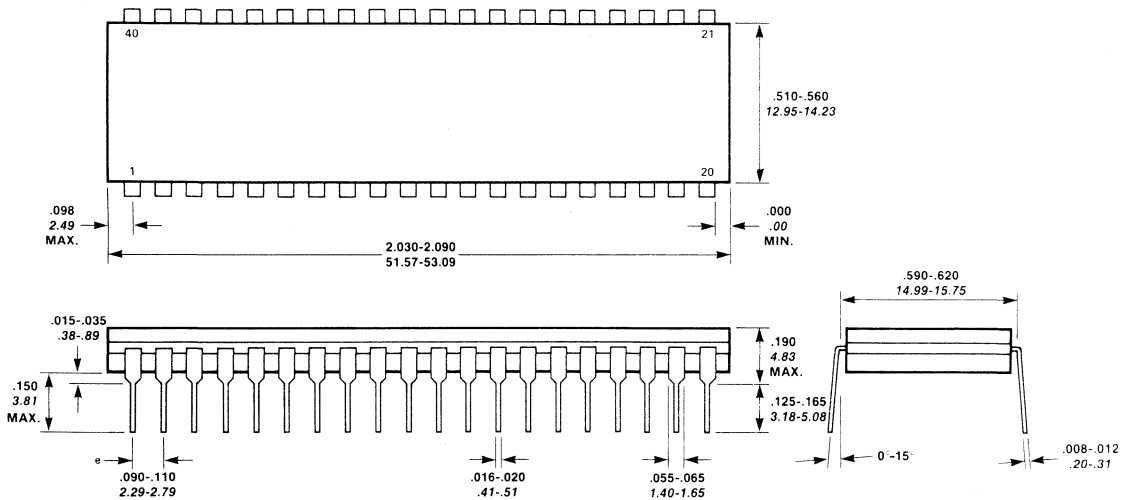
UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES.
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.

D28 Side Brazed Ceramic DIP



UNLESS OTHERWISE SPECIFIED:
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 ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.

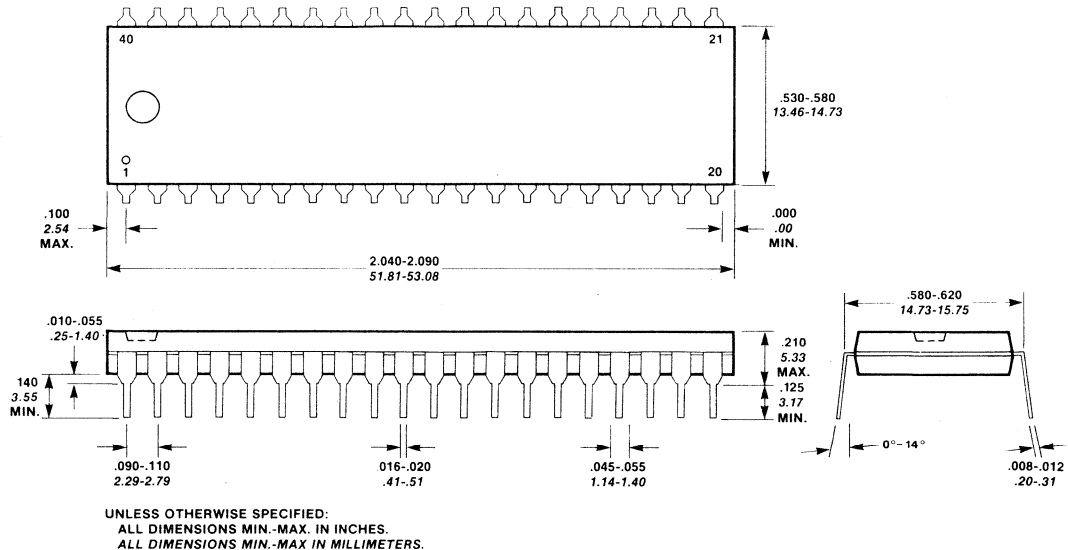
J40 Ceramic DIP



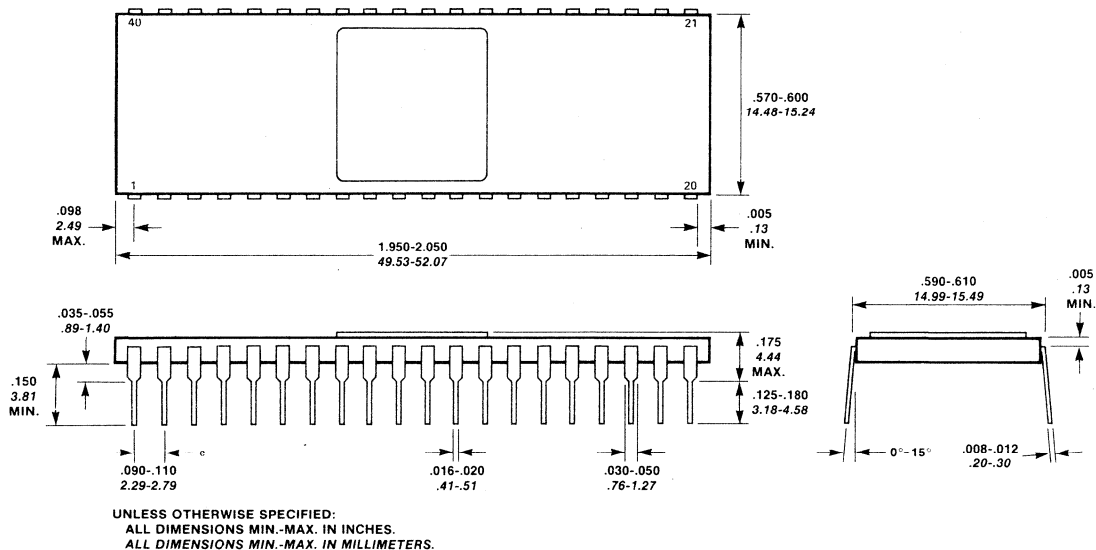
UNLESS OTHERWISE SPECIFIED:
 ALL DIMENSIONS MIN.-MAX. IN INCHES.
 ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS.

10

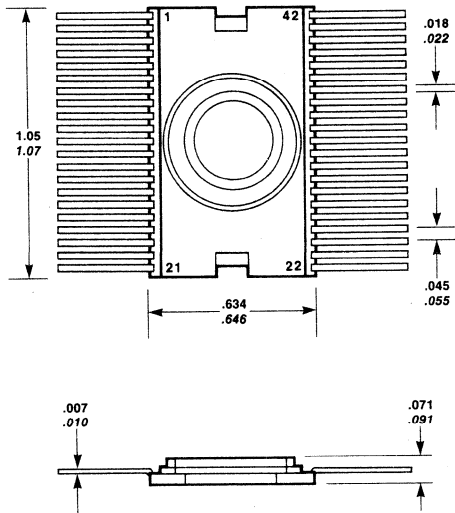
N40 Plastic Kool DIP™

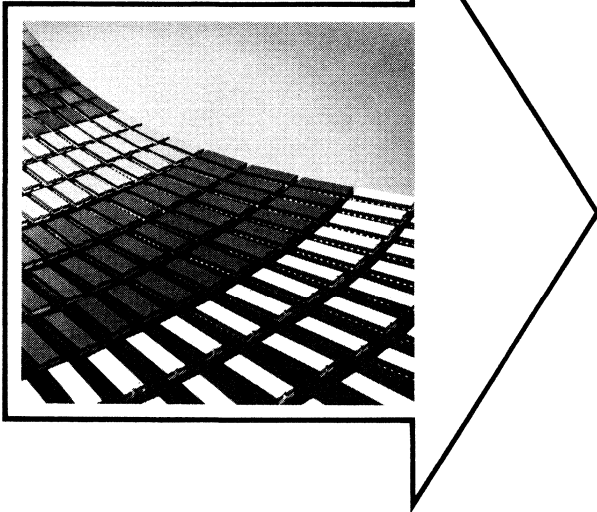


D40 Side Brazed Ceramic DIP



F42 Flat Pack (Eutectic Seal)





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RAMS	5
Programmable Logic	6
LSI Logic	7
Arithmetic Elements	8
Interface	9
General Information	10
Representatives/Distributors	11

MMI Area and Regional Sales Managers and FAEs

California		Illinois		New Jersey	
Huntington Beach		Lombard		Sussex	
Dick Siemiakowski	(714) 556-1216	Dick Jones, FAE	(312) 961-9200	Bill Bartley	(201) 875-9430
Long Beach		Naperville		Ohio	
Wayne Caraway	(714) 556-1216	Sal Graziano	(312) 961-9200	Lewisburg	
Santa Clara				Bob Ehrlich	(513) 885-5600
Jim Rapaich	(408) 988-2265			Texas	
		Massachusetts		Garland	
Florida		Framingham		Bob Rainwater	(214) 233-5833
Plantation		Russ French	(617) 655-7070	Plano	
Tom King	(305) 473-4227	Reading		Charlie Yole, FAE	(214) 233-5833
		Stan Karandanis	(617) 944-5535		

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U.S.A.

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Arizona		Kansas		Mentor	
Scottsdale		Olathe		Makin Associates	(216) 464-4330
Summit Sales	(602) 994-4587	Rush and West	(913) 764-2700	Oregon	
California		Maryland		Portland	
Culver City		Baltimore		Northwest Marketing	(503) 297-2581
Bestronics	(213) 870-9191	Monolithic Sales	(301) 296-2444	Pennsylvania	
Irvine		Massachusetts		Oreland	
Bestronics	(714) 979-9910	Needham Heights		CMS Marketing	(215) 885-5106
Mountain View		Comp Rep Associates	(617) 444-2484	Tennessee	
Thresum Associates	(415) 965-9180	Michigan		Jefferson City	
San Diego		Grosse Pointe		REP, Inc.	(615) 475-4105
Littlefield & Smith	(714) 455-0055	Greiner Associates	(313) 499-0188	Texas	
Colorado		Minnesota		Dallas	
Wheatridge		Minneapolis		West and Associates	(512) 451-2456
Waugaman Associates	(303) 423-1020	Nortec Sales	(612) 835-7414	Utah	
Connecticut		Missouri		Salt Lake City	
North Haven		Ballwin		Waugaman Associates	(801) 363-0275
Comp Rep Associates	(203) 239-9762	Rush and West	(314) 394-7271	Washington	
Florida		New Jersey		Bellevue	
Altamonte Springs		Teaneck		Northwest Marketing	(206) 455-5846
Dyne-A-Mark	(305) 831-2097	R.T. Reid Associates	(201) 692-0200	Wisconsin	
Clearwater		New York		Milwaukee	
Dyne-A-Mark	(813) 441-4702	Rochester		Sumer	(414) 259-9060
Fort Lauderdale		L-Mar Associates	(716) 328-5240	CANADA	
Dyne-A-Mark	(305) 771-6501	Syracuse		Ontario	
Georgia		L-Mar Associates	(315) 437-7779	Milton	
Tucker		North Carolina		Cantec	(416) 624-9696
REP, Inc.	(404) 938-4358	Raleigh		Ottawa	
Illinois		REP, Inc.	(919) 851-3007	Cantec	(613) 225-0363
Rolling Meadows		Quebec		Pierre Ponds	
Sumer	(312) 394-4900	Cantec			(514) 620-3121
Indiana					
Indianapolis					
Electro Reps	(317) 255-4147				

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Sterling Electronics (602) 258-4531

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Palo Alto
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San Diego
Intermark Electronics (714) 279-5200
Kieruff Electronics (714) 278-2112
Santa Ana
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Sunnyvale
Diplomat/Westland (408) 734-1900
Intermark Electronics (408) 738-1111
Tustin
Kieruff Electronics (714) 731-5711

Colorado
Denver
Kieruff Electronics (303) 371-6500
Wheatridge
Century Electronics (303) 424-1985

Connecticut
Hamden
Arrow Electronics (203) 248-3801
Wilton
Components for Industries (203) 762-8691

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Fort Lauderdale
Arrow Electronics (305) 776-7790
Hall-Mark Electronics (305) 971-9280
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Illinois
Elk Grove Village
Hall-Mark Electronics (312) 437-8800
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Indiana
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Advent Electronics (317) 297-4910

Kansas
Shawnee Mission
Hall-Mark Electronics (913) 888-4747

Maryland
Baltimore
Arrow Electronics (202) 737-1700
Pytronics/Savage (301) 792-0780
Gaithersburg
Pioneer Washington (301) 948-0710
Savage
Pytronics Industries (301) 792-0780

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Kieruff Electronics (617) 935-5134
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Lionex (617) 272-9400
Woburn
Arrow Electronics (617) 933-8130

Michigan
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Arrow Electronics (313) 971-8220
Farmington
Diplomat/Northland (313) 477-3200

Minnesota
Bloomington
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Hall-Mark Electronics (612) 884-9056

Missouri
Earth City
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New Hampshire
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Arrow Electronics (603) 668-6968

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Diplomat/IPC (201) 785-1830
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Arrow Electronics (609) 235-1900
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Kieruff Electronics (201) 935-2120
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Arrow Electronics (201) 797-5800

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Arrow Electronics (513) 253-9176

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Pioneer/Delaware Valley (215) 674-4000

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Austin
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Hall-Mark Electronics (713) 781-6100
Quality Components (713) 772-7100
Sterling Electronics (713) 627-9800

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Salt Lake City
Calron Electric Supply (801) 487-7451
Century Electronics (810) 972-6969

Washington
Seattle
Almac/Stroum Electronics (206) 763-2300
Tukwila
Kieruff Electronics (206) 575-4420

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Zentronics Limited (613) 238-6411
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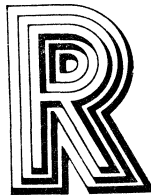
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ERRATA!

Following corrections should be added to your BIPOLAR LSI DATA BOOK 1979:

Page 2-21; Definition of waveforms:
Note:
During t_{AA} outputs are not defined!

Page 2-25; Definition of waveforms:
Note:
During t_{AA} outputs are not defined!

Page 6-4; Switching characteristics:
Military:
 t_{PD} typ = 25 ns
 t_{PD} max = 45 ns
Commercial:
 t_{PD} typ = 25 ns
 t_{PD} max = 40 ns

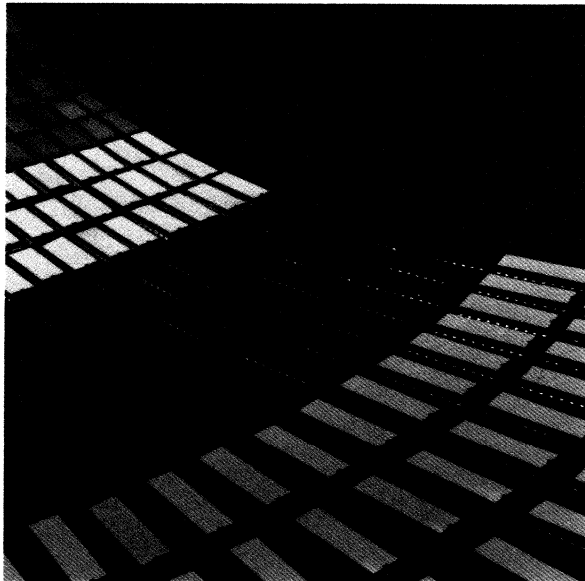
Page 11-4; Steiner, Austria:
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Bipolar LSI Data Book



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